# Bandgap Engineering Silicon Nanopillars

Thesis by

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# Abstract

Vertically oriented, bandgap engineered silicon nanopillars were fabricated and addressed. Devices were fabricated via a three dimensional etching process which created sub-5 nm constrictions in silicon radius upon oxidation. This effect was used to create a Coulomb blockade device. Devices were tested at room and liquid nitrogen temperatures. They showed a clear blockade effect distinctive of an asymmetric double tunnel junction at low temperatures which disappeared when tested at higher temperatures. Different device fabrication parameters were also tested to develop high-current devices, including chip anneal time. Furthermore, both device fabrication steps and current flow were modeled and simulated.

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# Chapter 1

# Introduction

## 1.1 Overview

Although transistor-like devices had been in employ for some time, the modern semiconductor transistor was invented by Moore, Bardeen, Brattain, and Shockley in December 1947, for which the latter three were given a Nobel prize in Physics in 1956. Large and unwieldy, their prototype still bears great similarity to the silicon counterparts we use today. Under the economic imperative of Moore's law, the transistor has seen its size reduced many orders of magnitude by industry. In doing so, semiconductor device manufacturers of the past half century have created a vast and efficient infrastructure with which to make their chips. Key to silicon's success as a platform is not its particular semiconducting characteristics, but rather its ability to easily form thin dielectric layers upon oxidation.

Meanwhile, the physicists who have carried on the tradition of Moore *et al.* have dived to smaller dimensions and more exotic materials in their quest for interesting devices. At low temperatures and length scales, quantum effects become important to the operation of fabricated samples, and it is the job of the physicist to tease out

their nature and implications.

This paper seeks to unite one such novel physical effect, Coulomb blockade, within the existing Complementary Metal-Oxide-Semiconductor (CMOS) platform which entire industries have been built around. By the deterministic nature of the fabrication process, this thesis seeks to model manufacturing of the device when it can and place important experimental signatures of successful operation within a broader context. The single-electron device presented herein has forged the path for reliable and repeatable single-electron transistors for use in future commercial applications.

## 1.2 Background

The primary manufacturing technique this thesis is concerned with is top-down fabricated silicon nanowires. In order to understand the subtleties in nanowire electrical performance, we will review important equations and concepts relevant to charge transport in semiconductor devices. Beginning with a classical formulation of the problem, it will move into a more complete and complex semiclassical description which is relevant as a demonstration of a certain range of experimental signatures we can discount upon measurement. Finally, the most relevant modeling paradigm for this paper will be presented and reviewed: the single-electron transistor.

### 1.2.1 Charge Transport in Nanostructures

Within semiconductors, charge transport and conduction is facilitated by two carriers - electrons and holes. An argument due to Landau casts these so-called electrons and

holes not as interacting free-space particles, but rather as quasiparticle charge carriers which carry a (different) effective mass and no longer interact. The key insight is to picture the particles as lying on the Fermi surface of the material. Briefly, because the charge carriers are confined to the Fermi surface and must stay in place due to the Pauli exclusion principle, their scattering cross-section goes to zero. This result implies that we may treat these quasiparticles without worrying about the microscopic interactions.

With these simplifications in mind, it becomes tractable to form a set of governing equations for transport in semiconductors.

$$\mathbf{J}_n/(-q) = -D_n \nabla n - n\mu_n \mathbf{E} \tag{1.1}$$

$$\mathbf{J}_p/q = -D_p \nabla p + p\mu_p \mathbf{E} \tag{1.2}$$

$$\frac{\partial n}{\partial t} = -\nabla \cdot \mathbf{J}_n + R \tag{1.3}$$

$$\frac{\partial p}{\partial t} = -\nabla \cdot \mathbf{J}_p + R \tag{1.4}$$

The above relations are known as the *Drift-Diffusion Equations*. Here, $n$ and $p$ are the densities of electrons and holes carrying charge $q$ with mobilities $\mu_n$ and $\mu_p$. Likewise, $\mathbf{J}_n$ and $\mathbf{J}_p$ are their respective electric currents. $R$ is a phenomenological term describing carrier generation and recombination (for instance Shockley-Reed-Hall recombination, an effect which is prominent in certain devices) and may be coupled to other variables in the equation. Finally, $\mathbf{E}$ describes the electric field. The diffusion coefficients are related to the mobility by $D_n = \mu_n k_B T/q$ and $D_p = \mu_p k_B T/q$.

Equations 1.1 and 1.2 describe the diffusive process of carrier transport as well as the directed, drift process of carrier transport due to an external electric field. Equations 1.3 and 1.4 are mass conservation terms.

In order to self-consistently describe carrier transport, the Drift-Diffusion Equations are not enough. Because the carriers themselves possess a charge, they in turn create external electric fields. To account for this, we must couple in Maxwell's equations. In order to simplify calculations, we assume we are in the electrostatic limit. This gives us the steady-state Poisson's equation:

$$\nabla^2\phi = \frac{q}{\epsilon}(n - p + N_A^- - N_D^+) \tag{1.5}$$

From equation 1.5, we can easily derive the electric field by taking the gradient of the potential $\phi$. The unfamiliar terms are $N_A^-$ and $N_D^+$ which represent the number of acceptor and donor impurities in the semiconductor, respectively, and $\epsilon$ which gives us the dielectric constant of the material.

Using these equations and proper boundary conditions and device geometry, it is possible to converge on a self-consistent solution which solves all of them to arbitrary accuracy. This is done by starting with a thermal background of carriers in the device and alternately solving the Drift-Diffusion and Poisson equations.

Figure 2.6 gives an illustration for just such a solution in a nanowire device. Note the I-V plot in figure 2.5. Although this equation does provide plenty of flexibility in the introduction of phenomenological terms, it lacks precision because it ignores important quantum effects which take place at the nanoscale.

### 1.2.2 Non-Equilibrium Green's Function Technique

Although in principle one may attempt to solve the Schrodinger's equation, doing so is intractable. Alternate methods to include quantum characteristics in charge transport have been studied. A promising method which was implemented during this thesis was that of Non-Equilibrium Green's Function (NEGF). Due to its wide use and relatively easy implementation, it serves as an excellent tool in studying complex nanostructures where quantum effects may become important. [10, 3, 4]

Although the Poisson equation remains the same, the Drift-Diffusion equations are replaced by their quantum analog. In our case, the device under question is discretized into a real-space grid. The energy at each grid point in the device is determined by the material property and transition rates between grid points are given by the effective mass approximation, with $\mathbf{k}$ the wavevector and $m^*$ the effective mass,

$$E(\mathbf{k}) = \frac{\hbar^2}{m^*}\mathbf{k}^2 \tag{1.6}$$

Note that the discretization may be done in different ways. For instance, a common practice is to use a tight-binding Hamiltonian and describe atomic orbitals separately. This process results in a matrix which describes the initial Hamiltonian of the device $H_0$. Adding in the charge carrier energy $E$, the electric potential $U$, and the self-energy of the device $\Sigma$, we can define a Green's function:

$$G = [EI - H_0 - U - \Sigma]^{-1} \tag{1.7}$$

If we define the in-scattering function

$$\Sigma^{in} = \Sigma_1^{in} + \Sigma_2^{in} + \Sigma_s^{in} \tag{1.8}$$

We can get the correlation function

$$G^n = G\Sigma^{in}G^\dagger \tag{1.9}$$

The self-energy function from the Hamiltonian is given as

$$\Sigma = \Sigma_1 + \Sigma_2 + \Sigma_s \tag{1.10}$$

Where the 1, 2, and $s$ subscripts denote scatterings from the first and second leads as well as from the device itself.

If we finally define

$$A = i[G - G^\dagger] \quad \Gamma = i[\Sigma - \Sigma^\dagger] \tag{1.11}$$

then we can use all of these equations to determine important device properties. The density of states is given by the diagonal elements of $\rho$.

$$\rho = \frac{1}{2\pi}\int \mathrm{d}E\ G^n(E) \tag{1.12}$$

And the current at a lead $i$ given by

$$I_i = \frac{q}{2\pi\hbar}\int \mathrm{d}E\ \mathrm{Tr}[\Sigma_i^{in}A] - \mathrm{Tr}[\Gamma_i G^n] \tag{1.13}$$

Where in both cases we integrate over incoming carrier energy $E$. Again, these equations must be solved self-consistently with the Poisson equation 1.5, using $U$ as the potential term. It is important to note that the current resulting from such calculations is that in ballistic transport - where the carriers do not interact with phonons or scatter from impurities, although it may capture transport and mixing between different subbands of the device.

### 1.2.3 Single Electron Devices

Although the previous methods are quite versatile and can explain a large range of device behavior, they are lacking when discussing strongly non-perturbative effects such as Coulomb blockade. Nonetheless, the theory for single electron device operation is comparatively simple. To illustrate the function of such devices in a somewhat general scenario, we will focus on the single electron transistor (SET).

The fundamental unit of the SET is the single electron box (also known as the island or quantum dot). Due to its small size, the addition of an electron has a large effect on the addition of further electrons. We may write the electron addition energy $E_a$ as

$$E_a = q^2/C + E_k \tag{1.14}$$

Where $C$ is the island's capacitance and $E_k$ is the kinetic energy of the electron in the dot. When this energy is roughly an order of magnitude larger than the thermal energy, we may see charging effects manifest themselves. The inclusion of an electron

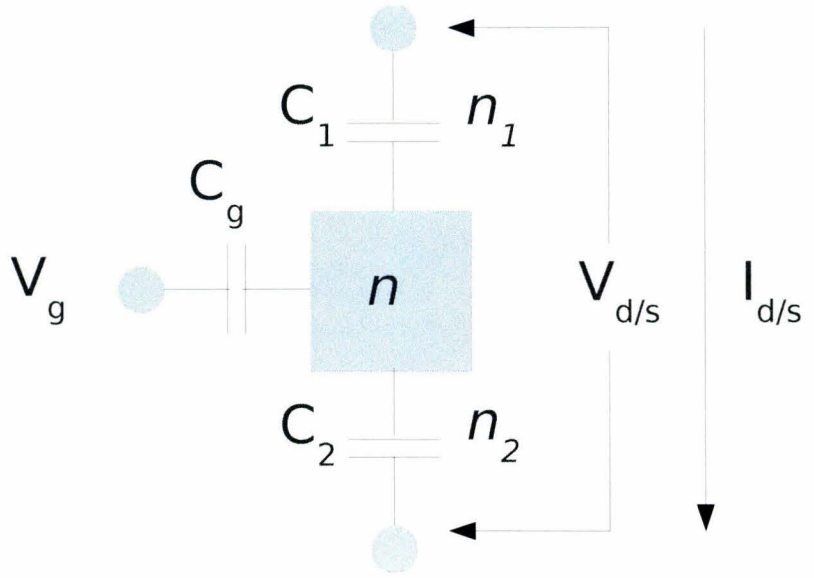


Figure 1.1: Schematic demonstrating principles of single electron transistor. A bias voltage is applied across $V_{d/s}$ and the inner electron box is modulated by $V_g$. The tunneling barriers are labeled by 1 and 2. Equation 1.15 describes the energy of the full device.

raises the energy of the box, thereby prohibiting further electrons from entering.

We now refer to figure 1.1. In this figure, we note two leads, the source and drain, as well as a gate modulating the potential of the electron island. The source and lead are separated by tunnel junctions from the inner island and the gate is capacitively coupled to it. We can write an expression for the total energy of the system[11].

$$U = \frac{1}{2C_\Sigma}(nq - V_g C_g)^2 - 2qV_{d/s}(n_1 C_2 + n_2 C_1)) \tag{1.15}$$

The amount of electrons inside the box $n$ is given by $n_1 - n_2$, which are the rates of electron flow from the second and first tunnel junction respectively. The capacitances are labeled for their terminal as are the voltages. Furthermore, $C_\Sigma = C_g + C_1 + C_2$.

Using this simple equation, we can derive from energy arguments the full range

of behavior of single electron devices. We begin at low bias voltages, where the right half of the equation may be ignored. Here we see that there is no advantage to adding more electrons to the inner dot so no current flows. However, past a certain threshold voltage it does become advantageous for current to flow. If the capacitances of the tunnel junctions are equal, then this results in a linear I-V curve past the threshold. If they are strongly asymmetrical, then it is possible for the tunneling rates to be different, resulting in a staircase-like pattern in the IV diagram as the box fills up with electrons.

An alternate way to get Coulomb oscillations is to look at the variations in current due to gate modulation. By changing the $V_g$ term, we can influence central island occupation, resulting in different tunneling rates between the two leads. Once again, a characteristic staircase structure arises from this consideration.

Taken together, these results give "Coulomb diamonds" which are readily seen in transconductance and I-V plots. From this it is possible to indirectly track electron occupation number within the dot.

## 1.3 Etching for Coulomb Blockade Devices

Silicon nanowires (SiNWs) have attracted considerable attention as platforms for nanoscale physics experiments over the past twenty years[15]. Recent work has used nanowires as cell probes[20], ion sensors[12], as thermoelectric[26] and as basic electronic components such as SiNWFETs[2].

The fabrication of SiNWs has progressed along two distinct paths; "Top-Down"

and "Bottom-Up." The bottom-up approach concentrates on growing wires using the vapor-liquid-solid technique[2]. Difficulty in specifying nanoparticle size and position has led to most groups relying on stochastic growth techniques. Typically nanowires are grown, cleaved off and suspended in a solvent, spun onto a receptive substrate and then an SEM is required to find appropriate targets for electrical contacting. Although this technique has been used with great success to create innovative devices it is unfortunately limited to the laboratory as it would be difficult to insert into the current CMOS fabrication paradigm. In response, several groups have extended fabrication capabilities to create SiNWs in a top-down method[14, 21, 6].

Using a novel three-dimensional etching process of silicon[24] and a self-terminating oxidation, single electron devices were created. The operational principle is to use the increased confinement at pinched regions of the fabricated device to cause an increase in bandgap. This is a well-known result in sub-10 nm diameter silicon nanowires from experiment and tight-binding calculations[23, 25, 16]. Using this increase in bandgap as a tunnel junction, the aim is to create a reproducible, reliable single electron transistor. This effect is schematically shown in figure 2.1(c).

# Chapter 2

# Methods

## 2.1 Fabrication

Fabrication of devices occurred in the Kavli Nanoscience Institute (KNI) cleanroom. Following standard CMOS techniques, samples were kept in a dust-free cleanroom environment until testing. Aligned electron beam lithography took place across several steps. The system is a Leica EBPG 5000+. For e-beam lithography for metal lift-off, first a layer of poly-methyl methacrylate (PMMA) at 2% concentration in anisole (A2) is spun at 4000 RPM on individual chips, then baked at 180 °C. After electron beam exposure, the chip is developed in 1:3 methyl-isobutyl ketone (MIBK) to isopropanol (IPA) solution for 20 seconds.

Initially, alignment pads are defined on the samples with the EBPG and etched via deep reactive ion etching a few microns deep. Each area to be tested has three squares of such alignment pads with sides of 2 mm, 3 mm, and 4 mm distances. These pads serve as markers for subsequent steps and show up darker during scanning electron microscope (SEM) imaging of the device. The etched marker design was chosen due to its robustness to later etching and deposition steps. The EBPG then uses these to

appropriately rotate and then write the subsequent steps.

After initial marker construction, the chips are aligned manually before being placed back into the EBPG. Each aligned area contains five separate pillars which are to be addressed individually. The samples are developed and a thin layer of aluminum oxide is sputtered on top. This takes place in a Lesker sputtering system at 20 mTorr in 100:1 Ar:$O_2$ atmosphere by sputtering an aluminum target at 400 W. This forms an excellent high-contrast etch mask[6]. After the oxide is deposited, the rest of the PMMA is lifted off by soaking in dichloromethane.

### 2.1.1 Etching

Etching was carried out in an Oxford inductively-coupled plasma reactive ion etcher (ICP-RIE) under a mixed mode etching and passivating process. The silicon was etched under a fluorine chemistry ($SF_6$) and suppressed by formation of a fluorinated polymer from $C_4F_8$. The etching is not reliant on silicon crystal axis.

Profile modulation was achieved by varying the ratio of these two gases and the forward power of the etch. This influences the angular distribution of the ions which gives a spread to the etch and creates an undercut. Under lower passivation gas concentrations, the etch undercuts. To continue the narrowed etch as a vertical sidewall, the forward power is increased and the ions collimated, decreasing their angular distribution. To under-etch the sample, more passivation gas was introduced to the etch chemistry in order to create a stronger buffer layer from the reactive species. By controlling the gas ratios as well as the forward power, a diverse set

of structures may be etched. In our case, the etch is continued straight for several hundred nanometers, then pinched in and out twice in rapid succession to create a bead near the base. Such a device is shown in figure 2.1(a).

### 2.1.2 Coulomb Blockade Device

Samples are then oxidized in a furnace at 925 °C until self-terminated. This leaves thin current apertures as effective tunnel barriers in the device. After oxidation, the samples are prepared by spinning a thin layer (200-400 nm) of PMMA on top and baking at 180 °C for five minutes. To remove residual PMMA which possibly wicked up the sides of the pillars, the samples are placed in an oxygen asher for 30 seconds at 75 W power and 300 mTorr. Finally, the samples are developed in buffered hydrofluoric acid (BHF) for 20 seconds, or until the inner silicon core is exposed. This step is often checked by SEM. The PMMA is removed in dichloromethane and the samples are aligned in the EBPG once again under fresh PMMA.

After alignment, the top contacts are written to the Coulomb blockade device. Once developed, they are placed in the Lesker sputtering system. Roughly 50-100 nm of titanium are sputtered on the target at 175 W. After this, several hundred nanometers of gold are sputtered at 80 W. This creates a Ti/Au top contact, wherein the gold serves as a protective layer against titanium oxidation. After the metal is lifted off with dichloromethane, the back side of the sample is swabbed with hydrofluoric acid in order to etch away any remaining thermal oxide. The samples are then placed back in the sputtering system upside-down where aluminum is sputtered on

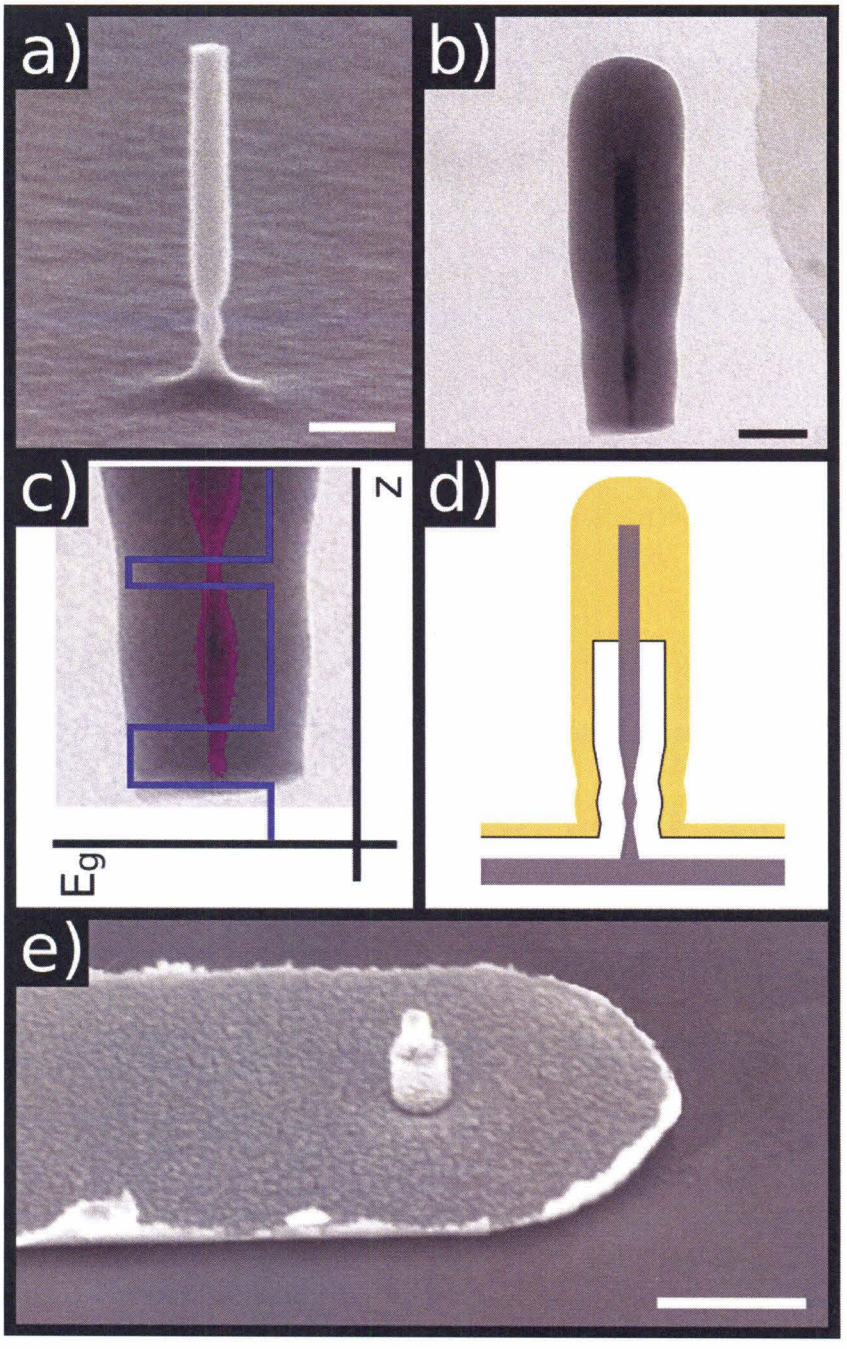


Figure 2.1: Fabrication and schematic of double tunnel junction device. (a) SEM of as-etched, sculpted, silicon nanopillar. Scale bar is 100nm. (b) TEM of oxidized double tunnel junction pillar after removal from the substrate. Scale bar is 50nm. (c) Schematic placed over the TEM image showing regions of widened silicon bandgap after oxidation. (d) Schematic of the completed device. (e) SEM of the completed device. Scale bar is 500 nm.

the back to protect against oxidation and create good contact. Finally, the devices are annealed in a rapid thermal annealer (RTA) under various conditions. Upon completion, the chips are cleaved into smaller subsections and wire bonded onto a chip holder.

### 2.1.3 Single Electron Transistor

Single electron transistor fabrication proceeds similarly. The process flow is shown in figure 2.2. Before the initial decapitation step, a gate contact is defined in the EBPG. A thin layer of titanium (for adhesion) followed by roughly 50 nm of gold is deposited as the gate metal. This is then lifted off in dichloromethane. After this, 200 nm of PMMA are spun on the chip and baked. The sample is placed in type TFA gold etchant for seven seconds. This defines the gate height. The PMMA is dissolved away and a fresh, slightly higher (250-300 nm) layer is spun on. The pillar is then decapitated by a 20 second buffered hydrofluoric acid etch. After removing this PMMA, the pillars are placed in a plasma-enhanced chemical vapor deposition system (PECVD) where a 150 nm layer of silicon dioxide is deposited on the substrate. This protects the top contact and gate from shorting. A layer of PMMA is spun on and the top of the deposited oxide is etched away in a similar fashion as before. This is done separately because of the noticeably different etch rates of thermal and PECVD oxide in BHF. Finally, the samples are prepped for an aligned write on the EBPG. After top contact definition, the process continues as before.

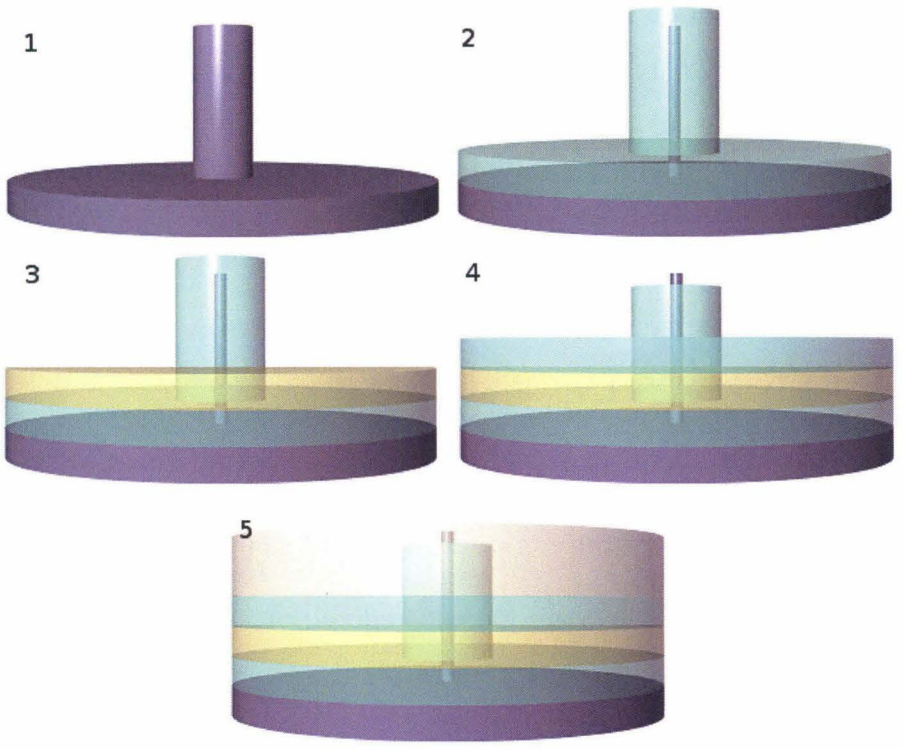


Figure 2.2: Process flow of transistor manufacture. Note that this schematic does not show the corrugations present in real devices. (1) Etching of silicon. (2) Thermal oxidation until self-termination. (3) Deposition of gate. (4) Decapitation of thermal oxide, deposition of PECVD oxide, and second decapitation thereof. (5) Top contact deposition

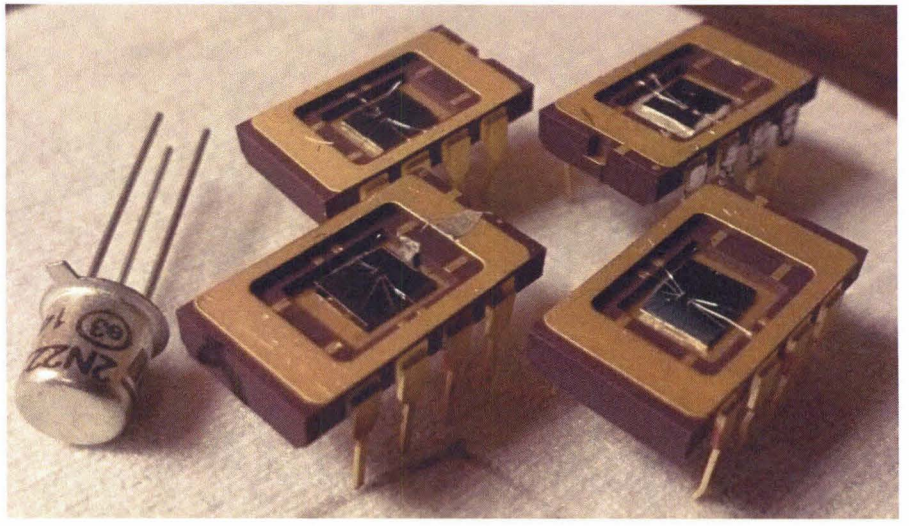

Figure 2.3: Picture showing completed chips after wirebonding to holders. Shown is a 2N222 NPN type tin-can transistor for comparison.

## 2.2 Simulation

### 2.2.1 Thermal Oxidation of Corrugated Silicon Nanopillars

Because straightforward etching cannot reach regimes where quantum confinement becomes important, further reduction of the active silicon radius is obtained by a self-terminating oxidation process. Since the original Deal-Grove paper[5] considerable research has been done in describing oxidation rates of surfaces with curvature[8]. Two complementary theories describe this step. Cui *et al* cite the creation of a high-stress region in the oxidation as inner radius narrows and a subsequent reduction in diffusivity as the reason for a decrease in the reaction rate[1]. Ma *et al* instead rely on a phenomenological approach and describe the process via pressure and strain dependent viscosities and reaction rates in the silicon, successfully applying their model to two-dimensional structures[13].

A multiphysics model was developed which coupled creeping flow of the oxide to oxidant diffusion. Strain dependence was incorporated via the following:

$$k_s = k_{s0}(T)\exp(-\frac{\sigma_{nn}V_r}{kT}) \tag{2.1}$$

$$D = D_0(T)\exp(-\frac{pV_d}{kT}) \tag{2.2}$$

$$\eta = \eta_0(T)\frac{\sigma_s V_c/(2kT)}{\sinh(\sigma_s V_c/(2kT))} \tag{2.3}$$

Where $\sigma_{nn}$ is the normal stress on the oxidation interface, $p$ is the hydrostatic pressure, and $V_r$, $V_d$, and $V_c$ are fitting parameters with values from Ma *et al*[13]. $D$ is the

diffusivity of oxidant, $\eta$ the viscosity of oxide, and $k_s$ the rate of the oxidation reaction.

The oxide growth is governed by creeping flow equations in radial coordinates ($\mathbf{u}$ is the velocity of the oxide):

$$\nabla p = \eta \nabla^2 \mathbf{u} \tag{2.4}$$

$$\nabla \cdot \mathbf{u} = 0 \tag{2.5}$$

The oxidant diffusion within the silicon dioxide is simply governed by the diffusion equation in radial coordinates:

$$\frac{d\phi}{dt} = D(p,T)\nabla^2 \phi \tag{2.6}$$

With these simulations, the pinching of bumps from an initially corrugated structure becomes apparent, as in figure 2.4. High-strain regions form on the inner dot surface and regions of great curvature. Furthermore, it is feasible to imagine extending these simulations to entire pillars, although that lies outside the range of possibility with this particular solver.

### 2.2.2 Modeling Transport in Silicon Nanopillars

To get a classical baseline for the current-voltage characteristics of devices, TEMs of small corrugated pillars were digitized and their borders input into a multiphysics modeling program with the classical drift-diffusion and Poisson equations. An image of the simulated structure as well as current plots are given in figures 2.6 and 2.5.

Using the framework of NEGF, two separate models were considered. One di-

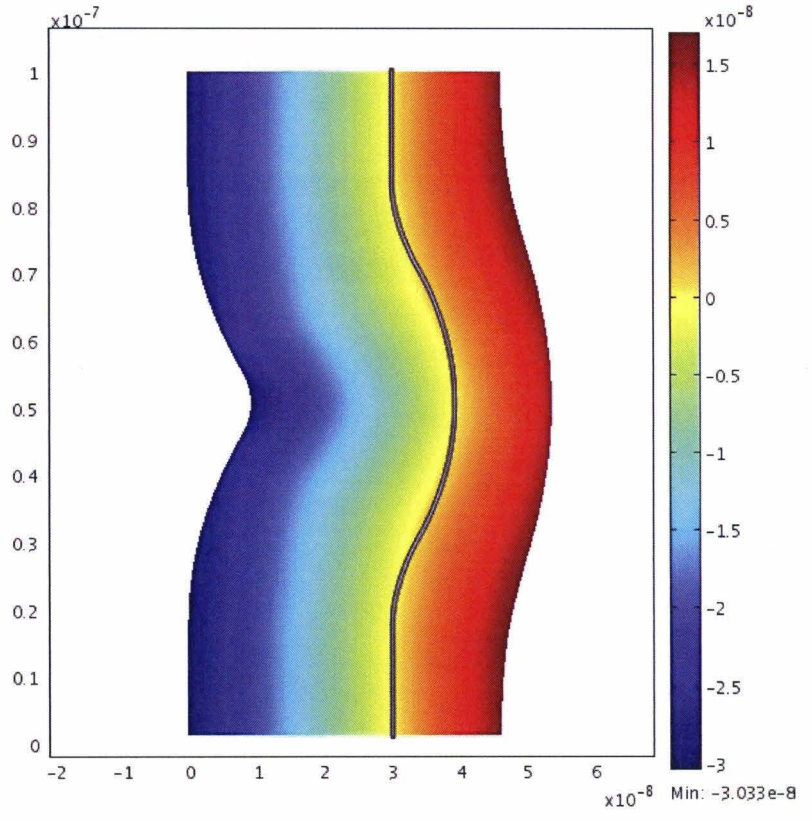


Figure 2.4: Oxidation simulation results of a lump in the pillar. Clearly visible are several distinct features: the pinching off of the central bump into a more confined space and the overall flattening of the outer oxide profile. The overlaid image shows the initial thin oxide shell. The colormap shows the distance of the grown oxide from the starting oxide. The dimensions are given in meters.

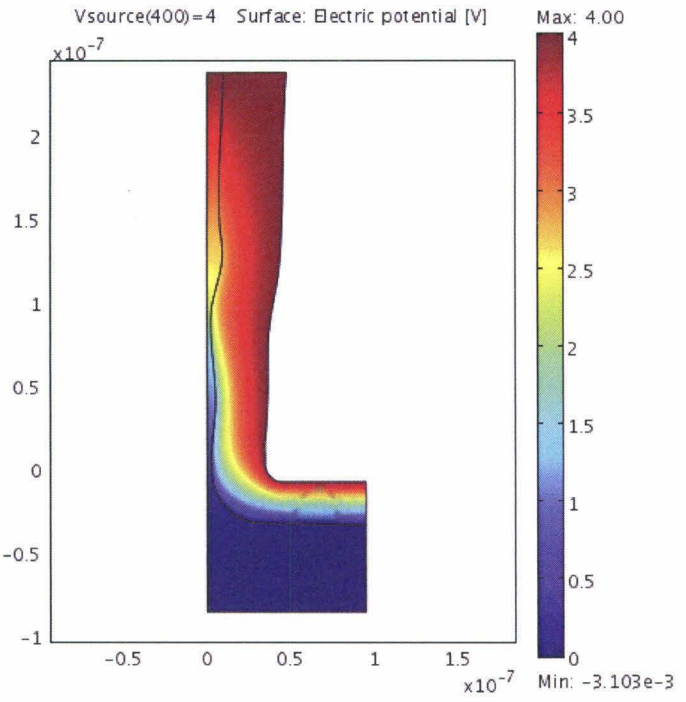


Figure 2.5: Digitized and simulated pillar taken from TEM of figure 2.1(b). The colormap shows voltage and the cross section is in cylindrical coordinates. Voltage is applied uniformly on the outer surface just as in a real Coulomb blockade device.

mensional toy models were developed and used to study the "first-order" effects of variations and constrictions in the device. A full three-dimensional model in cylindrical coordinates was built which used a coupled-mode space approach in order to simplify computational complexity.

Using effective mass and band gap data derived from tight-binding simulations and taking size dimensions from TEMs of oxidized structures, results were compared to theoretical structures which showed large resonant tunneling effects. The mesh was discretized as small as 0.2 nm and solved. Plots shown are IV curves for devices, as in figure 2.7.

In order to realistically simulate transport through small constrictions, a coupled-mode space approach was used. In this approach, the current flows in the z direction,

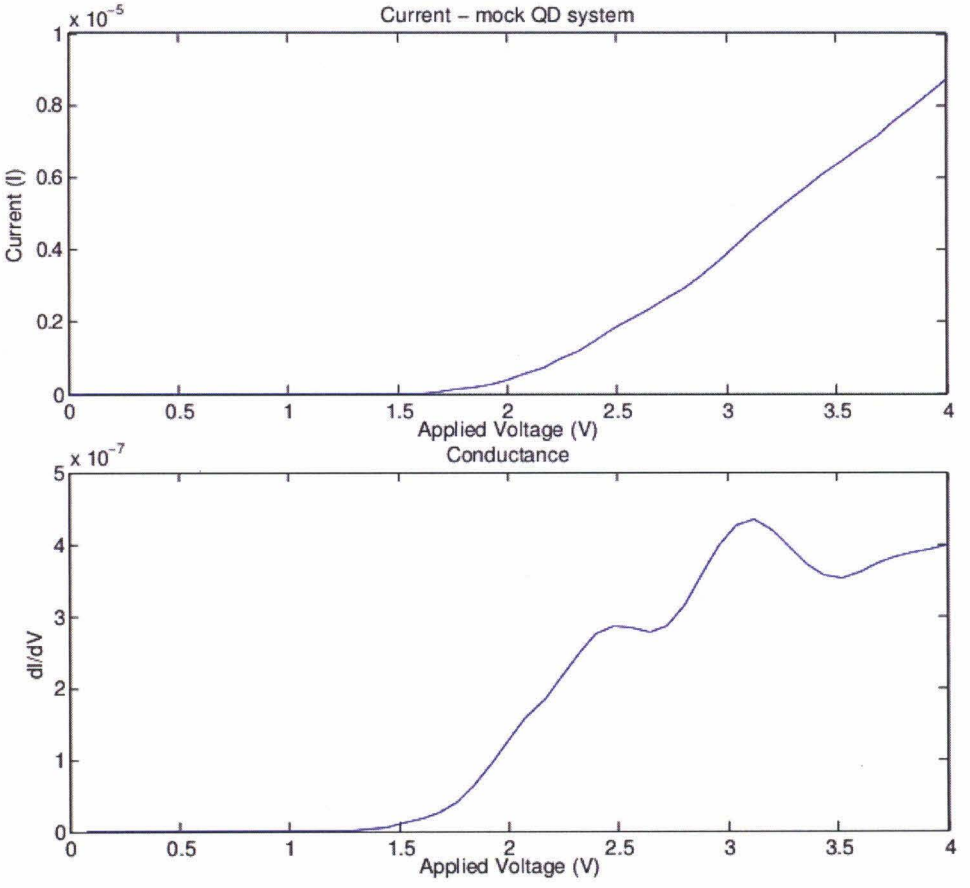


Figure 2.6: Current-voltage and conductance curves for pillar shown in figure 2.5. Although there are some slight nonlinearities in the conductance, the effects of a double tunnel junction on a classical picture of transport are negligible.

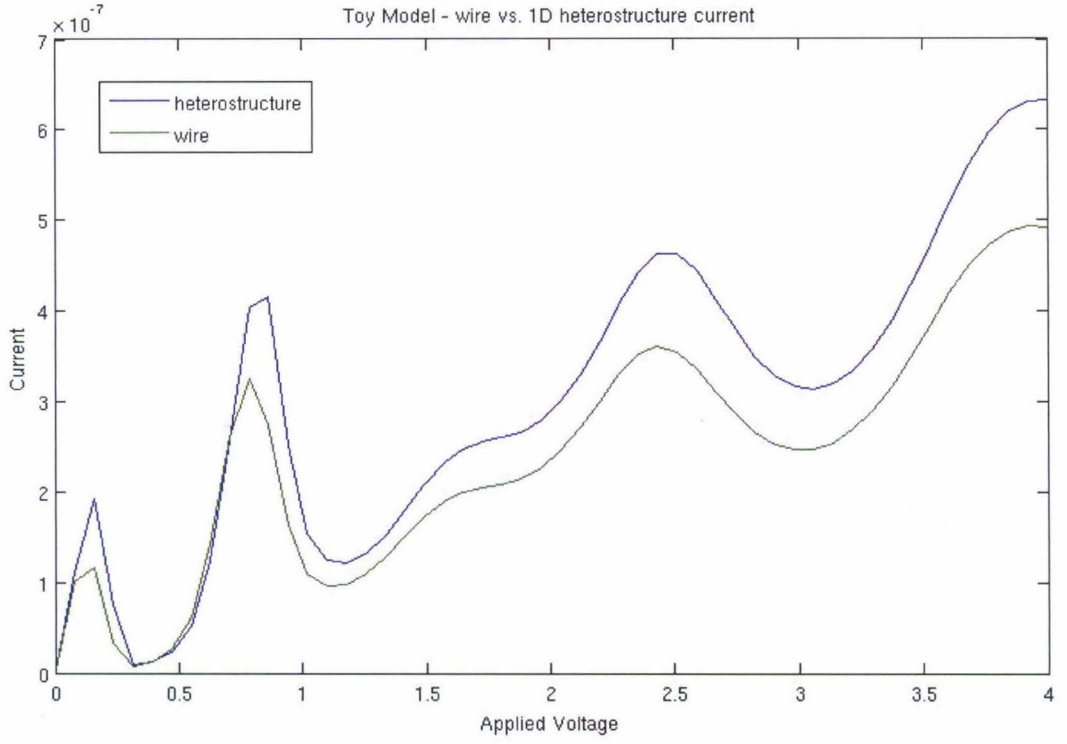


Figure 2.7: One-dimensional toy models in NEGF showing the difference in IV plots between effectively one dimensional structures such as heterostructures and structures such as nanopillars. The negative differential resistance regions are characteristic of resonant tunneling effects.

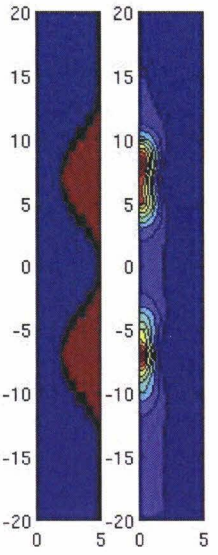


Figure 2.8: Full three dimensional self-consistent NEGF calculations for toy nanopillars. The left image shows the distribution of silicon and silicon dioxide (blue being silicon), while the right image shows carrier density for an applied voltage.

while the x-y direction is discretized. At each point in z direction, the corresponding x-y plane is solved for its eigenmodes and eigenvalues. Then, the Hamiltonian is transformed into this mode-space basis where only the first few low-energy modes are kept. This greatly reduces computation time[22, 18]. This is done by solving for the eigenfunctions in the x-y plane at each point in the z direction. This gives a wavefunction as a function of radial coordinate. The mode Hamiltonian is given as

$$H_{\text{mode}} = U^{\dagger} H U \tag{2.7}$$

Where $U$ is constructed from the eigenfunctions and is truncated at mode $N_m$. This change of basis then ignores modes of energy higher than $N_m$ which in principle may be unimportant for transport.

Figure 2.8 shows the carrier density of a simulated device. Due to real imperfec-

tions, this model does not encapsulate all of the considerations that go into calculating transport.

# Chapter 3

# Results

## 3.1 Effect of Annealing on Device Performance

Using the RTA, Coulomb blockade devices of varying initial radius were treated with a quick annealing step. Annealing is used to obtain good electrical contact between source/drain and device. In this process, titanium is driven into the silicon to form a silicide and establishing conductivity over any native oxide layer that may have formed during processing. A key consideration was to balance anneal times and rates, as it is well-known that gold under rapidly changing thermal environments reflows and may reshape itself. This was mitigated by depositing a thick layer of gold. Figure 3.1 compares behavior of two devices annealed at different temperatures.

Measurements were carried out with a computer controlled voltage supply and pico-ammeter. Each data point was polled several times and the mean value and variance of the measured current was kept. Figure 3.2 shows the current-voltage measured for the pillar in 2.1(a) at both room and cryogenic temperatures. The data at cryogenic temperatures is markedly different than that at room temperature due to reduction of carriers. The results obtained agreed well with Cui *et al.*[2] Further

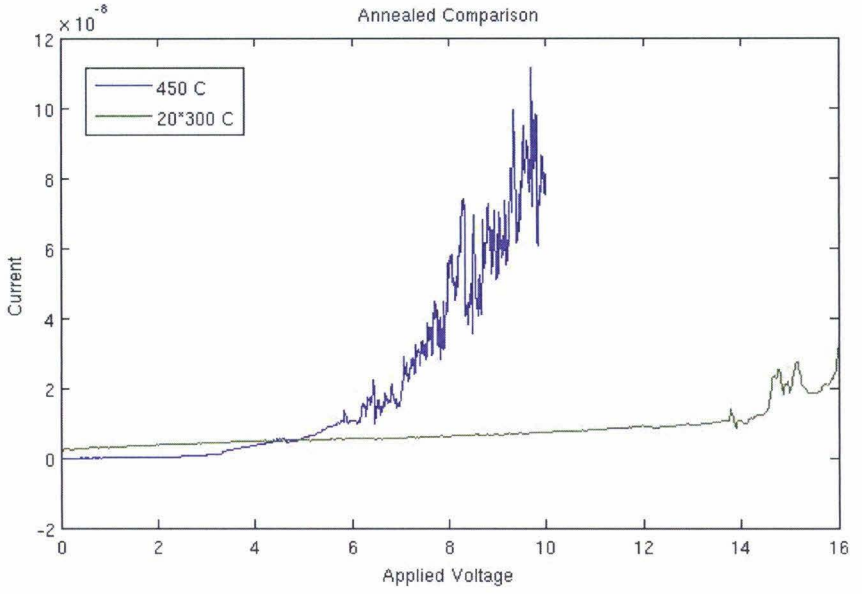


Figure 3.1: Results of different anneal temperatures on performance of nanopillar devices. The anneal at 450 °C shows significant improvement in performance. Note the 300 °C data is scaled by a factor of 30. The noise in this data set is due to sampling only a few points per voltage step.

tests used an anneal temperature of 450 °C.

## 3.2 Demonstration of Coulomb Blockade

Devices tested from the smallest initial pillar diameter performed with characteristics of Coulomb blockade. The differential conductance of the cooled sample, shown in figure 3.3 and computed from I-V measurements, displays multiple periodic peaks indicating regular jumps in conductance. At room temperature however, these features disappear and the device shows the exponential current/voltage behavior of a single tunnel junction.

The measured behavior of the device at cryogenic temperatures is demonstrative of an asymmetric double tunnel junction[7]. In this case the capacitance, or 'trans-

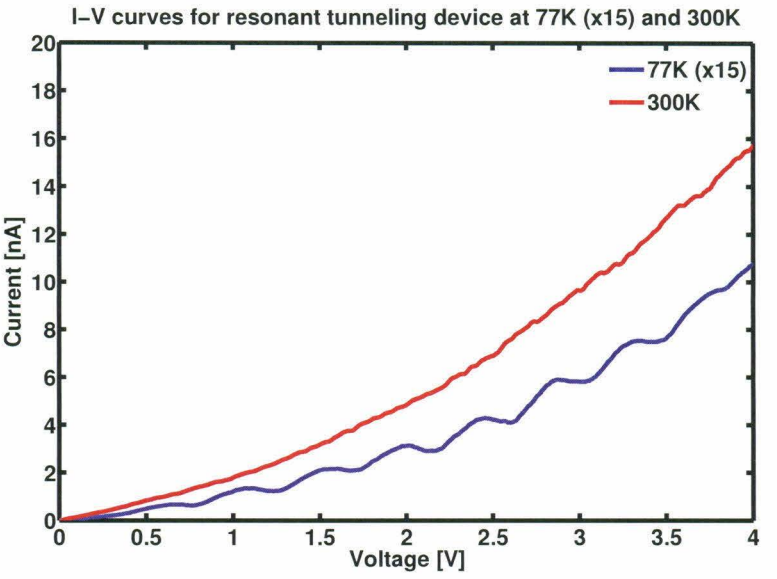


Figure 3.2: Measured I-V plot of a double tunnel junction device at 300K and 77K. Note that the 77K data is scaled by a factor of 15. Clear steps can be seen in the low-temperature measurement.

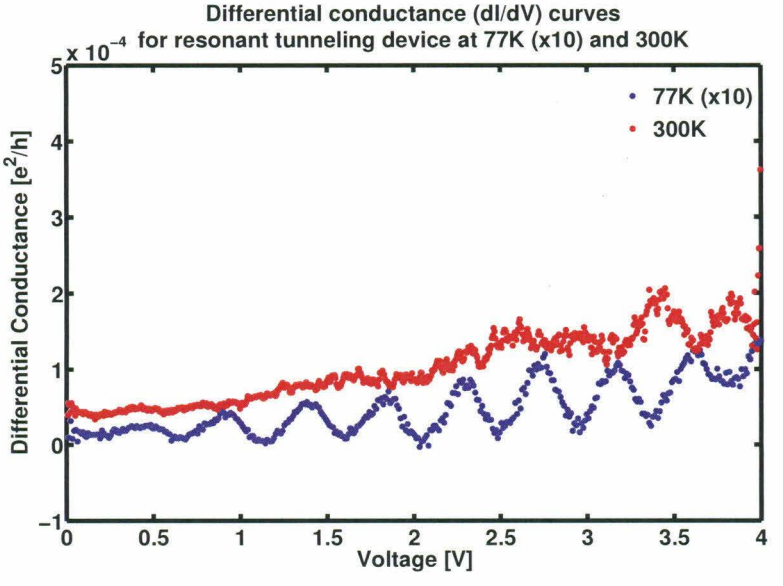


Figure 3.3: Differential conductance of a double tunnel junction device at 300K and 77K. Plot was numerically computed from measured I-V data. Note that the 77K data is scaled by a factor of 10. Periodic peaks can be seen with a spacing of 0.452V.

parency,' of one of the junctions is significantly smaller than the other, schematically shown in figure 3.4(a).

In our case, for a small forward bias, the first tunnel barrier is easily surpassed and the island is populated with an integer number of charges(figure 3.4(a)). The low transparency of the second barrier keeps the electrons trapped, and the electrostatic repulsion between electrons prevents the island from accumulating more charge. The tunneling coefficient of the opaque barrier, which determines the current allowed through the device, is a function of both the forward bias and the number of charges on the island. The approximate functional dependence can be written as $I_{tunneling} \sim I_o(V_a, n) \times \exp(\frac{\alpha V_a}{k_B T})$ where $\alpha$ contains the geometry of the barrier. As the applied voltage is increased, the tunneling rate through the opaque barrier increases but the fixed number of electrons allowed on the island forces the current to remain constant. When the forward bias reaches a large enough value, the electrostatic repulsion can be overcome and an additional electron is forced onto the island(figure 3.4(b)). While the new charge increases the electrostatic repulsion of the island, it is equally negated by the applied voltage; so the voltage increase required to add subsequent electrons remains constant.

When the device was measured at room temperature the lack of distinct current steps can be attributed to the addition of thermal noise. The effect of thermal broadening on the distribution of electron energy is to provide a background charge density on the island great enough to effectively remove it from isolation by shorting the more transparent tunnel junction[7]. The resultant structure behaves as a single

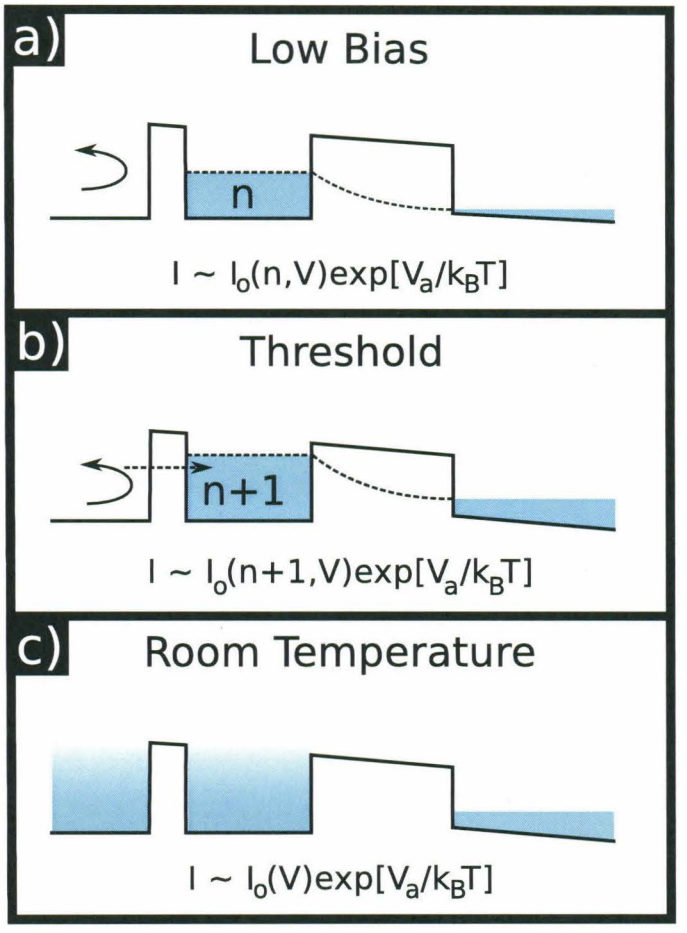


Figure 3.4: Schematic illustrating the behavior of asymmetric double tunnel junction diode under different bias and temperature conditions. (a) At low bias the island is populated and charged to saturation. Little charge can tunnel across the opaque barrier. (b) At a higher forward bias extra electrons can be forced into the island against the electrostatic repulsion of existing charges. The increased number of electrons allows for a greater amount of current to flow through the opaque barrier. (c) At room temperature the thermal fluctuations remove the island from isolation effectively creating a single tunnel junction device.

rectangular tunnel barrier(schematically shown in 3.4(c)), displaying the characteristic exponential behavior where $I \sim \exp\left(\frac{\alpha V_{fwd}}{kT}\right)$ in which the $\alpha$ prefactor contains the relevant geometry of the barrier. At small voltages ($V_{fwd} < 1V$) some small peaks in conductance can be seen(the red plot in figure 3.3) but this behavior seems to be rapidly swamped by the noise introduced at higher voltages. Careful measurements made with greater precision will be done in the future to quantify the possible presence of Coulomb blockade effects at room temperature. The oscillations present in the differential conductance at larger voltages are likely a result of high-energy injection effects and not from a blockading effect.

## 3.3 Further Work

It is important to note that the 'semi-classical' treatment of this device does not include secondary effects such as the charge dependent modification of the bandstructure or strain effects. We can see hints of the influence of one of these phenomena as the small decrease in current present after each 'step' in the I-V plot in figure 3.2. (This corresponds to a negative differential conductance in figure 3.3.) The origin of the dip in current is believed to come from the build-up of electrons at the interface of the opaque junction. This collection of charges opposes the tunneling of electrons, dropping the magnitude of the current. Careful study of this behavior is required to quantify this effect and can be done by either cooling the sample to liquid helium temperatures or creating a device with a greater asymmetry in junction transparency. Future studies will also explore methods to quench the collection of fractional charge

on the island. This charge can be measured by examining the I-V curve for asymmetries across zero applied voltage[17]. It is hoped that the elimination of this excess charge will help to push the Coulomb blockade behavior to higher temperatures.

Although many gated structures have been fabricated, the increased difficulty of doing so has made success fleeting. Some devices have shown transistor-like behavior, but due to imperfections none have shown the classical Coulomb diamond effect. After finally pinning the process down, it is expected that such gated devices will soon be observed. Once a single electron transistor is achieved, more exotic devices may be tested. Previous groups have shown low-temperature single electron logic gates[9] and the potential for spintronic applications[19].

## 3.4 Conclusion

This thesis summarizes the work done towards the fabrication, modeling, and theoretical understanding of single electron devices created from bandgap engineered silicon nanopillars. Etching dependent geometric modification of the silicon bandstructure was used to create an asymmetric, double tunnel junction energy landscape. Measurements taken at liquid nitrogen temperature show clear Coulomb blockade effects and quantum conductance oscillations. Further research will focus on gating such structures and creating sharper deviations in the etch profile with the aim of bringing the Coulomb blockade behavior into the room temperature regime and creating single electron transistors.

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