S1

Spacer #2

Spacer_number_2

S2

Spacer #2

Spacer_number_2

S3

Spacer #2

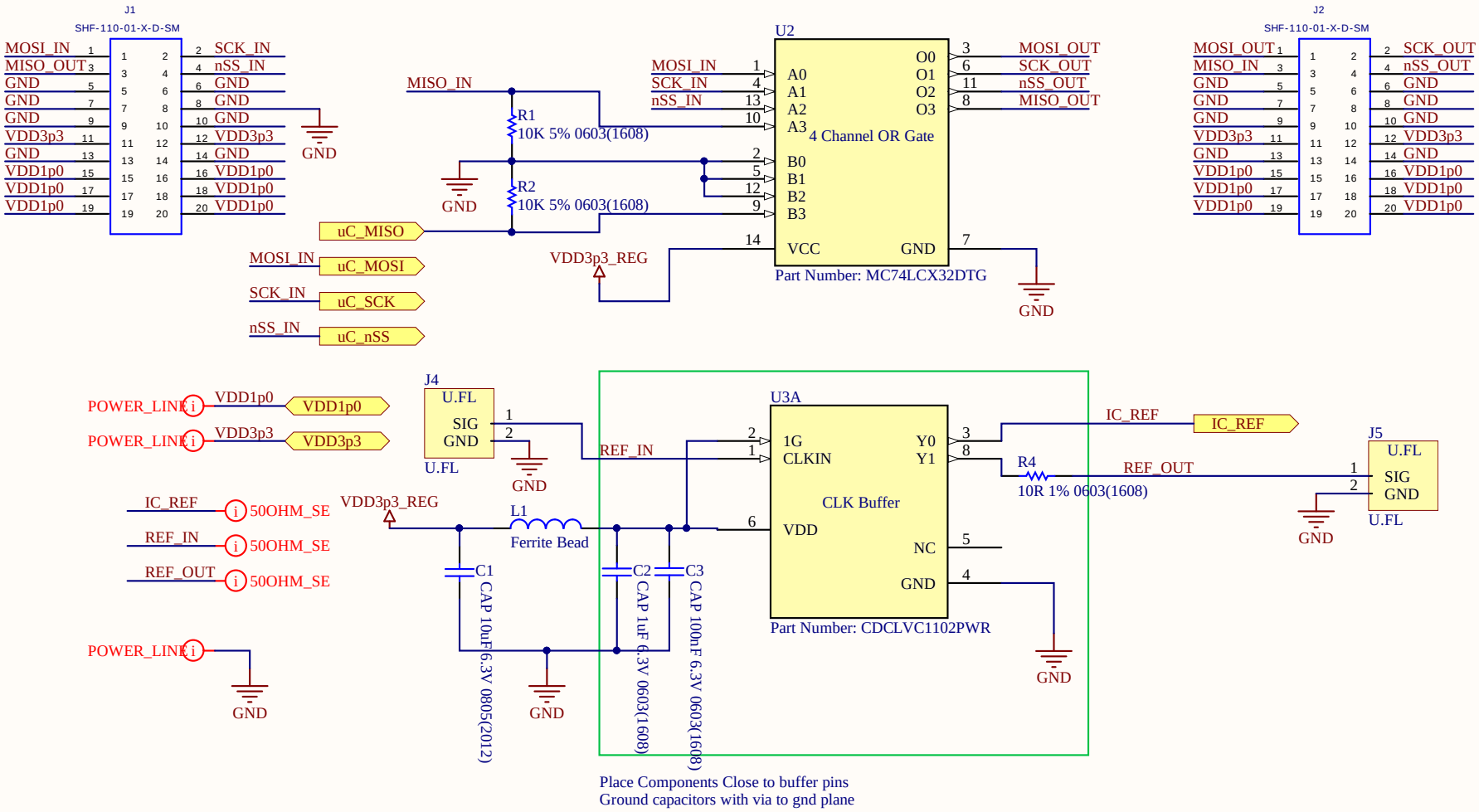
Spacer_number_2

S4

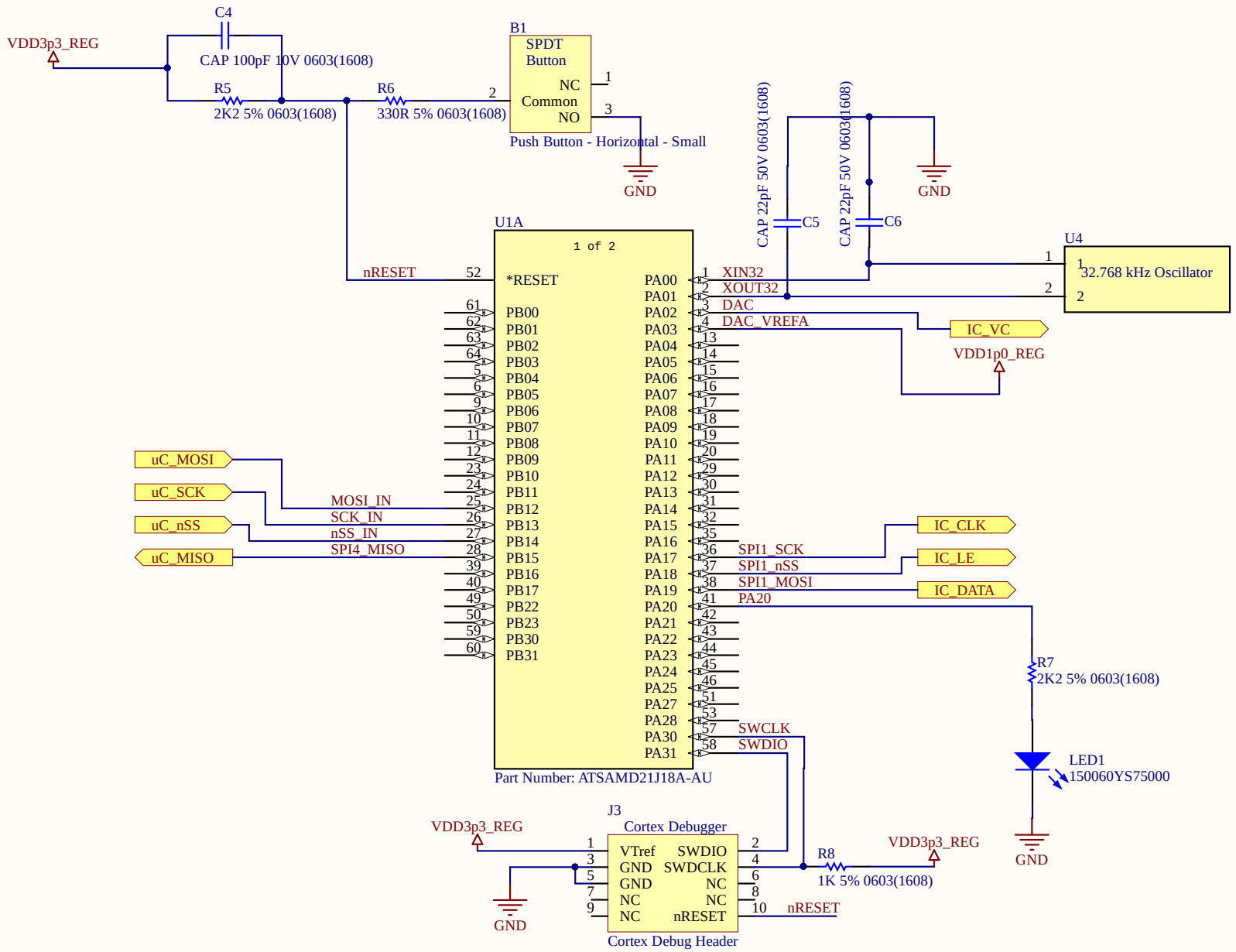
Spacer #2

Spacer_number_2

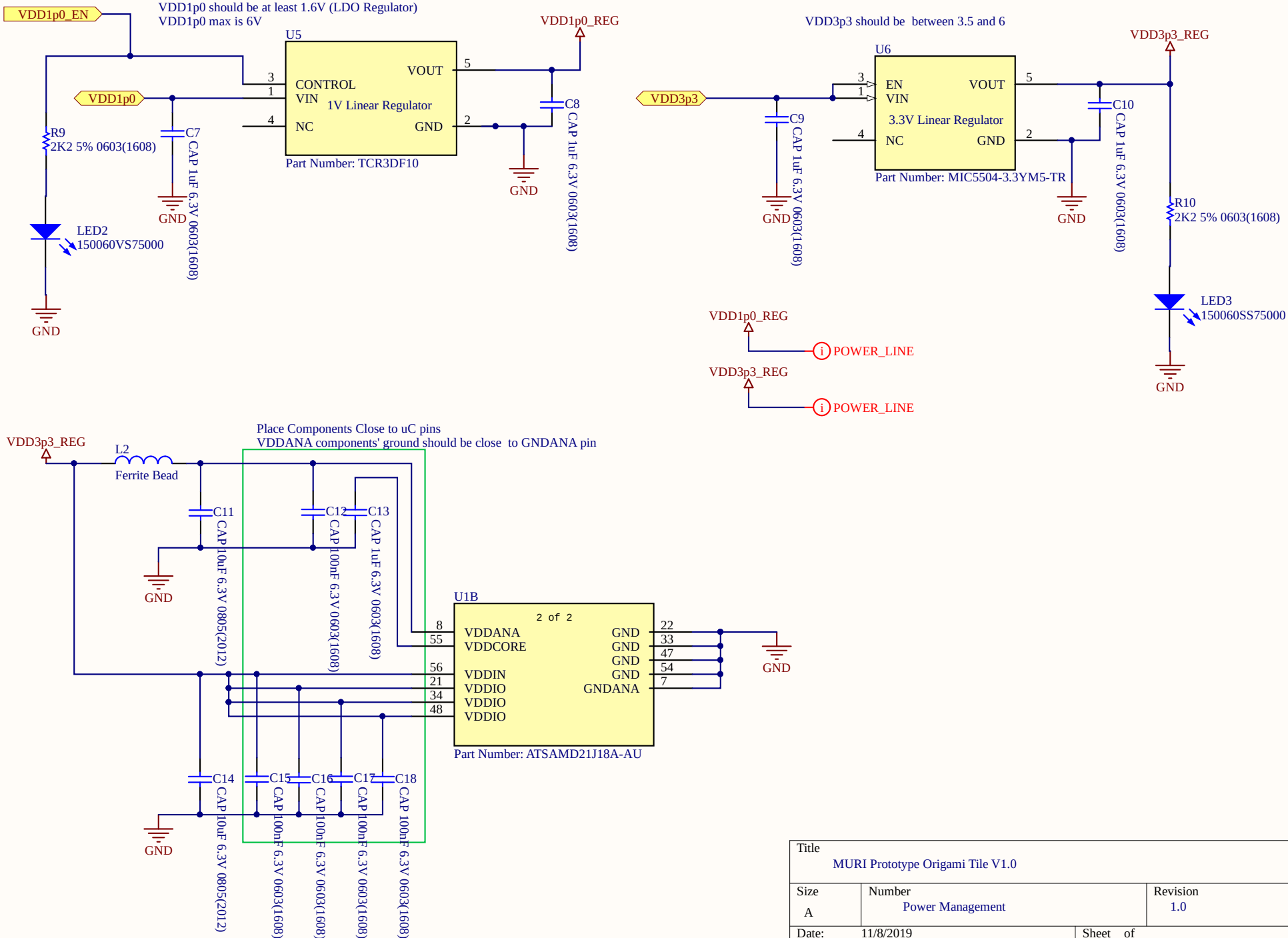
Title: MURI Prototype Origami Tile V1.0		
Size: A	Number: Hardware	Revision: 1.0
Date: 11/8/2019		Sheet of
File: D:\Designs\..\Hardware.SchDoc		Drawn By: Elliott Williams

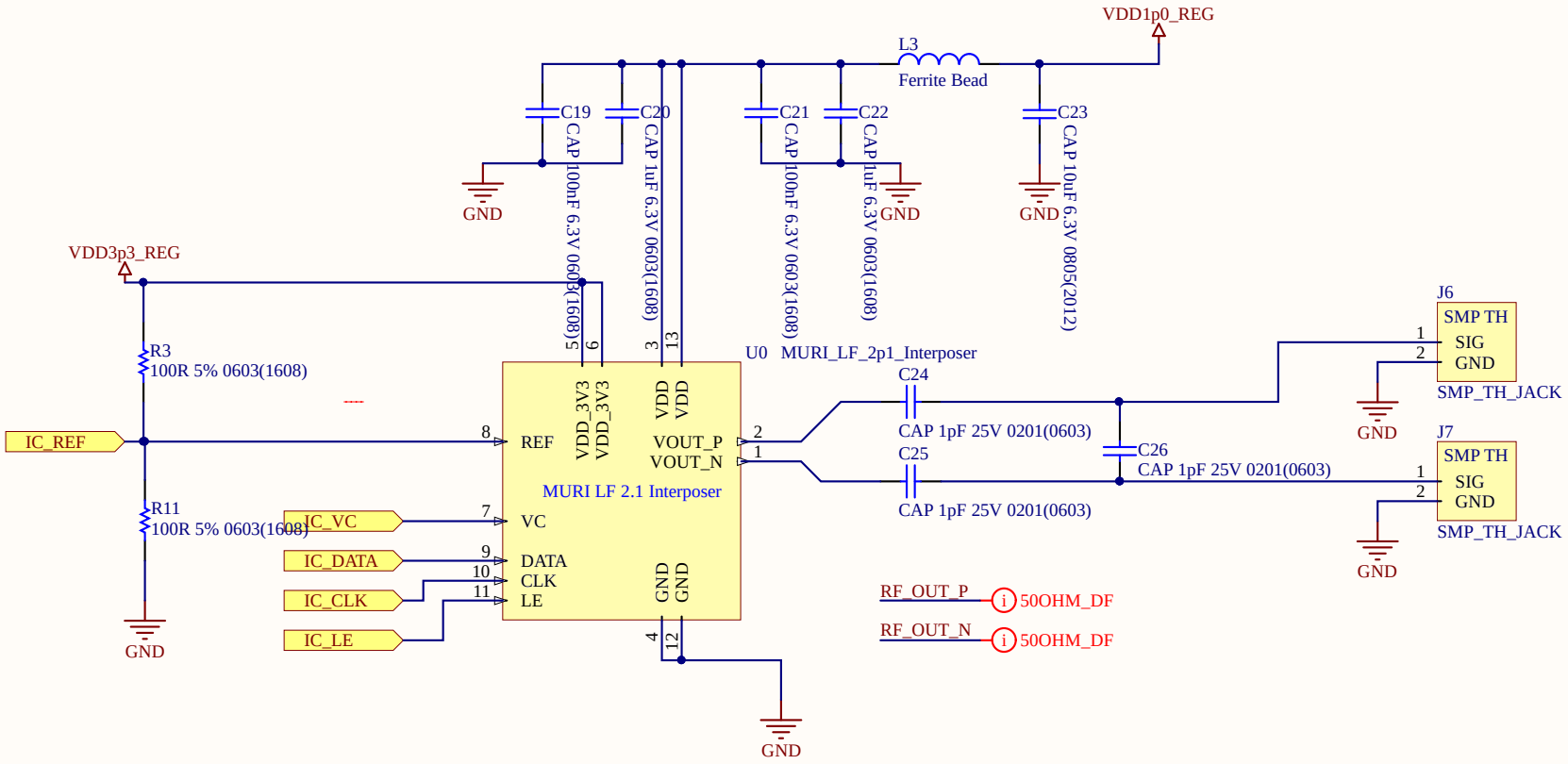


Title: MURI Prototype Origami Tile V1.0		
Size: A	Number: Interconnect	Revision: 1.0
Date: 11/8/2019		Sheet of
File: D:\Designs\..\Interconnect.SchDoc		Drawn By: Elliott Williams



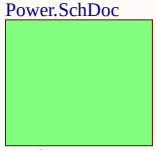
Title	MURI Prototype Origami Tile V1.0	
Size: A	Number: Microcontroller	Revision: 1.0
Date: 11/8/2019		Sheet of
File: D:\Designs\..\MCU.SchDoc		Drawn By: Elliott Williams


VDD1p0_EN
VDD1p0 should be at least 1.6V (LDO Regulator)
VDD1p0 max is 6V
U5
VDD1p0_REG
CONTROL
VIN
NC
VOUT
GND
1V Linear Regulator
Part Number: TCR3DF10
VDD1p0
R9
2K2 5% 0603(1608)
C7
CAP 1uF 6.3V 0603(1608)
C8
CAP 1uF 6.3V 0603(1608)
LED2
150060VS75000
GND
VDD3p3 should be between 3.5 and 6
U6
VDD3p3_REG
EN
VIN
VOUT
NC
GND
3.3V Linear Regulator
Part Number: MIC5504-3.3YM5-TR
VDD3p3
C9
CAP 1uF 6.3V 0603(1608)
C10
CAP 1uF 6.3V 0603(1608)
R10
2K2 5% 0603(1608)
LED3
150060SS75000
VDD1p0_REG
POWER_LINE
VDD3p3_REG
POWER_LINE
Place Components Close to uC pins
VDDANA components' ground should be close to GNDANA pin
L2
Ferrite Bead
C11
CAP 10uF 6.3V 0805(2012)
C12
CAP 100nF 6.3V 0603(1608)
C13
CAP 1uF 6.3V 0603(1608)
U1B
2 of 2
VDDANA
VDDCORE
VDDIN
VDDIO
VDDIO
VDDIO
GND
GNDANA
Part Number: ATSAMD21J18A-AU
C14
CAP 10uF 6.3V 0805(2012)
C15
CAP 100nF 6.3V 0603(1608)
C16
CAP 100nF 6.3V 0603(1608)
C17
CAP 100nF 6.3V 0603(1608)
C18
CAP 100nF 6.3V 0603(1608)
Title
MURI Prototype Origami Tile V1.0
Size
A
Number
Power Management
Revision
1.0
Date:
11/8/2019
Sheet of
File:
D:\Designs\..\Power.SchDoc
Drawn By:
Elliott Williams

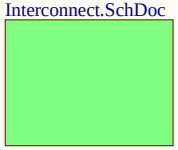


Title: MURI Prototype Origami Tile V1.0		
Size: A	Number: RF	Revision: 1.0
Date: 11/8/2019		Sheet of
File: D:\Designs\..\RF.SchDoc		Drawn By: Elliott Williams

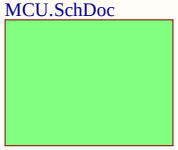
Power
Power.SchDoc



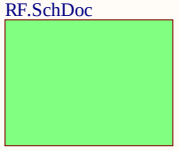
Interconnect
Interconnect.SchDoc



Microcontroller
MCU.SchDoc

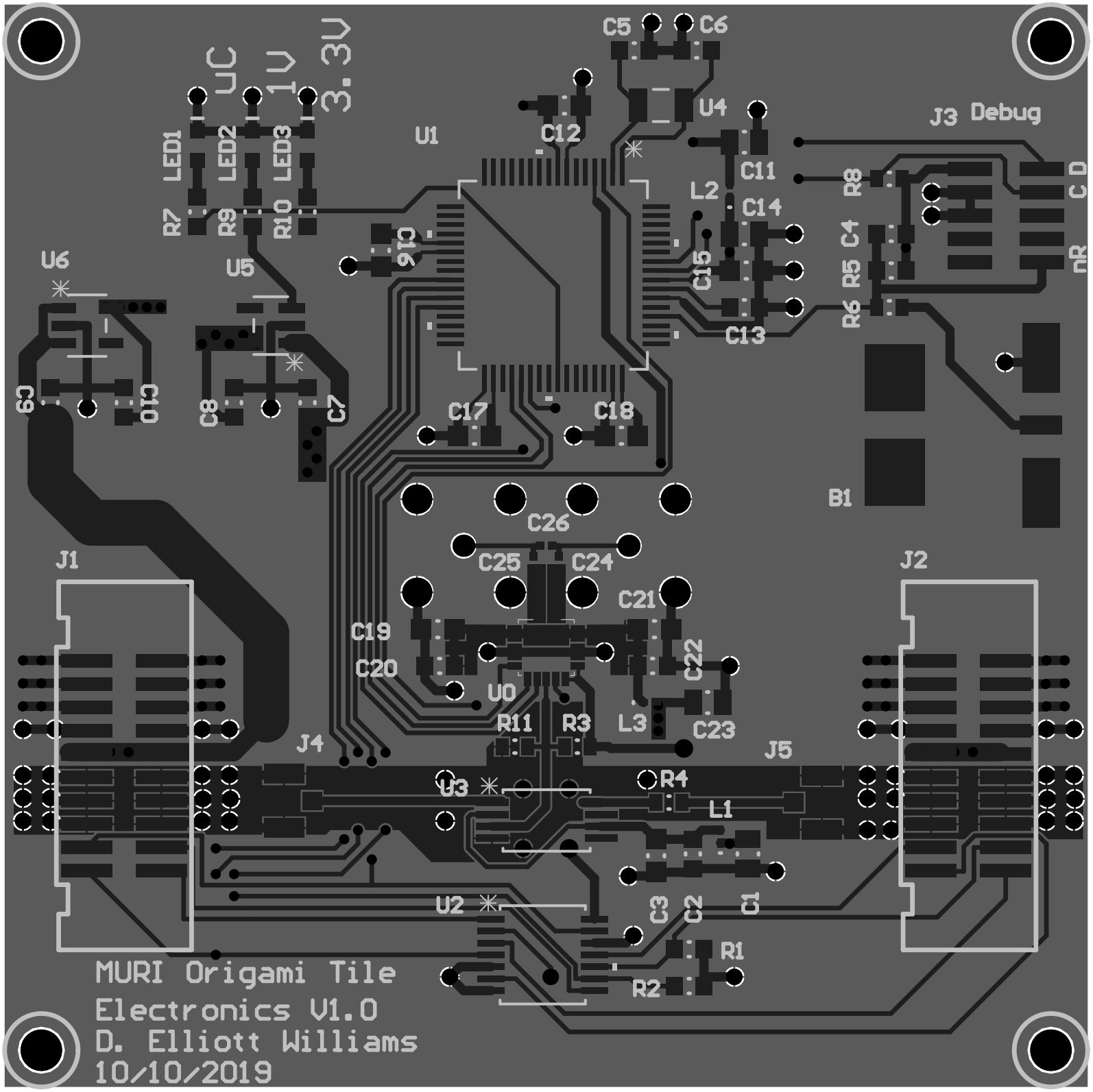


RF
RF.SchDoc



Hardware
Hardware.SchDoc

Title			
Size A	Number		Revision
Date:	11/8/2019	Sheet of	
File:	D:\Designs\..\TOP_Origami_Tile_Split_Electronics.SchDoc	Drawn By:	


uC
1V
3.3V
LED1
LED2
LED3
R7
R9
R10
U1
U4
U5
U6
C5
C6
C12
C11
L2
C14
C15
C13
C16
J3 Debug
R8
C4
R5
R6
C9
C10
C8
C7
C17
C18
B1
C26
C25
C24
C21
J1
J2
C19
C20
C22
U0
R11
R3
L3
C23
J4
J5
U3
R4
L1
U2
C3
C2
C1
R1
R2
MURI Origami Tile
Electronics V1.0
D. Elliott Williams
10/10/2019