Analysis of Single Phase Rectifier Circuits

Thesis by
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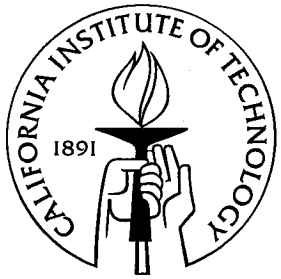
In Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy



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to my family

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Every graduate of the Power Electronics Group is indebted to his (her) predecessors, each of whom has sacrificed part of himself (herself) to contribute to the body of knowledge representative of the Power Electronics Group.

Abstract

The preponderant application of rectifier circuits is the powering of dc loads from the ac utility line. Ordinary rectifier circuits present a nonlinear load impedance to the utility line, thereby generating harmonic currents, and contributing to the harmonic current problem. There are many active and passive rectifier circuits offering reduced harmonic currents, and in this work a methodology is developed by which these circuits may be analyzed and compared.

Rectifier circuits can be classified as either active or passive. A passive rectifier circuit contains passive components (inductors, capacitors, saturable reactors, etc.), and passive switches (rectifier diodes) only. Active rectifier circuits use at least one controllable active switch (power transistor), in addition to passive switches and passive components. The performance characteristics of these circuits can be assessed with respect to a fictional device called the ideal rectifier. This assessment allows direct comparison of various approaches, passive or active, using the ideal rectifier as the common reference. Rectifier circuit performance may also be compared against specified requirements.

The next topic considered is the analysis of active rectifier circuits employing a pwm (pulse width modulation) converter as a means to control power flow within the rectifier circuit. The pwm converter is modeled using the pwm switch method. A large-signal nonlinear pwm switch model is used for modeling large-signal rectifier circuit behavior, and models are developed for operation in either the continuous or discontinuous conduction mode. Similarly, a small-signal model is developed for small-signal considerations. In addition, for pwm converters operating in the continuous conduction mode, the effect of lossy resistive elements inside the converter are accounted for in the

pwm switch model, and this modeling technique is shown to give results identical to those obtained via the state-space averaging method.

The methods developed are then applied to the analysis of the boost rectifier operating in the discontinuous conduction mode. Three control schemes are compared, each offering a different compromise between circuit complexity and performance. Finally, a design example is given, and experimental results are provided.

Contents

Chapter 1

Introduction

Electrical power conversion systems process electric power at the system input into a desired form at the system output. There are two basic types of electrical power, namely ac and dc, which implies that that there are four basic power conversion processes. These processes have been given the names dc/dc conversion, dc/ac inversion, ac/dc rectification, and ac/ac cycloconversion. The systems that perform these processes are similarly named dc/dc converters, dc/ac inverters, ac/dc rectifiers, and ac/ac cycloconverters. This thesis is concerned primarily with the process of ac/dc rectification, specifically as it pertains to single phase ac/dc rectifier circuits. Although the primary focus is on ac/dc rectification, because a dc/dc converter is at the heart of many ac/dc rectifier systems, much attention is given to the analysis of dc/dc converters, and then further extended to the ac/dc rectification problem. The omnipresence of ac power sources and dc loads, and the desire to connect them, makes this study an important one.

Ideally, the electrical utility system provides low frequency ac power to the electric power consumer via a fixed frequency, fixed amplitude, sinusoidal voltage waveform. The electric power consumer then connects loads, some linear, some nonlinear, to the utility line to perform some desired task. However, the connection of nonlinear loads drawing non-sinusoidal current, combined with the non-zero source impedance of the utility line, causes distortion of the line voltage waveform. Further, this distortion is presented not only to the offending load, but to non-offending loads and consumers as well. In addition, the utility provider is asked to provide the non-sinusoidal current, through a utility grid which must be designed to carry the extra burden.

This scenario raises the issue of power quality, which is the primary motivation for studying the ac/dc rectification problem. The subject of power quality is concerned with the degree to which the electrical utility provides stable, reliable, zero distortion and disturbance-free voltage. Because many ac/dc rectifier circuits present a nonlinear load to the utility, they influence power quality by inducing distortion of the utility line voltage, and lower the power delivery system reliability through the circulation of non-sinusoidal current. While the influence of any one load, however small, on the utility line may seem insignificant, it is the net effect of all such loads that causes difficulty. The proliferation of personal computers as part of the information age is a particularly troublesome example.

In chapter 2, a quantitative measure of the effectiveness of electric power transfer, called the circuit power factor, is defined in general. Like most general definitions, however, it is difficult to draw many conclusions and obtain useful results without first making assumptions. To this end, the general case is quickly abandoned for the specific case of ideal sinusoidal utility line voltage. Although the actual voltage measured at the load operating on the utility line will never be an ideal sinusoid, this assumption leads to simple, intuitive results and provides a basis by which various rectifier circuits may be compared. Besides, an ideal sinusoid is certainly a reasonable approximation to what is actually measured at the terminals of a typical wall outlet. The effect of non-sinusoidal voltage components present on the utility line can be considered separately.

Also in chapter 2 is a general discussion of the terminal behavior of the constant power load. The constant power load is used many times throughout this thesis as a simple means of modeling the loading effect of a switching post-regulator as part of a complete ac/dc rectifier system. It is shown that this type of load exhibits the large-signal character of a positive resistance, and the small-signal character of a negative resistance. For this reason, modeling the loading effect of a switching regulator simply as an equivalent resistor can lead to incorrect results.

In chapter 3, the results developed in chapter 2 are applied to the analysis of passive rectifier circuits. In each case, it is assumed that the passive rectifier circuit is to be followed by a switching post-regulator, and the constant power load is therefore used to

emulate its loading effect. Passive rectifier circuits offer the advantages of simplicity and durability over active approaches, but are generally bulky and heavy as compared to their active counterparts. For high frequency input power sources, these disadvantages are less apparent, but for low frequency utility line applications, the size and weight of passive components are often prohibitive. The results contained in this chapter can be applied to make this determination, based on the specific performance requirements. The performance characteristics of each passive rectifier circuit are presented graphically, and can be compared directly against characteristics of other rectifier circuits, and also against the actual performance requirements.

The necessity for a single phase rectifier circuit to store energy is examined in chapter 4. Under the assumptions of unity input power factor and constant output power, the energy stored in the rectifier circuit is determined to within a constant. The minimum stored energy necessary for load balancing is determined, and this places a fundamental limitation on the design of these systems.

The remainder of this thesis considers ac/dc rectifier circuits incorporating pwm (pulse width modulation) dc/dc converters acting as the power processing interface between the ac input and dc output. To simplify matters, the pwm switch concept is considered in chapters 5 and 6, where several conceptually new pwm switch models are introduced. The pwm switch is a simplified circuit-oriented analysis method which confines the nonlinearity inherent in the switching process to the transistor and diode switches themselves. Pwm switches for converters operating in the continuous conduction mode are taken up in chapter 5, followed by pwm switches for converters in the discontinuous conduction mode in chapter 6. Although pwm switches are derived based on converter operation in a dc/dc system, they can be used for the analysis of ac/dc rectifier circuits under certain conditions.

The determination of the boundary between the continuous and discontinuous conduction modes is considered in chapter 7. In dc/dc converter applications, this boundary is a static one, since the operating point is fixed. In contrast, in ac/dc rectifier applications, the boundary changes continuously since the converter operating point varies throughout the line period. The converter can, however, be designed to maintain

a particular conduction mode over the entire line period, by ensuring that the boundary is not crossed at any point. It is usually desired for the converter in a rectifier circuit to operate exclusively in a single operating mode because the control system designed for operation in one mode may not be suitable for operation in another.

Finally, many of the ideas developed in the previous chapters are put to use in chapter 8, which is devoted entirely to analysis and design of the boost rectifier operating in the discontinuous conduction mode. The boost converter remains the converter of choice in ac/dc rectifier circuits for two main reasons. The first is that it is capable of voltage step-up, and therefore operates down to zero input voltage, through the zero crossings of the utility line. The second is that the boost is a partial power processing converter, where the switches process only part of the total output power. Hence, part of the input power passes directly to the output without being processed, and therefore without the associated power loss. This property makes the boost converter extremely efficient when compared to total power processing converters, such as the buck-boost, or any of the buck-boost type converters (cuk, sepic, zeta, etc.). One drawback of the boost converter which is a consequence this partial power processing property, is that it cannot directly provide galvanic isolation. However, in a complete rectifier system, a secondary post-regulator is usually added to provide precise regulation of the dc output voltage and to provide multiple dc outputs, and this regulator can employ a converter which is easily isolated. A second drawback is that the output voltage of the boost converter must be greater than the input voltage, since it is capable only of voltage step-up (hence, its name). In an ac/dc rectifier application, this requirement implies that the output voltage must be greater than the peak input voltage, which may be higher than desired. However, excellent performance is demonstrated with the peak conversion ratio approaching unity.

Chapter 2

Power Factor and the Ideal Rectifier

In this chapter, the basic definitions are set forth which quantify the quality with which a load processes power delivered from an ac power source. Power factor is a concept familiar to most engineers, but is often understood only at a rudimentary level. In section 2.1, the general time-domain definition of power factor is given. Next, the frequency-domain interpretation of power factor is discussed, for the specific case of ideal sinusoidal input voltage. Using a Fourier series expansion of the input current waveform, it is shown that the power factor may be written as the product of two factors, one called the distortion factor, and the other called the displacement factor. The distortion factor is concerned with the current harmonics flowing in the circuit, and the displacement factor with the phase of the fundamental component of the input current relative to the input voltage. The power factor is a compact way of quantifying the effect of both of these factors, although in practice it is often necessary to consider the two factors separately.

In section 2.2, the ideal rectifier circuit is defined. The ideal rectifier, like most idealizations, is unrealizable, but provides a theoretical reference against which real rectifier circuit performance can be assessed. The ideal rectifier is used extensively in this manner throughout this thesis. In section 2.3, the constant power load is discussed. The constant power load is a simple way to model the static and low frequency dynamic behavior of the input to a high performance switching regulator. A high performance switching regulator is often used in a complete ac/dc rectifier system as a secondary regulator, following the high power factor rectifier input stage. In this configuration, the secondary regulator is used to provide fast and precise output voltage regulation, multiple outputs, and also to provide galvanic isolation with respect to the ac input.

2.1 Power Factor

The Power Factor is a measure of the effectiveness with which an ac source transfers power to a load. The power factor ranges between zero and unity, with zero power factor corresponding to completely ineffective power transfer, and unity power factor corresponding to completely effective power transfer. When the power factor is unity, the burden on the power delivery system is minimized, making this mode of operation very desirable.

2.1.1 Definition of Power Factor

Consider the connection of a load, either linear or nonlinear, to a source of ac power, as in figure 2.1. It is assumed that the system is in steady-state, and that the voltage and current waveforms are periodic with the same period. Under these conditions, the power factor is defined, and is given by the ratio

$$PF \equiv \frac{P}{S} \tag{2.1.1}$$

where P is the average power and S is the apparent power delivered to the load. The average power P is the time-average value of the instantaneous power taken over one period

$$P = \frac{1}{T}\int_T v(t)i(t)dt \tag{2.1.2}$$

and is the quantity which would be read by a suitable wattmeter. The apparent power S is the product of the root-mean-square (rms) values of the voltage and current

$$S = V_{rms} I_{rms} \tag{2.1.3}$$

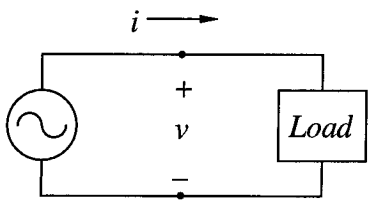


Figure 2.1: Single-phase ac circuit consisting of an ac power source and a load.

where the rms values of the voltage and current are defined by

$$V_{rms} \equiv \sqrt{\frac{1}{T}\int_T v^2(t)dt} \quad ; \quad I_{rms} \equiv \sqrt{\frac{1}{T}\int_T i^2(t)dt} \tag{2.1.4}$$

It is important to note that the power factor is a quantity which is defined for a *circuit*, and not for a *load*. It is therefore incorrect to say that a load exhibits a particular power factor. If identical loads are connected to two different ac sources, the power factor in each of these circuits may be different. One exception is if the load is a linear resistor. In this case, at any instant, the voltage and current are related by

$$v(t) = i(t)R \tag{2.1.5}$$

Substituting this expression into the definition of power factor, we find that the power factor is unity, regardless of the ac source waveform. Thus, proportional current, in general, yields unity power factor. This explains why high power factor rectifier circuits are sometimes referred to as "resistor emulators."

In the analysis of the power factor in ac/dc rectifier circuits, the goal is to determine the power factor of the circuit formed when the input to the rectifier circuit is connected to the ac utility line. Throughout this thesis, for the sake of simplicity, the utility line is modeled by a zero-impedance voltage source. Since the power factor is a circuit quantity which depends on both the ac power source and the load, in order to compare the power factor and performance of different rectifier circuits, the ac power source should of course be the same. The choice of a standard ac power source is obvious, namely an ideal sinusoidal voltage source, and the implications of this choice on the power factor formulation are the subject of the next section.

2.1.2 Frequency-Domain Formulation with an Ideal Sinusoidal Voltage Source

For the purpose of studying the power factor and current harmonics in circuits operating on the ac utility line, it is reasonable to model the utility line as an ideal sinusoidal voltage source. The sinusoidal assumption is invoked because it simplifies the analysis considerably, yielding results which are both accurate and informative. The effect of voltage waveform distortion can be handled separately, and is not considered

here. The purpose here is to develop concepts and methods useful for rectifier circuit design, simple enough that they are easily applied, yet complex enough that the results are accurate. To begin, we define angle θ as the normalized time variable

$$\theta \equiv \omega_l t \tag{2.1.6}$$

where ω_l is the line frequency. The source voltage is, by assumption, sinusoidal, with zero phase shift. We may therefore write

$$v(\theta) = \sqrt{2}\, V_{ideal} \sin\theta \tag{2.1.7}$$

where V_{ideal} is the rms value of the ideal sinusoidal source voltage. The following auxiliary formulas are introduced here because they are useful in the determination of the coefficients in the Fourier series expansion, and also in the derivation of the frequency-domain interpretation of power factor that follows. For any two integers $n, m \neq 0$, we have:

$$\int_{-\pi}^{\pi} \cos n\theta \, d\theta = 0$$

$$\int_{-\pi}^{\pi} \sin n\theta \, d\theta = 0$$

$$\int_{-\pi}^{\pi} \cos n\theta \cos m\theta \, d\theta = \begin{cases} \pi \; ; & n = m \\ 0 \; ; & n \neq m \end{cases}$$

$$\int_{-\pi}^{\pi} \sin n\theta \sin m\theta \, d\theta = \begin{cases} \pi \; ; & n = m \\ 0 \; ; & n \neq m \end{cases} \tag{2.1.8}$$

$$\int_{-\pi}^{\pi} \sin n\theta \cos m\theta \, d\theta = 0$$

$$\int_{-\pi}^{\pi} \sin(n\theta + \phi_n) \sin(m\theta + \phi_m) \, d\theta = \begin{cases} \pi \; ; & n = m \\ 0 \; ; & n \neq m \end{cases}$$

Let the periodic current waveform admit a Fourier series expansion of the form

$$i(\theta) = I_0 + \sum_{n=1}^{\infty} a_n \cos n\theta + b_n \sin n\theta \tag{2.1.9}$$

To determine the Fourier coefficients, first consider the dc term I_0. Integrating both sides of the Fourier series expansion (2.1.9) from $-\pi$ to π, and taking the integral inside the summation, we get

$$\int_{-\pi}^{\pi} i(\theta)\, d\theta = \int_{-\pi}^{\pi} I_0\, d\theta + \sum_{n=1}^{\infty} \left[a_n \int_{-\pi}^{\pi} \cos n\theta\, d\theta + b_n \int_{-\pi}^{\pi} \sin n\theta\, d\theta \right] \tag{2.1.10}$$

From the auxiliary formulas (2.1.8), the integrals inside the summation vanish, leaving only

$$\int_{-\pi}^{\pi} i(\theta)\, d\theta = 2\pi I_0 \tag{2.1.11}$$

which is used to compute I_0. To determine the a_n coefficients, multiply both sides of the Fourier series expansion (2.1.9) by $\cos m\theta$, and then integrate from $-\pi$ to π:

$$\int_{-\pi}^{\pi} i(\theta) \cos m\theta\, d\theta = I_0 \int_{-\pi}^{\pi} \cos m\theta\, d\theta + \sum_{n=1}^{\infty} \left[a_n \int_{-\pi}^{\pi} \cos n\theta \cos m\theta\, d\theta + b_n \int_{-\pi}^{\pi} \sin n\theta \cos m\theta\, d\theta \right] \tag{2.1.12}$$

Referring to the auxiliary formulas (2.1.8), the first integral on the right side vanishes, and the last integral on the right side vanishes as well. The only integral that remains is the one beside a_n, which is nonzero only when $n = m$. Thus, we conclude

$$\int_{-\pi}^{\pi} i(\theta) \cos n\theta\, d\theta = a_n \pi \quad ; \quad n = 1,2,3,\ldots \tag{2.1.13}$$

which is used to compute a_n. Similarly, to find a formula for b_n, multiply both sides of the Fourier series expansion (2.1.9) by $\sin m\theta$, and integrate from $-\pi$ to π. In this case, we find

$$\int_{-\pi}^{\pi} i(\theta)\sin n\theta\, d\theta = b_n\pi \quad ; \quad n = 1,2,3,\ldots \tag{2.1.14}$$

In summary, for a periodic function $i(\theta)$ with period 2π, the Fourier coefficients are given by the formulas

$$\left.\begin{aligned} I_0 &= \frac{1}{2\pi}\int_{-\pi}^{\pi} i(\theta)\, d\theta \\ a_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} i(\theta)\cos n\theta\, d\theta \\ b_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} i(\theta)\sin n\theta\, d\theta \end{aligned}\right\} \; n = 1,2,3,\ldots \tag{2.1.15}$$

To evaluate the power factor, first we find the average power delivered to the load. The average power delivered is the time-average value of the instantaneous power taken over one line period. This gives

$$P = \frac{1}{2\pi}\int_{-\pi}^{\pi} \sqrt{2}\, V_{ideal}\sin\theta\left[I_0 + \sum_{n=1}^{\infty} a_n\cos n\theta + b_n\sin n\theta\right] d\theta \tag{2.1.16}$$

where the current has been replaced by its Fourier series expansion (2.1.9). Bringing the integral inside the summation, we have the somewhat lengthy expression

$$P = \frac{V_{ideal}}{\sqrt{2}\,\pi}\left\{ I_0\int_{-\pi}^{\pi}\sin\theta\, d\theta + \sum_{n=1}^{\infty}\left[a_n\int_{-\pi}^{\pi}\sin\theta\cos n\theta\, d\theta + b_n\int_{-\pi}^{\pi}\sin\theta\sin n\theta\, d\theta\right]\right\} \tag{2.1.17}$$

However, the first integral vanishes, as does the one beside a_n. The last integral vanishes for every n except $n = 1$. Hence, only the b_1 term contributes to the average power delivered, which can now be written simply as

$$P = \frac{b_1}{\sqrt{2}} V_{ideal} \tag{2.1.18}$$

The quantity "$b_1/\sqrt{2}$" has special meaning, and is given the name "ideal current." The reason that this name is chosen will become apparent at the end of this section. The average power delivered can now be written in terms of the ideal current

$$P = I_{ideal} V_{ideal} \tag{2.1.19}$$

and this allows the power factor to be written simply as the ratio

$$PF = \frac{I_{ideal}}{I_{rms}} \tag{2.1.20}$$

Next, we define what is meant by a harmonic. For any positive integer n, the n^{th} harmonic is a function of the form

$$i_n(\theta) = \sqrt{2}\, I_n \sin(n\theta + \phi_n) \tag{2.1.21}$$

where I_n is the rms magnitude of the harmonic, and ϕ_n is the phase. The frequency of the n^{th} harmonic is n times that of the fundamental (first) harmonic. Using a well-known formula from trigonometry, this harmonic may also be written

$$i_n(\theta) = \sqrt{2}\, I_n (\cos n\theta \sin\phi_n + \sin n\theta \cos\phi_n) \tag{2.1.22}$$

Now, by setting

$$a_n = \sqrt{2} I_n \sin\phi_n \quad \text{and} \quad b_n = \sqrt{2} I_n \cos\phi_n \tag{2.1.23}$$

we find that every harmonic of the form (2.1.21) can also be expressed

$$i_n(\theta) = a_n \cos n\theta + b_n \sin n\theta \tag{2.1.24}$$

Conversely, every function of this form is also a harmonic. To show this, we can solve equations (2.1.22) for I_n and ϕ_n. The result is

$$I_n = \sqrt{\frac{a_n^2 + b_n^2}{2}} \quad \text{and} \quad \phi_n = \tan^{-1}\frac{a_n}{b_n} \tag{2.1.25}$$

The Fourier series expansion of the input current, equation (2.1.8), can now be written as the sum of harmonics of the form (2.1.21):

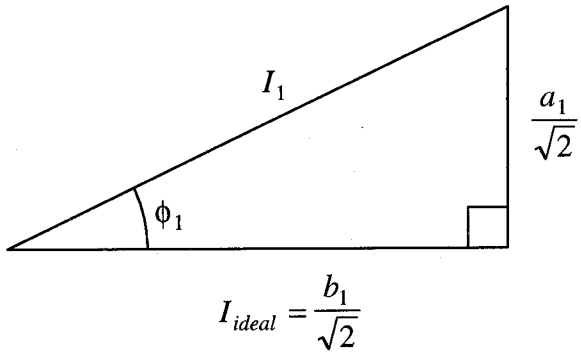


Figure 2.2: Geometric picture of the fundamental input current component.

$$i(\theta) = I_0 + \sum_{n=1}^{\infty} \sqrt{2}\, I_n \sin(n\theta + \phi_n) \tag{2.1.26}$$

Consider the fundamental harmonic. Its magnitude and phase angle are given by

$$I_1 = \sqrt{\frac{a_1^2 + b_1^2}{2}} \quad ; \quad \phi_1 = \tan^{-1}\frac{a_1}{b_1} \tag{2.1.27}$$

These formulas provide the geometric picture of the fundamental component of the current shown in figure 2.2. From the picture, it is clear that

$$I_{ideal} = I_1 \cos\phi_1 \tag{2.1.28}$$

which allows the power factor (2.1.20) to be expressed as the product of two factors

$$PF = \frac{I_1}{I_{rms}} \cos\phi_1 \tag{2.1.29}$$

The first factor, I_1/I_{rms}, is called the "distortion factor." To see how the distortion factor gets its name, we need a result called Parseval's theorem. We can derive Parseval's theorem as follows: In the definition of rms current, equation (2.1.4), replace the function $i(\theta)$ by its Fourier series expansion (2.1.8):

$$I_{rms}^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} \left[I_0 + \sum_{n=1}^{\infty} \sqrt{2} I_n \sin(n\theta + \phi_n) \right]^2 d\theta \tag{2.1.30}$$

If we now expand the square of the quantity in brackets, and then integrate term-by-term, only the integrals of products of like functions remain, while integrals of products of different functions vanish. This equation may therefore be written

$$I_{rms}^2 = \frac{1}{2\pi}\left\{\int_{-\pi}^{\pi} I_0^2 \, d\theta + \sum_{n=1}^{\infty} \int_{-\pi}^{\pi} \left[\sqrt{2}\, I_n \sin(n\theta + \phi_n)\right]^2 d\theta\right\} \tag{2.1.31}$$

Using the last of the auxiliary formulas (2.1.8), this reduces to simply

$$I_{rms}^2 = I_0^2 + I_1^2 + I_2^2 + \ldots \tag{2.1.32}$$

also known as Parseval's theorem. Now consider the usual case when the dc component of the current $I_0 = 0$. In this case, the distortion factor, I_1/I_{rms}, can be expressed

$$DF = \frac{1}{\sqrt{1 + (THD)^2}} \tag{2.1.33}$$

where *THD* is the total harmonic distortion. It is clear from this result how distortion components present in the circuit act to degrade the power factor.

The second component of the power factor in equation (2.1.29), $\cos\phi_1$, accounts for the phase displacement of the fundamental component of the current relative to the voltage, and is therefore given the name "displacement factor." From figure 2.2, it is easily seen that the displacement factor may be expressed

$$\cos\phi_1 = \frac{I_{ideal}}{I_1} \tag{2.1.34}$$

It is clear that this ratio is unity only when the quadrature component of the fundamental current harmonic, a_1, is zero. It is also clear that this quadrature component is solely responsible for any degradation of the power factor due to phase displacement, and that the phase of all other harmonic components is irrelevant insofar as the power factor is concerned.

Summarizing the results of this section, the power factor, distortion factor, and displacement factor may be written as the ratios of currents

$$PF = \frac{I_{ideal}}{I_{rms}} \quad ; \quad DF = \frac{I_1}{I_{rms}} \quad ; \quad \cos\phi_1 = \frac{I_{ideal}}{I_1} \tag{2.1.35}$$

and these expressions will be used to compute these quantities in later chapters. From the results of this section, it is easy to see that the following inequalities must hold

$$I_{rms} \geq I_1 \geq I_{ideal} \tag{2.1.36}$$

with equality only when the power factor is unity. Therefore, when the power factor is unity, we conclude that the current consists of a single component at the fundamental frequency, with no harmonics present, and with no phase displacement of the current relative to the voltage waveform. Thus, when the power factor is unity, the current waveform is determined, as given by

$$i(\theta) = \sqrt{2}\, I_{ideal} \sin\theta \tag{2.1.37}$$

and this is exactly the ideal current waveform. We stated in the beginning of this chapter that, in general, proportional current yields unity input power factor, as demonstrated by the case of the linear resistor. The present result shows, at least for the case of sinusoidal input voltage, that unity input power factor also implies that the input current is proportional, and that this current waveform is unique. Note that any current waveform for which $b_1 = \sqrt{2} I_{ideal}$, regardless of all other coefficients, causes exactly the same average power, $P = I_{ideal} V_{ideal}$, to be absorbed by the load. The ideal current waveform is, however, the smallest of all of these waveforms, in the rms sense.

It should be reemphasized that these results are based on the assumption of ideal sinusoidal input voltage, and are not correct in general. For the more general case of a non-sinusoidal periodic input source, the linear resistor example demonstrates that input current which is proportional to the input voltage implies unity input power factor. It can also be shown that the converse is true; i.e., that unity input power factor implies proportional voltage and current [1]. However, proof of this statement beyond the scope of this discussion. Nevertheless, we have proven this result for the specific case of sinusoidal input voltage, and conclude not only that proportional input current implies unity input power factor, but also that unity input power factor implies proportional (i.e., sinusoidal) input current.

2.2 The Ideal Rectifier

The ideal rectifier system represents the goal of a real rectifier system, and therefore provides a basis against which the real system may be compared. The ideal rectifier itself is a two-port network within the ideal rectifier system, as shown in figure 2.2. In this idealization, the ac power source is assumed to be an ideal sinusoidal voltage source, from which the ideal rectifier, by definition, draws power with unity input power factor. Further, the ideal rectifier is assumed to be lossless, and therefore all of the ac power absorbed at the ac input port is converted to dc power at the dc output port. By "dc power," we mean only that both the current and the voltage at the dc output port are *unipolar*, and nothing is implied about the quality of these waveforms. The quality of the dc output waveforms is handled as a separate issue.

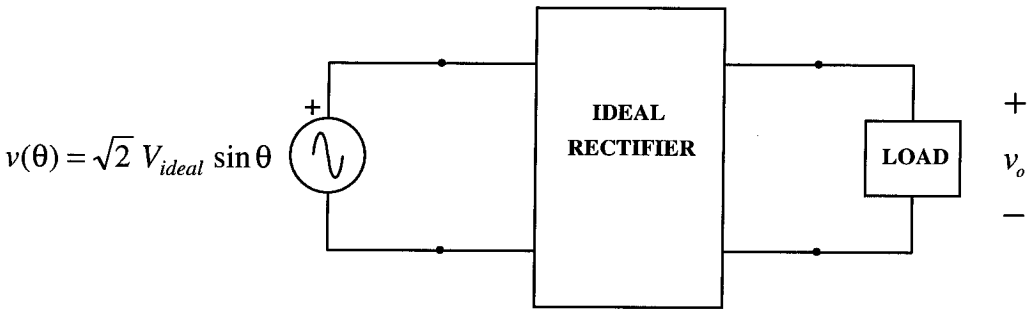


Figure 2.3: The ideal rectifier system consists of an ideal sinusoidal voltage source, the ideal rectifier, and a dc load.

Since the ideal rectifier absorbs power with unity input power factor, the current flowing into the ac port is exactly the ideal current given by equation (2.1.37). The average power absorbed at this port is therefore

$$P = I_{ideal} V_{ideal} \tag{2.2.1}$$

Since the ideal rectifier is lossless, this power represents the output power as well. At any instant, the input current is proportional to the input voltage, and we may therefore write

$$v(\theta) = i(\theta) R_{ideal} \tag{2.2.2}$$

where the constant of proportionality, R_{ideal}, represents the impedance looking into the ac port of the ideal rectifier. This representation leads to the familiar static relationships for rms quantities

$$V_{ideal} = I_{ideal} R_{ideal} \quad ; \quad P = I_{ideal}^2 R_{ideal} \quad ; \quad P = \frac{V_{ideal}^2}{R_{ideal}} \tag{2.2.3}$$

In actual rectifier applications, the known quantities are usually the input voltage and the output (load) power. The ideal current and ideal resistance may be written in terms of these quantities as

$$I_{ideal} = \frac{P}{V_{ideal}} \quad ; \quad R_{ideal} = \frac{V_{ideal}^2}{P} \tag{2.2.4}$$

These relations will prove to be useful in assessing the performance of non-ideal rectifier circuits, since they represent optimum values, and therefore serve as a basis for the normalization of theoretical or measured values. For example, input current harmonics can be normalized according to

$$\mathrm{i}_n = \frac{I_n}{I_{ideal}} \tag{2.2.5}$$

Also, in the analysis of passive rectifier circuits, we will find it convenient to normalize the impedance of reactive elements within the rectifier circuit with respect to the ideal resistance R_{ideal}. Hence, we define

$$\rho \equiv \frac{|Z(j\omega_l)|}{R_{ideal}} \tag{2.2.6}$$

called the normalized impedance. This ratio is a measure of the size of the impedance of the reactive component, evaluated at the line frequency, relative to the input impedance of the ideal rectifier. In chapter 3, we will see how the performance characteristics of the passive rectifier circuits can be assessed as a function of this parameter alone. In addition, the time domain input voltage and input current waveforms can be normalized with respect to their ideal values. That is, the (sinusoidal) input voltage is normalized with respect to its peak value, according to

$$v(\theta) = \frac{v(\theta)}{V_p} \quad ; \quad V_p = \sqrt{2}\, V_{ideal} \tag{2.2.7}$$

Similarly, the input current is normalized with respect to the peak value of the ideal current

$$i(\theta) = \frac{i(\theta)}{\sqrt{2} I_{ideal}} \tag{2.2.8}$$

This choice of normalization yields the picture shown in figure 2.4 for the ideal rectifier, where the normalized voltage and current waveforms are both ideal sinusoids with unity peak amplitude. When evaluating a real rectifier circuit, the quality of the input current waveform can be compared to that of the ideal rectifier, not only qualitatively by visually comparing the waveforms, but also quantitatively by using the ideal waveforms as a basis for the normalization of the non-ideal current waveform and its harmonics.

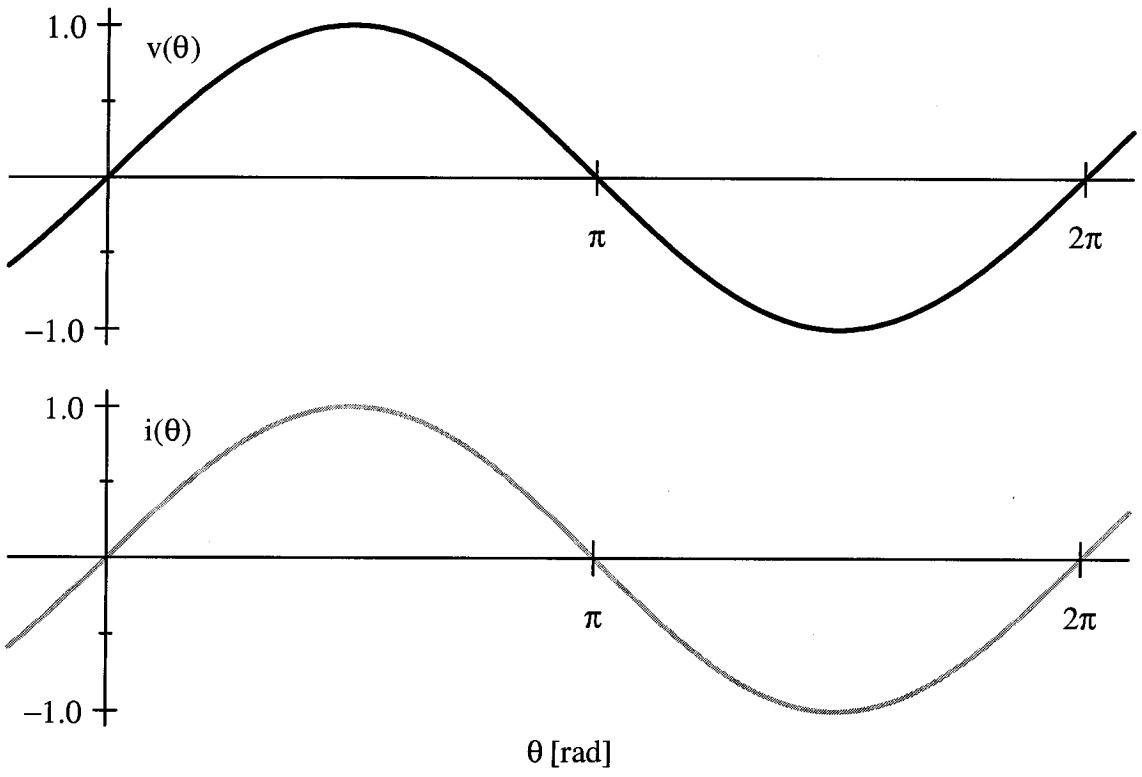


Figure 2.4: Normalized input voltage (black) and input current (grey) for the ideal rectifier.

2.3 Constant Power Load

In the analysis of single phase rectifier circuits, we often make use of a two-terminal element called the constant power load. The constant power load is a simple way to model the effect of loading a rectifier/pre-regulator with a high-performance switching post-regulator, as shown in figure 2.5. In this configuration, the feedback loop of the post-regulator acts to fix the output voltage despite changes in voltage at the post-regulator input, thereby fixing not only the output voltage, but the output power as well. If we assume that the post-regulator is completely efficient and stores no energy, then the power flow into the post-regulator is equal to the output power, and thus appears to the rectifier/pre-regulator as a constant power load.

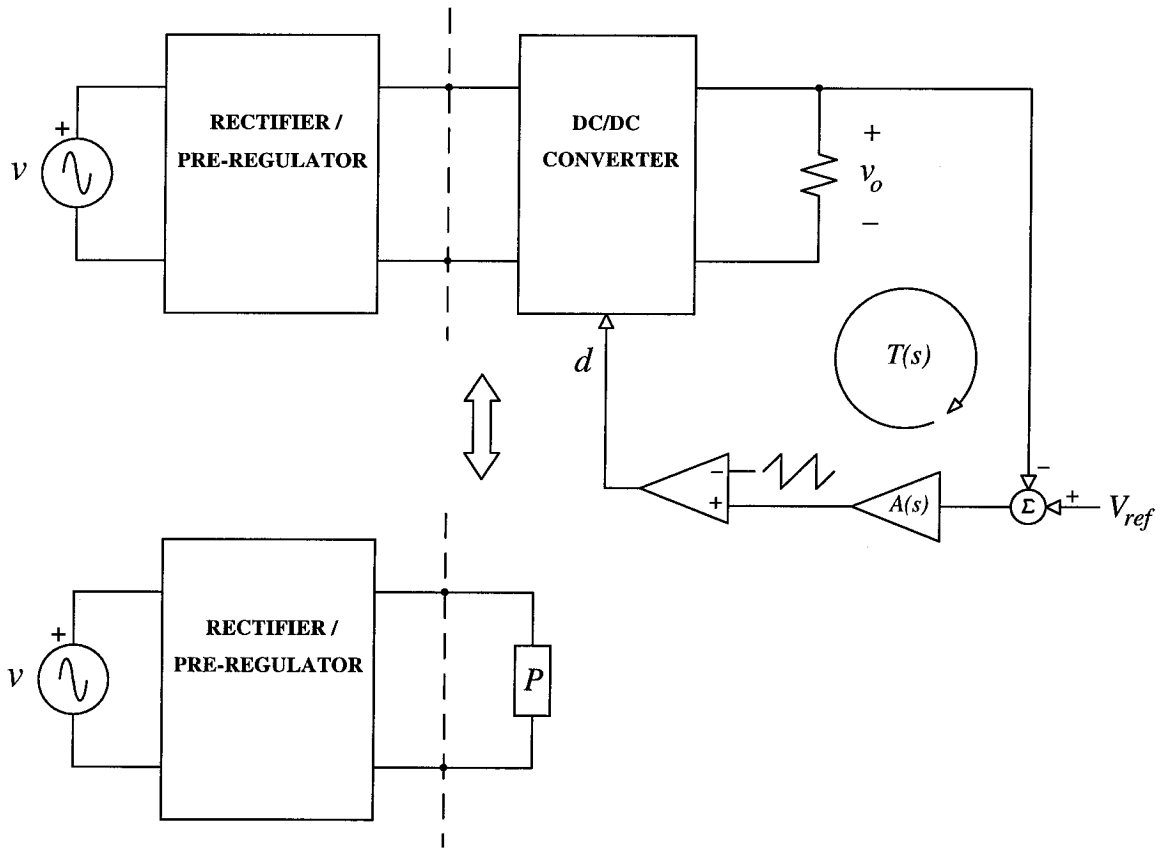


Figure 2.5: The effect of loading the rectifier/pre-regulator with a high performance switching regulator is simply modeled by a constant power load.

In arriving at this conclusion, there are at least three major assumptions necessary. First, it is assumed that the post-regulator feedback loop maintains the output voltage as constant. This assumption is valid at frequencies below the post-regulator loop gain crossover frequency, since crossover marks the frequency at which the feedback is no longer effective. In a well designed post-regulator, this frequency is typically about a decade below the switching frequency. Since, in the design of a rectifier/pre-regulator, we are concerned with circuit operation at the *line* frequency and harmonics thereof, this assumption is normally well justified.

The second assumption is that the post-regulator is completely efficient. This idealization is usually nearly true, with typical post-regulator efficiencies approaching 0.90 or even higher. If it is desired to include the effect of the efficiency, the constant power load is easily adjusted to accommodate this factor, provided the efficiency is independent of the operating point [17]. For the present purpose, we will assume that the post-regulator is completely efficient.

Finally, it is assumed that the post-regulator does not store energy. This, of course, is never justified in any switching regulator containing inductors or capacitors, since these energy storage elements are fundamental to the power conversion process itself. However, in the typical switching post-regulator, these components are sized to process power at the switching frequency, and have little effect on power flow when a small-signal disturbance is introduced at the line frequency, or at low harmonic frequencies thereof. In conclusion, the constant power load can be used to emulate the dc and low frequency loading effect of a high performance switching regulator.

2.3.1 Terminal Characteristics

The large-signal and small-signal terminal characteristics of the constant power load are very different. Consider the constant power load shown in figure 2.6. Its terminal characteristics are defined by

$$P = iv \tag{2.3.1}$$

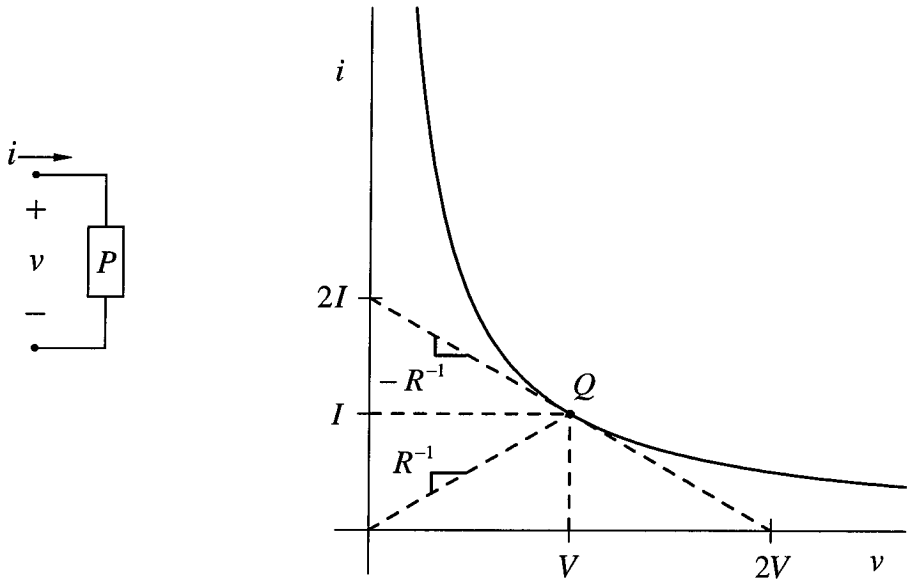


Figure 2.6: The constant power load and its hyperbolic i-v characteristic.

and its i-v characteristic is the constant power hyperbola also shown in figure 2.6. In theory, a constant power load as defined by equation (2.3.1) could also operate in the third quadrant, or even in quadrants two and four as a constant power source, if P is allowed to be negative. However, the purpose here is to emulate the loading effect of the input to a dc/dc switching regulator, which accepts voltage of only one polarity. It is therefore assumed that the constant power load operates in only in the first quadrant. The operating range of a real switching regulator is further limited by its maximum and minimum operating voltages, beyond which it cannot operate. For simplicity however, we will assume that the switching regulator can operate anywhere along the constant power hyperbola in the first quadrant, and that its operating range is not exceeded.

If we denote the ratio of the voltage to the current, evaluated at the operating point, as the large-signal equivalent resistance R, we find

$$R \equiv \frac{V}{I}\bigg|_Q = \frac{V^2}{P} \tag{2.3.2}$$

and the small-signal equivalent resistance r can then be expressed

$$r \equiv \left.\frac{dv}{di}\right|_{Q} = -R \tag{2.3.3}$$

The constant power load exhibits the large-signal behavior of a positive resistance with value R, and the small-signal behavior of a negative resistance with value $-R$. The slope of the line tangent to the i-v curve at point Q in figure 2.3 represents the small-signal *conductance* of the constant power load, which is actually the inverse of this small-signal resistance. These characteristics, both large and small-signal, are good approximations to the low-frequency large and small-signal characteristics of the input to a switching regulator [13]. Hence, for the purpose of studying the low frequency static and dynamic behavior of a rectifier/pre-regulator loaded by a high performance switching post-regulator, the constant power load can be used to emulate the loading effect of the high performance switching post-regulator.

Chapter 3

Passive Rectifier Circuits

In order to put in perspective the wide variety of known rectifier circuits, including both passive and active rectifier circuits, the performance and limitations of passive circuits need to be studied. Passive rectifier circuits consist of passive filter components and diodes only, and are therefore sometimes referred to simply as "passive filters." They offer the advantages of simplicity, durability, and even perhaps cost over active circuits, but disadvantages include the size and weight of passive filter components, the inability to actively control the output voltage, and the limitation of less than unity power factor. However, for a required level of performance, the advantages of a passive scheme may outweigh the disadvantages, making it a viable alternative in certain applications.

In this chapter, several practical passive rectifier circuits are analyzed to determine their level of performance. In each case, it is assumed that the passive rectifier circuit serves as a pre-regulator only, and is to be followed by a high performance switching post-regulator to form a complete ac/dc rectification system. Since the purpose here is to evaluate the pre-regulator portion of this system, the post-regulator is simply modeled by a constant power load, as described in section 2.3. By including the constant power load in the analysis, some surprising differences from similar analyses based on resistive loads are brought out.

The performance of a rectifier circuit can be quantified in various ways, including power factor, total harmonic distortion, and output voltage regulation. In this chapter, these measures are analyzed in detail, with results presented in graphical form. From these graphs, compliance with a particular performance specification or standard can be determined, and the results are easily compared with other passive or active approaches.

3.1 Capacitor Filter

The capacitor filter is actually a problem rather than a solution. Owing to the pulsed nature of the input current to this type of filter, the input current waveform is rich in harmonic content. In the past, the use of these filters was justified in devices that operated in the low power range, say several hundred watts or less, since the number of such devices was not large. In recent years, however, owing to the proliferation of this filter in many different types of electronic equipment, the net effect of having many of these low power devices operating on the same power line simultaneously is significant. Hence, it has become necessary to consider the harmonic content of the input current even for devices operating at low power levels.

The capacitor filter is shown in figure 3.1(a), with its equivalent circuit in figure 3.1(b). The equivalent circuit is actually the output equivalent circuit, which properly represents the voltages and currents on the output side of the bridge rectifier. The actual input current i is found by "unfolding" the equivalent current waveform i_g through the bridge rectifier. This unfolding process is defined mathematically in appendix A.

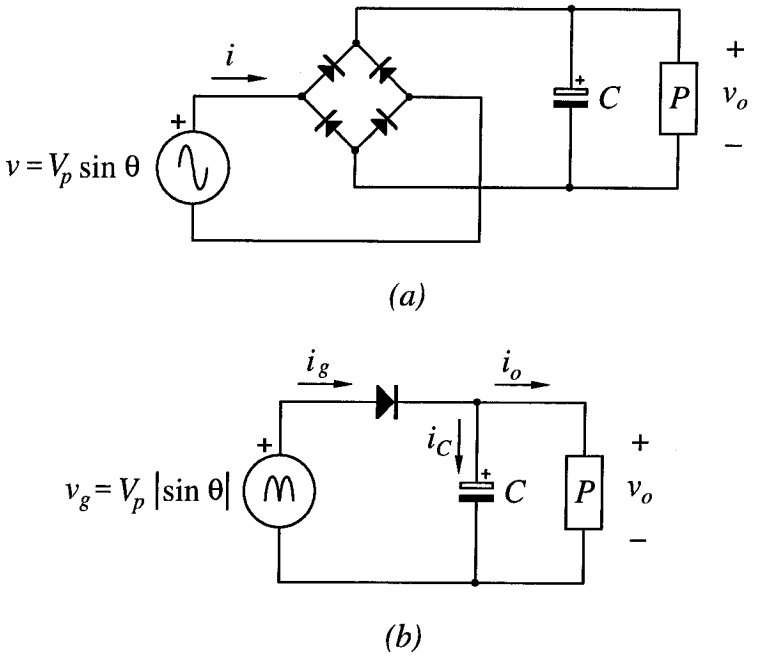


Figure 3.1 *Capacitor filter with constant power load; (a) circuit, and (b) equivalent circuit.*

The analysis of this apparently simple circuit is complicated by the fact that the diodes are not conducting continuously, and the angles through which they conduct need to be determined. Several assumptions are in order before beginning the analysis. These are: (1) the input is an ideal sinusoidal voltage source; (2) the diodes are ideal, with zero voltage when forward-biased, and zero current when reverse-biased; (3) the capacitor is linear and ideal; and (4) the load is the constant power type described in section 2.3. To begin, consider the equivalent circuit of figure 3.1(b). The input voltage to this circuit is the rectified version of the ideal source voltage, given by

$$v_g(\theta) = V_p |\sin\theta| \tag{3.1.1}$$

where V_p is the peak value of the input voltage, related to the ideal sinusoidal input voltage (rms value) by

$$V_p = \sqrt{2}\, V_{ideal} \tag{3.1.2}$$

Since the period of the rectified line voltage is half of the line period, it is sufficient to consider only half of a line cycle to determine the steady-state behavior of the equivalent circuit of figure 3.1(b). Once the input current i_g is found for the equivalent circuit, the input current to the actual circuit is easily constructed by "unfolding" the current waveform i_g through the bridge rectifier. The input current to the equivalent circuit is

$$i_g = \begin{cases} i_C + i_o & ; \text{ diode conducting} \\ 0 & ; \text{ else} \end{cases} \tag{3.1.3}$$

where the capacitor current and the output current are given by

$$i_C(\theta) = \omega_l C \frac{d}{d\theta} v_C(\theta) \quad ; \quad i_o(\theta) = \frac{P}{v_C(\theta)} \tag{3.1.4}$$

Consider the typical capacitor voltage waveform of figure 3.2. Let θ_1 be the angle at which diode conduction begins, and let θ_2 be the angle at which diode conduction terminates. Between these angles, the diode is conducting, and the input voltage and the capacitor voltage are therefore equal. The input current for the equivalent circuit over the entire half cycle $0 \le \theta \le \pi$ is therefore

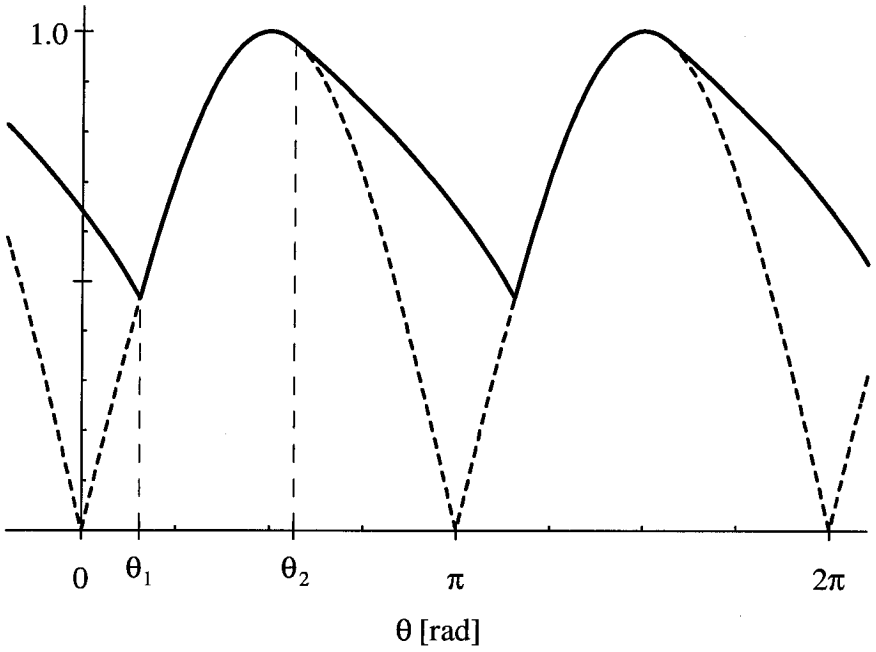


Figure 3.2: Normalized capacitor voltage waveform (solid) and rectified input voltage (dashed) for the capacitor input filter. ($\rho_C = 0.16$)

$$i_g(\theta) = \begin{cases} 0 \;\; ; \;\; 0 \le \theta < \theta_1 \\ \omega_l C V_p \cos\theta + \dfrac{P}{V_p \sin\theta} \;\; ; \;\; \theta_1 \le \theta \le \theta_2 \\ 0 \;\; ; \;\; \theta_2 \le \theta \le \pi \end{cases} \tag{3.1.5}$$

The current is discontinuous at θ_1, when the diode turns on, but continuous at θ_2, when the diode opens. Solving equation (3.1.5) for angle θ_2 gives

$$\sin 2\theta_2 + \rho_C = 0 \tag{3.1.6}$$

where the normalized impedance of the capacitor, ρ_C, combines the effects of known circuit quantities into one convenient parameter

$$\rho_C \equiv \frac{|Z_C(j\omega_l)|}{R_{ideal}} = \frac{P}{\omega_l C V_{ideal}^2} \tag{3.1.7}$$

The solution of equation (3.1.6) is multi-valued and choosing the correct solution for θ_2 is a little tricky. Examining figure 3.2, the correct solution is the first solution that occurs after $\theta = \pi/2$, and is given by

$$\theta_2 = \frac{\pi}{2} + \frac{1}{2}\mathrm{Sin}^{-1}\rho_C \tag{3.1.8}$$

where $\mathrm{Sin}^{-1}\rho_C$ denotes the principal value of the inverse sine function.

Next, consider the interval $\theta_2 \le \theta \le \pi + \theta_1$. During this interval, the diode is open and the output current is supported entirely by the capacitor. The capacitor voltage is described by the separable type first-order differential equation

$$\omega_l C \frac{dv_C}{d\theta} + \frac{P}{v_C} = 0 \tag{3.1.9}$$

subject to the initial condition at $\theta = \theta_2$:

$$v_C(\theta_2) = V_p \sin\theta_2 \tag{3.1.10}$$

Solving, we find the capacitor voltage for the interval $\theta_2 \le \theta \le \pi + \theta_1$:

$$v_C(\theta) = V_p\sqrt{\sin^2\theta_2 - \rho_C(\theta - \theta_2)} \tag{3.1.11}$$

Angle θ_1 is still undetermined. Referring to figure 3.2, angle $\pi + \theta_1$ occurs at the moment when the capacitor voltage waveform intercepts the rectified line voltage waveform. This leads to the transcendental relation

$$\sin^2\theta_2 - \sin^2\theta_1 - \rho_C(\pi + \theta_1 - \theta_2) = 0 \tag{3.1.12}$$

which, given angle θ_1, is solved to find angle θ_2, with θ_1 in the range $0 < \theta_1 < \pi/2$. Note that if $\theta_1 = 0$ is allowed, the capacitor voltage falls to zero at the instant $\theta = \theta_1$. However, the capacitor voltage must not be allowed to fall to zero, because infinite output current will result in order to maintain constant power to the load. It is therefore necessary to restrict θ_1 to be strictly larger than zero. Hence, the case $\theta_1 = 0$ defines a critical boundary of circuit operation. The corresponding critical value of θ_2 is found by solving equations (3.1.6) and (3.1.12) for angle θ_2 with $\theta_1 = 0$. This yields a transcendental equation for $\theta_{2,\mathrm{crit}}$:

$$\tan\theta_{2,\text{crit}} + 2(\pi - \theta_{2,\text{crit}}) = 0 \;\Rightarrow\; \theta_{2,\text{crit}} \cong 1.9760 \text{ rad} \tag{3.1.13}$$

Again using equation (3.1.6), this value of θ_2 corresponds to a critical value for ρ_C, beyond which operation with a constant power load is rendered impossible:

$$\rho_{C,\text{crit}} = -\sin 2\theta_{2,\text{crit}} \cong 0.7246 \tag{3.1.14}$$

For values of ρ_C larger than $\rho_{C,\text{crit}}$, the capacitor voltage is allowed to fall to zero during the line cycle, rendering operation of the rectifier circuit with a constant power load impossible. The value $\rho_C = \rho_{C,\text{crit}}$ thus represents the critical boundary for circuit operation with a constant power load, and in practical circuits, ρ_C should probably be kept well below this critical value.

It is interesting to note that operation of the capacitor filter with a resistive load exhibits no such critical boundary. With a resistive load, the interval during which the bridge rectifier is open is characterized by exponential decay of the capacitor voltage. This is in contrast to the discharge of the capacitor into a constant power load, described by the square-root relationship in equation (3.1.11). This difference is apparent by examining the capacitor voltage waveform in figure 3.2. The plot shows that with a constant power load, during the interval when the rectifier bridge is open, the capacitor voltage waveform actually curves *downward*, indicative of the increased output current demand necessary to maintain constant output power as the output voltage decreases. During the equivalent interval with a resistive load, the capacitor voltage decays exponentially, and theoretically never reaches zero regardless of the values chosen for the resistor and capacitor. Thus, with a resistive load, there may be large ripple, but there is no critical boundary like that for the constant power load.

3.1.2 Performance Characteristics

In this section, it is shown that the performance characteristics such as ac/dc conversion ratio, ripple ratio, and power factor can be considered functions of a single parameter, namely the normalized impedance ρ_C. These performance characteristics are then plotted as a function of this parameter alone. Using these results, the applicability of a particular design can easily be assessed.

Conduction Angle

Angle θ_2 is expressed as an explicit function of the normalized impedance ρ_C in equation (3.1.8). In addition, angle θ_1 is related to angle θ_2 through the transcendental relationship (3.1.12), and thus may also be considered a function of ρ_C. Using these results, these angles are plotted in figure 3.3 as a function of ρ_C. Although the conduction angle is largest at the critical boundary, operation near this boundary is not recommended, because the output voltage ripple becomes too large for most practical applications.

Ac/Dc Conversion Ratio, Ripple Ratio

With the angles θ_1 and θ_2 known, the ac/dc conversion ratio and output ripple voltage can be determined. We define the peak ac/dc conversion ratio as the ratio of the average dc output voltage to the peak line voltage

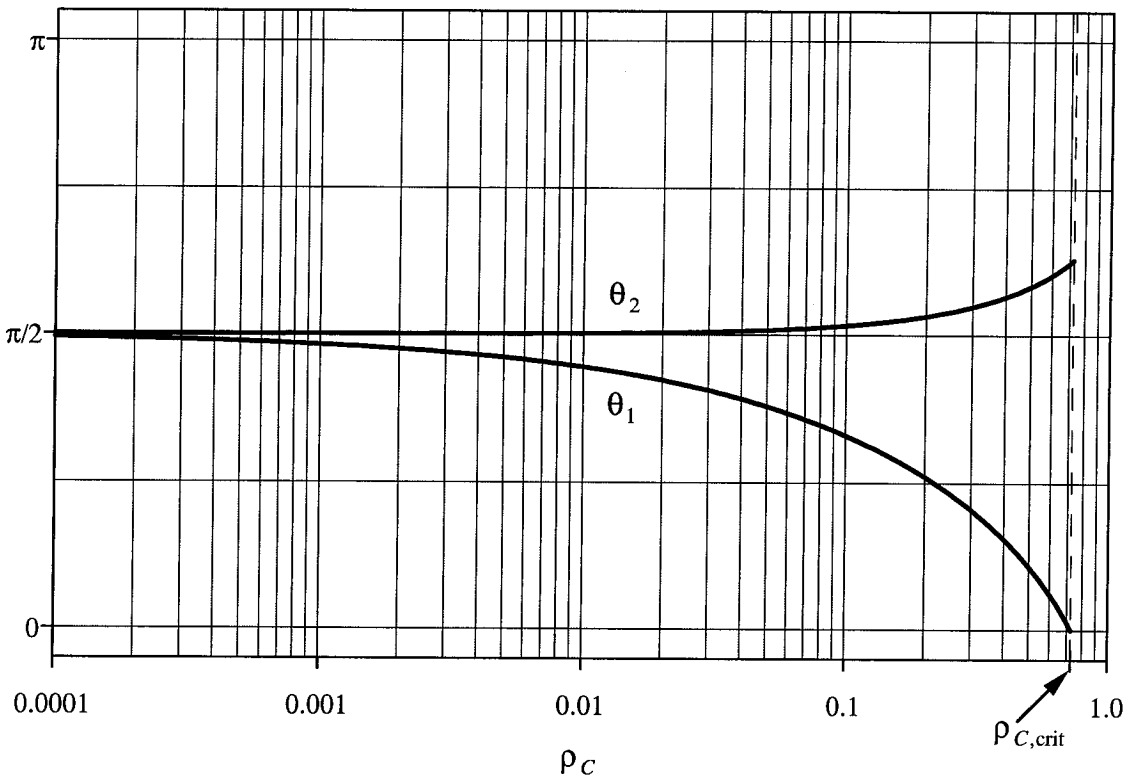


Figure 3.3: Angles θ_1 and θ_2 for the capacitor filter as a function of the normalized impedance ρ_C.

$$M_p \equiv \frac{V_o}{V_p} \tag{3.1.15}$$

The average output voltage is given by the integral

$$V_o = \frac{1}{\pi} \int_{\theta_1}^{\pi+\theta_1} v_C(\theta) d\theta \tag{3.1.16}$$

Over the interval of integration, the instantaneous capacitor voltage is given by

$$v_C(\theta) = \begin{cases} V_p \sin\theta \quad ; \quad \theta_1 \le \theta \le \theta_2 \\ V_p \sqrt{\sin^2 \theta_2 - \rho_C(\theta - \theta_2)} \quad ; \quad \theta_2 \le \theta \le \pi + \theta_1 \end{cases} \tag{3.1.17}$$

from which the peak ac/dc conversion ratio is found

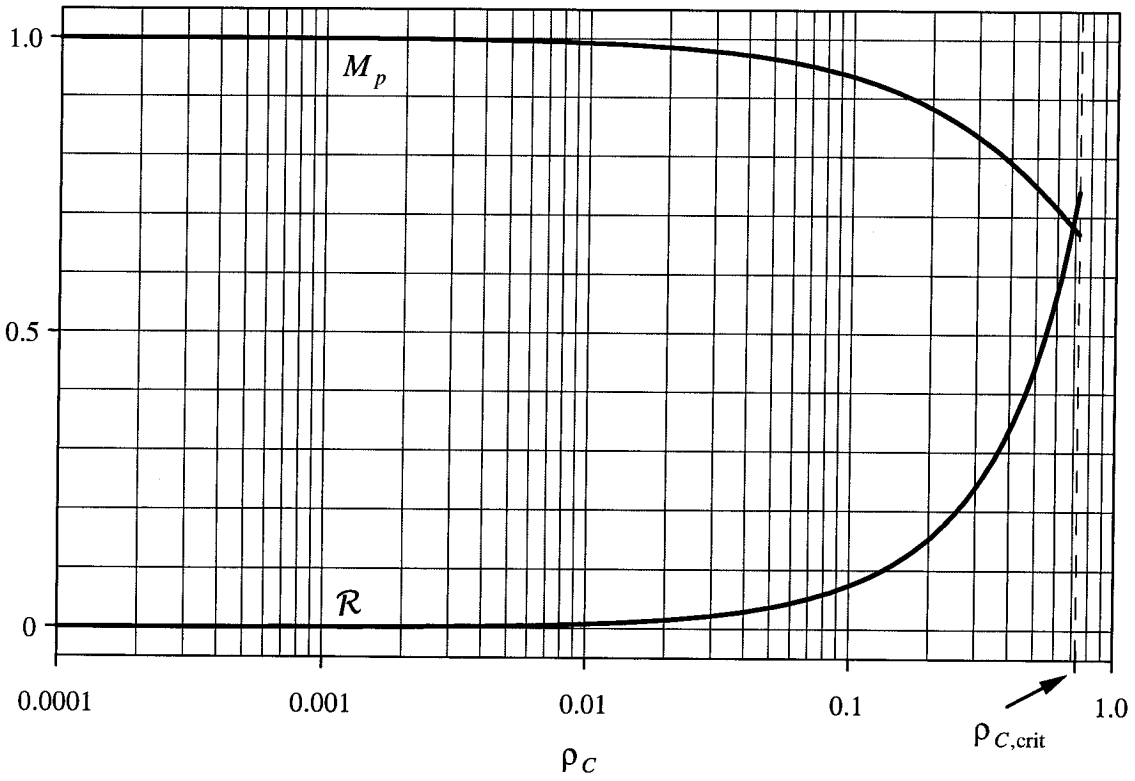


Figure 3.4: Peak ac/dc conversion ratio M_p and ripple ratio $\mathcal{R}$ as a function of the normalized impedance ρ_C.

$$M_p = \frac{1}{\pi}\left[\cos\theta_1 - \cos\theta_2 + \frac{2}{3\rho_C}(\sin^3\theta_1 - \sin^3\theta_2)\right] \tag{3.1.18}$$

and is plotted in figure 3.4 as a function of normalized impedance ρ_C. We define the "ripple ratio" $\mathcal{R}$ as the ratio of one-half of the peak-to-peak output voltage ripple to the average dc output voltage

$$\mathcal{R} \equiv \frac{v_{o,\max} - v_{o,\min}}{2V_o} \tag{3.1.19}$$

A little algebra gives the ripple ratio for the capacitor filter

$$\mathcal{R} = \frac{1 - \sin\theta_1}{2M_p} \tag{3.1.20}$$

which is also plotted in figure 3.4 as a function of the normalized impedance ρ_C.

Power Factor and Harmonics

In the preceding analysis, normalized impedance ρ_C was used to collect known circuit quantities into a single parameter, against which the desired circuit performance characteristics could be evaluated. In this section, it is shown that the line current harmonics and power factor can also be expressed as functions of this same parameter. The actual input current to the capacitor filter is the alternating periodic extension (see appendix A) of the input current to the equivalent circuit on the interval $0 \le \theta \le \pi$. For the equivalent circuit, the input current is given by equation (3.1.5), and may be written in terms the ideal current as

$$i_g(\theta) = \begin{cases} 0 \;\; ; \;\; 0 \le \theta < \theta_1 \\ I_{ideal}\sqrt{2}\left[\dfrac{1}{\rho_C}\cos\theta + \dfrac{1}{2}\csc\theta\right] \;\; ; \;\; \theta_1 \le \theta \le \theta_2 \\ 0 \;\; ; \;\; \theta_2 \le \theta \le \pi \end{cases} \tag{3.1.21}$$

where the ideal current, defined in chapter 2, is given by

$$I_{ideal} = \frac{P}{V_{ideal}} \tag{3.1.22}$$

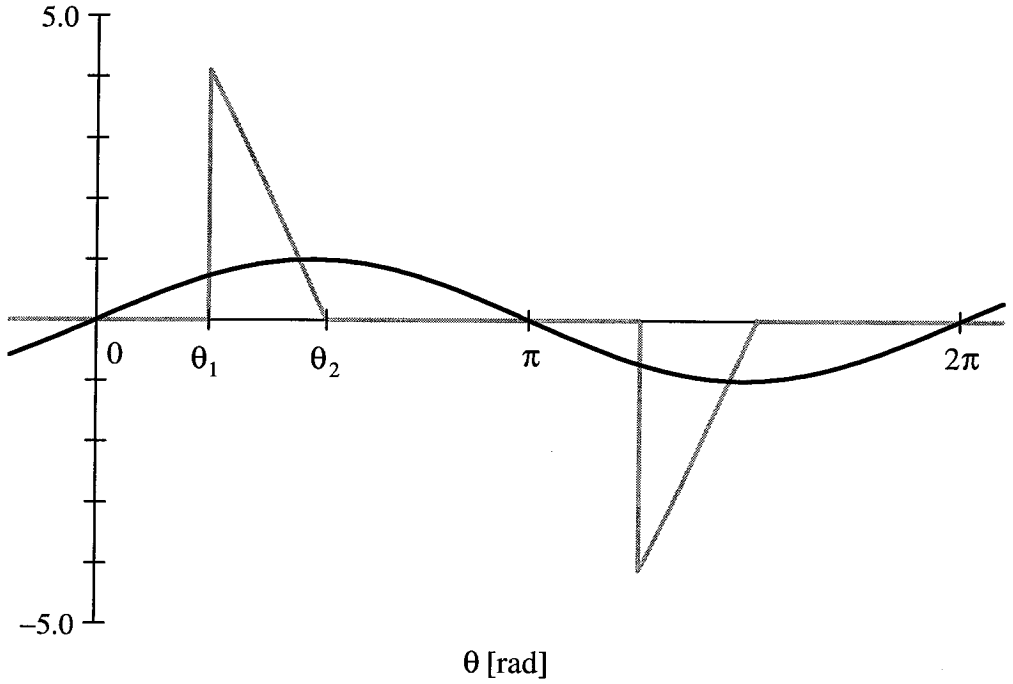


Figure 3.5: Normalized input voltage (black) and input current (grey) for the capacitor filter. ($\rho_C = 0.20$)

Figure 3.5 shows a plot of the normalized input voltage and current for the capacitor filter with $\rho_C = 0.20$. This example exemplifies the poor performance of this filter.

The Fourier coefficients of the alternating periodic extension are computed using the results of appendix A. Fundamental coefficients a_1 and b_1 are given by

$$a_1 = I_{ideal}\frac{\sqrt{2}}{\pi}\left\{\frac{1}{\rho_C}(\theta_2 - \theta_1) + \frac{1}{2\rho_C}(\sin 2\theta_2 - \sin 2\theta_1) + \log_e \frac{\sin\theta_2}{\sin\theta_1}\right\} \qquad (3.1.23)$$

$$b_1 = I_{ideal}\sqrt{2}$$

The rms input current is given by

$$I_{rms} = I_{ideal}\frac{1}{\sqrt{2\pi}}\left[\cot\theta_1 - \cot\theta_2 + \frac{2}{\rho_C^2}(\theta_2 - \theta_1) + \frac{4}{\rho_C}\log_e\frac{\sin\theta_2}{\sin\theta_1} + \frac{1}{2\rho_C^2}(\cot\theta_2 - \cot\theta_1 + \cos 3\theta_1 \csc\theta_1 - \cos 3\theta_2 \csc\theta_2)\right]^{\frac{1}{2}} \qquad (3.1.24)$$

Using these results, the power factor, distortion factor, and displacement factor are computed using the results of chapter 2, and are plotted in figure 3.6 as a function of the normalized impedance ρ_C.

The normalized current harmonics are defined by the ratio

$$i_n \equiv \frac{I_n}{I_{ideal}} \tag{3.1.25}$$

These harmonics are computed by finding the Fourier coefficients of the alternating periodic extension of the current waveform i_g over the interval $0 \le \theta \le \pi$. As shown in appendix A, the alternating periodic extension of a function contains only odd harmonics. Using these results, normalized odd current harmonics 1 through 39 are computed numerically and are plotted in figure 3.7, once again as a function of the normalized impedance ρ_C.

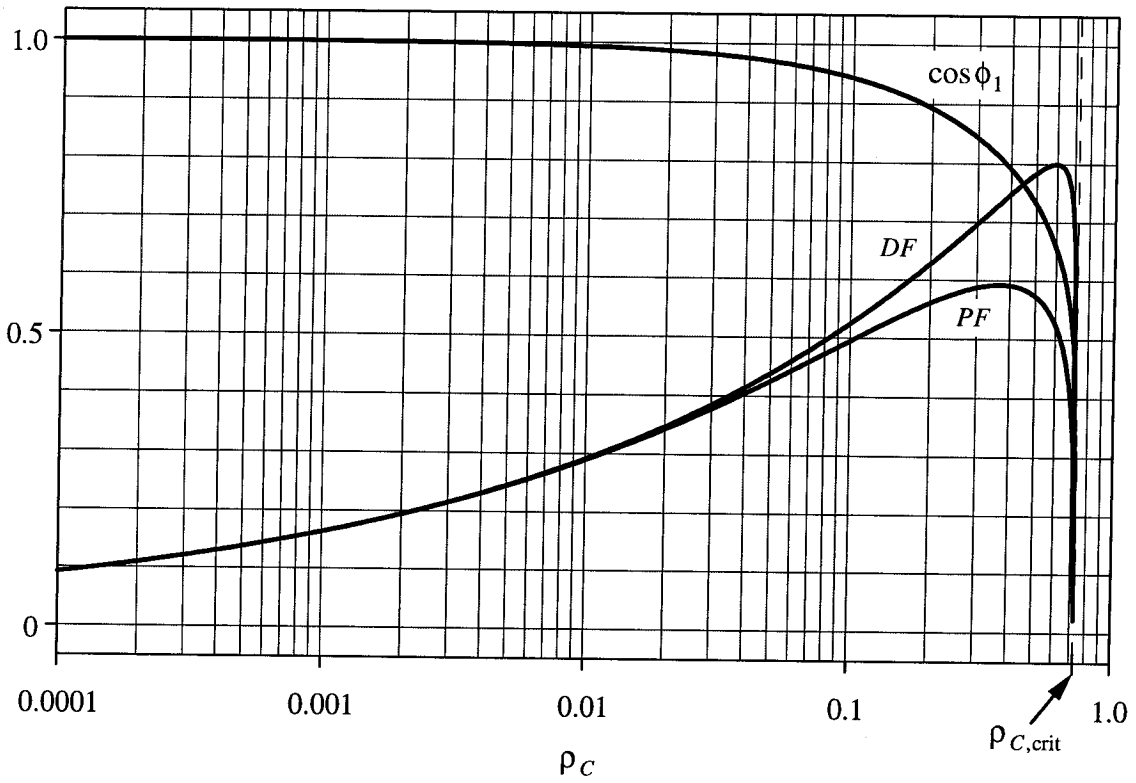


Figure 3.6: Power factor, distortion factor, and displacement factor as a function of normalized impedance ρ_C for the capacitor filter. Operation in the region beyond $\rho_C = \rho_{C,crit}$ is not possible.

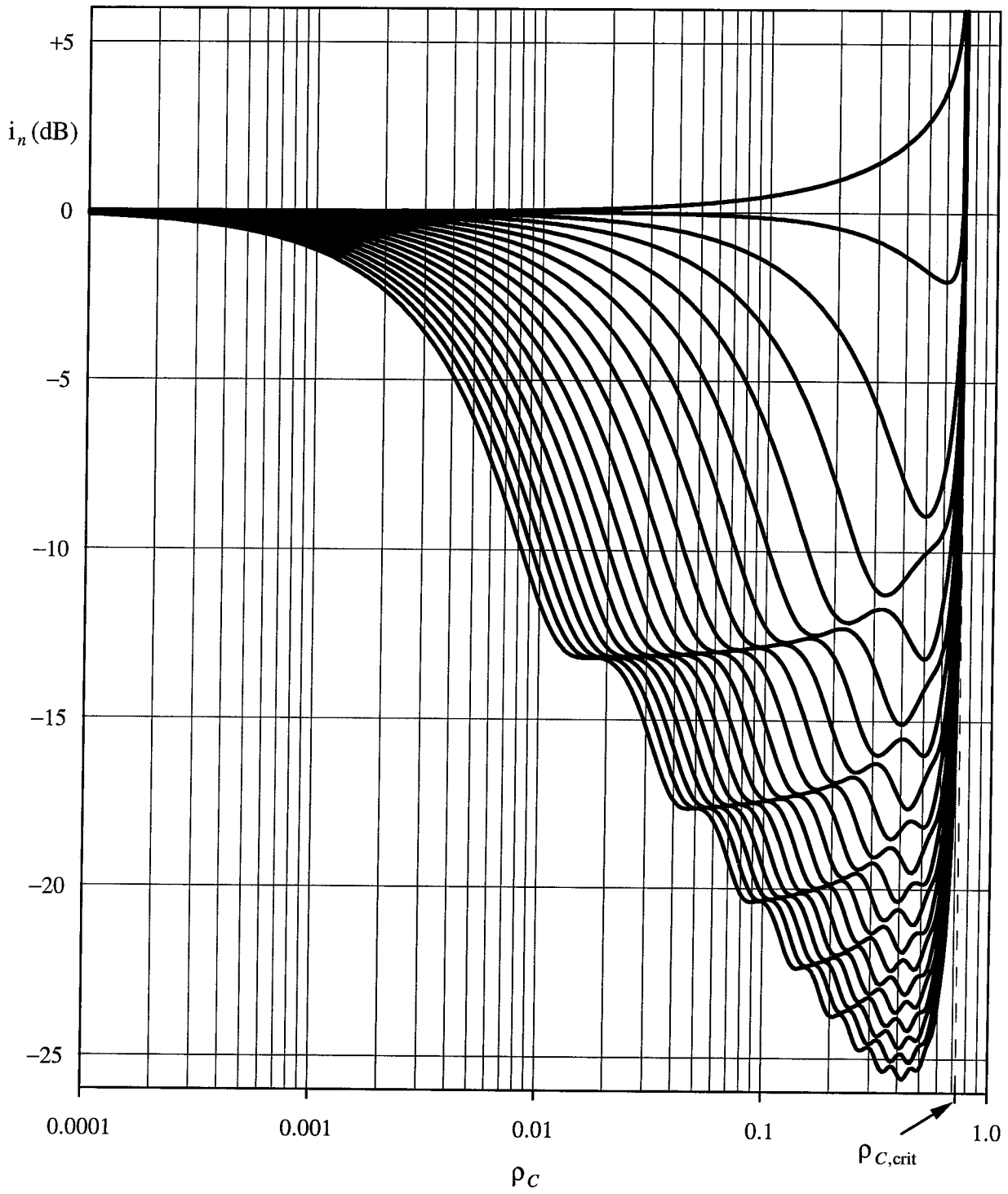
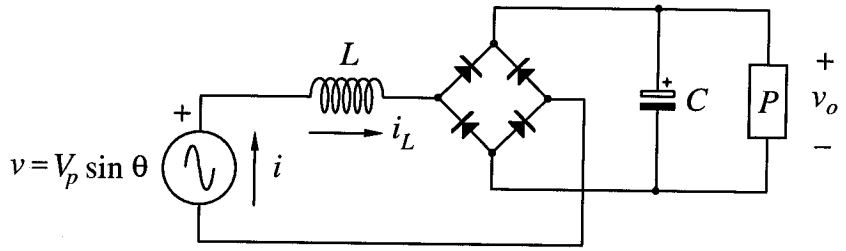


Figure 3.7: Normalized odd current harmonics 1-39 as a function of normalized impedance ρ_C for the capacitor filter. The topmost curve is the fundamental, and odd harmonics 3-39 progress downward in order.

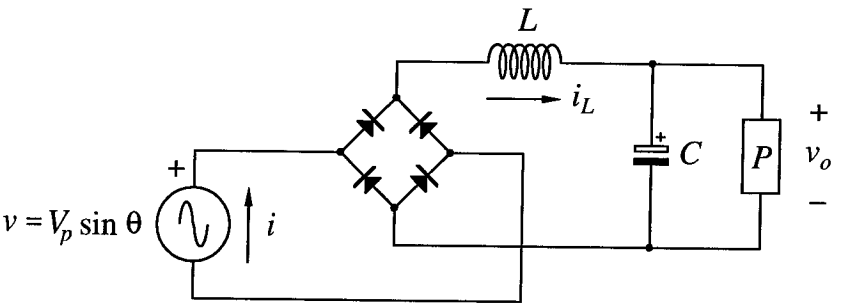
3.2 Inductor Filter

The inductor filter consists of the same elements found in the capacitor filter, plus an inductor. The inductor improves performance by broadening the conduction angle of the bridge rectifier. The inductor filter offers an additional degree of freedom over the capacitor filter, since the inductor can be sized to provide quality ac input current, and the capacitor sized to provide quality dc output voltage. In the present analysis, however, the capacitor is assumed to be large enough that the output voltage may be considered constant, and only the effect of the inductor is considered.

Two different inductor filter configurations are analyzed in the following sections, and are shown in figure 3.12. The behavior of these two configurations can be identical or very different, depending on the operating mode. The load-side inductor filter is frequently analyzed in the literature [1,30]. It is shown here, however, that the line-side inductor filter can offer a performance improvement, by offering reduced input current harmonics over a wider operating range. The simple explanation for this is that the



(a)



(b)

Figure 3.8: Two different inductor input filter configurations: (a) line-side inductor filter; and (b) load-side inductor filter.

inductor in the line-side inductor filter is connected adjacent to the input, thereby promoting continuity of the input current, and reducing the current harmonics.

The line-side filter does, however, suffer from one serious drawback which may explain why it is not often used. Consider a device employing a line-side inductor filter which is suddenly removed from the ac power source (i.e., unplugged). The inductor current path is suddenly interrupted, leaving no path for the inductor current to flow. In actual designs, however, a capacitor can be connected across the input both to correct the lagging phase angle, and to provide a path for the inductor current as well. The load-side filter, on the other hand, suffers from no such drawback, since the bridge rectifier provides the necessary path for the inductor current. However, even for the load-side inductor filter, it may be desirable to include the additional capacitor across the input, to correct the lagging phase angle thereby improving the circuit power factor.

Analysis of the inductor filters proceeds in much the same way as the capacitor filter. The assumptions here are: (1) the output capacitor is assumed sufficiently large so that the output voltage may be considered constant; (2) the input is an ideal sinusoidal voltage source; (3) the diodes are ideal, with zero voltage when forward-biased, and zero current when reverse-biased; (4) the inductor is ideal; and (5) the load is the constant power type of section 2.3.

3.3 Line-Side Inductor Filter

The behavior of this filter depends on the operating mode. The line-side inductor filter possesses two distinct operating modes, one called the continuous conduction mode (ccm), and the other called the discontinuous conduction mode (dcm). In ccm, there is no finite interval within the line period over which the inductor current is zero. The inductor current in ccm is zero only at the distinct instants of the zero-crossings. In dcm, however, the inductor current remains zero during finite intervals within the line period.

3.3.1 Discontinuous Conduction Mode

Operation in the discontinuous conduction mode (dcm) is characterized by finite intervals during which the inductor current is zero. Typical normalized input voltage

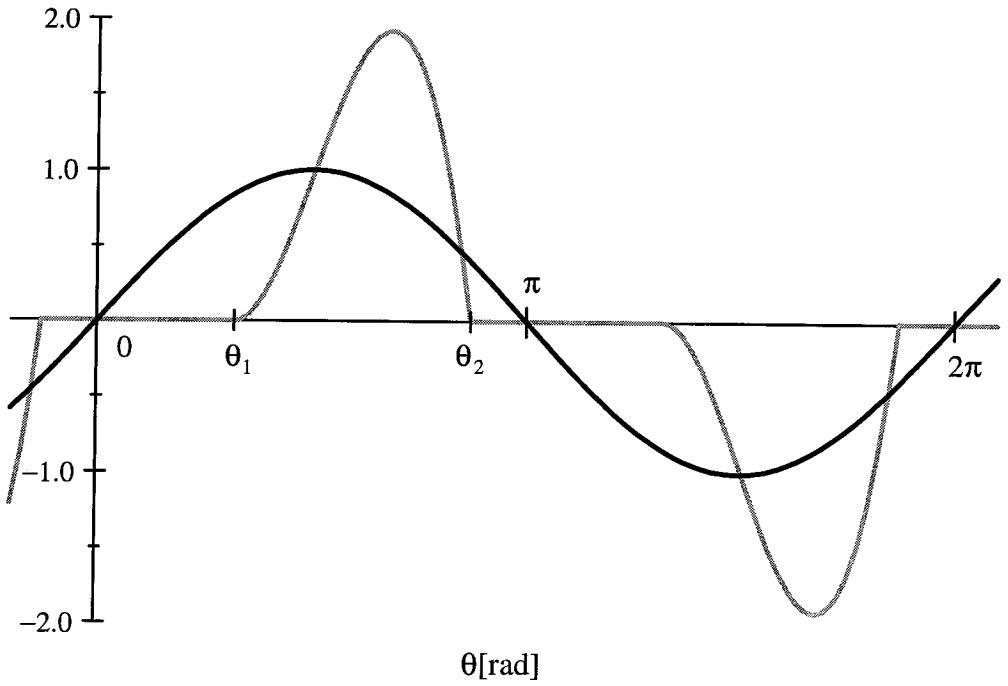


Figure 3.9: Normalized input current (grey) and input voltage (black) for the inductor input filter in discontinuous conduction mode ($\rho_L = 0.063$).

and current waveforms in dcm are shown in figure 3.9. Assume that the circuit is operating in steady-state with constant dc output voltage V_o. Turn-on angle θ_1 occurs at the moment when the ac input voltage overtakes the dc output voltage. This gives

$$V_p \sin\theta_1 = V_o \tag{3.3.1}$$

where V_p is the peak value of the sinusoidal input voltage. The peak ac/dc conversion ratio in dcm is then simply

$$M_{p,\mathrm{dcm}} = \sin\theta_1 \tag{3.3.2}$$

The fundamental *i-v* relationship for an inductor, as a function of the normalized time variable θ, is given by

$$v_L(\theta) = \omega_l L \frac{d}{d\theta} i_L(\theta) \tag{3.3.3}$$

The inductor current on the interval $\theta_1 \le \theta \le \theta_2$, found by integrating the inductor voltage with respect to θ, is given by

$$i_L(\theta) = \frac{V_p}{\omega_l L}\left[\cos\theta_1 - \cos\theta - \sin\theta_1(\theta - \theta_1)\right] \tag{3.3.4}$$

Substituting $i_L(\theta_2) = 0$ yields a transcendental relationship between angles θ_2 and θ_1 valid in dcm

$$\cos\theta_1 - \cos\theta_2 - \sin\theta_1(\theta_2 - \theta_1) = 0 \tag{3.3.5}$$

The critical angles for operation at the boundary between dcm and ccm can be found by finding the angle $\theta_{1,\text{crit}}$, for which angle $\theta_{2,\text{crit}} = \theta_{1,\text{crit}} + \pi$. Substitution in equation (3.3.5) gives

$$\theta_{1,\text{crit}} = \tan^{-1}\frac{2}{\pi} \tag{3.3.6}$$

The actual input current is the alternating periodic extension (see Appendix A) of the inductor current over the half-cycle $\theta_1 \le \theta \le \pi + \theta_1$. On this interval, the inductor current may be written in terms of the ideal current as

$$i_L(\theta) = \begin{cases} I_{ideal}\dfrac{\sqrt{2}}{\rho_L}\left[\cos\theta_1 - \cos\theta - \sin\theta_1(\theta - \theta_1)\right];\ \theta_1 \le \theta \le \theta_2 \\ 0\ ;\ \theta_2 \le \theta \le \pi + \theta_1 \end{cases} \tag{3.3.7}$$

where the normalized impedance ρ_L is given by

$$\rho_L \equiv \frac{\left|Z_L(j\omega_l)\right|}{R_{ideal}} = \frac{\omega_l L P}{V_{ideal}^2} \tag{3.3.8}$$

Equating the average inductor current over the half cycle with the output current,

$$\frac{1}{\pi}\int_{\theta_1}^{\theta_2} i_L(\theta)\, d\theta = \frac{P}{V_o} \tag{3.3.9}$$

establishes a relationship between normalized impedance ρ_L and angles θ_1 and θ_2:

$$\rho_L = \frac{2}{\pi}\sin\theta_1\left[\sin\theta_1 - \sin\theta_2 + (\theta_2 - \theta_1)\cos\theta_1 - \frac{1}{2}(\theta_2 - \theta_1)^2\sin\theta_1\right] \tag{3.3.10}$$

Substituting critical angles $\theta_{1,\text{crit}}$ and $\theta_{2,\text{crit}}$ in this equation gives the critical value of the normalized impedance ρ_L corresponding to operation at the boundary between dcm and ccm

$$\rho_{L,\text{crit}} = \frac{16}{\pi^3 + 4\pi} \cong 0.3672 \tag{3.3.11}$$

Hence, the filter operates in dcm with normalized impedance ρ_L in the range

$$0 < \rho_L < \frac{16}{\pi^3 + 4\pi} \Rightarrow \text{dcm} \tag{3.3.12}$$

and the range for which the filter operates in ccm remains to be determined.

3.3.2 Continuous Conduction Mode

The continuous conduction mode (ccm) is characterized by inductor current which is not zero over any finite interval. The input current is zero only at the instants when it crosses zero, and it is at these instants that commutation of the bridge rectifier takes place. Typical normalized voltage and current waveforms in ccm are shown in figure 3.10. The inductor current over the interval $\theta_1 \le \theta \le \pi + \theta_1$ is again found by integrating the fundamental *i-v* relationship for an inductor, equation (3.3.3), with respect to θ:

$$i_L(\theta) = \frac{V_p}{\omega_l L} \int_{\theta_1}^{\theta} (\sin\theta' - M_p)\, d\theta' \tag{3.3.13}$$

The condition that the current is zero at $\theta = \pi + \theta_1$ leads to the following relationship between the peak ac/dc conversion ratio and angle θ_1, valid in ccm

$$M_{p,\text{ccm}} = \frac{2}{\pi}\cos\theta_1 \tag{3.3.14}$$

The inductor current over the interval $\theta_1 \le \theta \le \pi + \theta_1$ can then be written in terms of the ideal current as

$$i_L(\theta) = I_{ideal} \frac{\sqrt{2}}{\rho_L}\left[\cos\theta_1 - \cos\theta - \frac{2}{\pi}\cos\theta_1(\theta - \theta_1)\right] \tag{3.3.15}$$

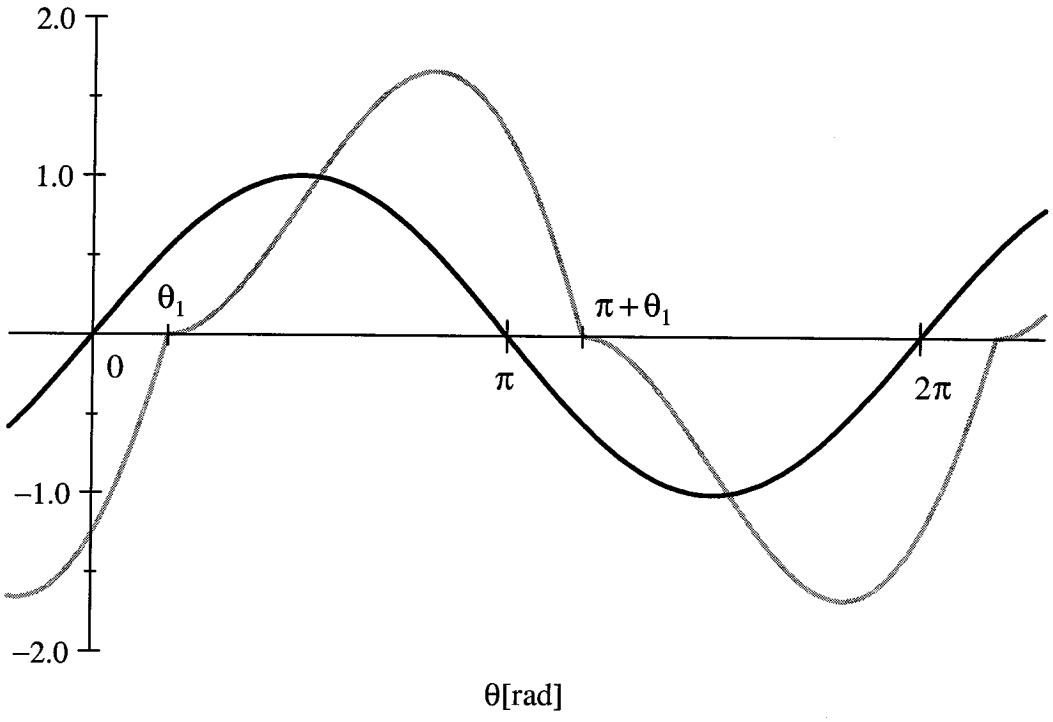


Figure 3.10: Normalized input current (grey) and input voltage (black) for the line-side inductor input filter operating in ccm ($\rho_L = 0.38$).

Equating the average inductor current over the half cycle with the output current

$$\frac{1}{\pi}\int_{\theta_1}^{\pi+\theta_1} i_L(\theta)\, d\theta = \frac{P}{V_o} \tag{3.3.16}$$

establishes an explicit relationship between the normalized impedance ρ_L and angle θ_1:

$$\rho_L = \frac{4}{\pi^2}\sin 2\theta_1 \tag{3.3.17}$$

From this result, it is clear that the maximum value of the normalized impedance ρ_L is

$$\rho_{L,\max} = \frac{4}{\pi^2} \cong 0.4053 \tag{3.3.18}$$

If ρ_L exceeds this limit, the circuit cannot operate properly. That is, the circuit is rendered incapable of delivering the required constant power P to the load, limited by the large impedance of the inductor in series with the input voltage.

At the boundary between dcm and ccm, we found the lowest value of ρ_L for which the filter operates in ccm. The upper bound is given by (3.3.18), and the very narrow range of ρ_L for which the filter operates in ccm is therefore

$$\frac{16}{\pi^3+4\pi} \le \rho_L \le \frac{4}{\pi^2} \Rightarrow \text{ccm} \tag{3.3.19}$$

and the filter cannot operate at all for larger values of ρ_L. Hence, the line-side inductor filter exhibits a phenomenon similar to the one observed for the capacitor filter—a critical value of the normalized impedance beyond which operation is not possible. In both cases, the constant power load is responsible for this behavior, but the cause in each case is different: For the capacitor filter, the output capacitor voltage drooping to zero renders the filter incapable of supplying constant power; For the line-side inductor filter, it is the impedance of the inductor in series with the ac source which effectively limits the available power.

Like the capacitor filter, the line-side inductor filter does not exhibit this behavior if the load is resistive. For resistive loads, the line-side inductor filter continues to operate for any value of load resistor, but is still effectively power limited by the impedance of the inductor in series with the ac source. Hence, the maximum power point with resistive load is achieved by choosing a resistor whose value corresponds to the same large-signal dc operating point as the constant power load, with $\rho_L = \rho_{L,\max}$. Using the results of this section, it can be shown that this resistor possesses the value

$$R_{\text{max power}} = \omega_l L \tag{3.3.20}$$

which, interestingly, is the identical result obtained by maximizing the ac power delivered to the resistor in a simple series linear *L-R* circuit driven by a sinusoidal ac voltage source.

3.3.3 Performance Characteristics

The performance characteristics of the line-side inductor filter, such as the ac/dc conversion ratio, input power factor, and input current harmonics, are again assessed as a function of the normalized impedance alone, just as was done for capacitor filter.

Conduction Angle

In dcm, transcendental relation (3.3.5) is used to solve for θ_2 given θ_1, with θ_1 in the range $\theta_{1,crit} < \theta_1 < \pi/2$. Equation (3.3.10) is then used to compute the normalized impedance ρ_L. In plotting, the process is reversed, and angles θ_1 and θ_2 are plotted as a function of normalized impedance ρ_L. In ccm, angle θ_1 is found by inverting equation (3.3.17), which gives

$$\theta_1 = \frac{1}{2}\sin^{-1}\left[\frac{\pi^2}{4}\rho_L\right] \tag{3.3.21}$$

Angle θ_2 is then simply

$$\theta_2 = \pi + \theta_1 \tag{3.3.22}$$

The results for operation in both dcm and ccm are plotted in figure 3.11.

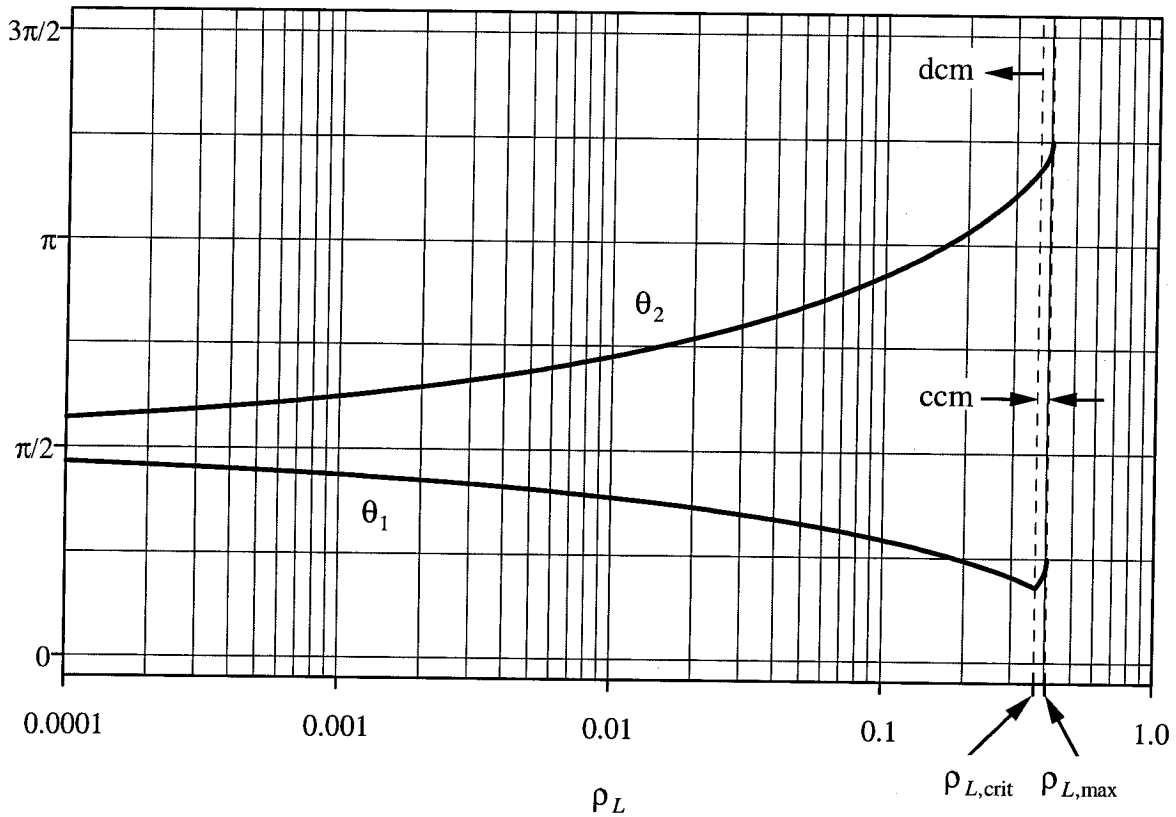


Figure 3.11 *Turn-on angle θ_1 and turn-off angle θ_2 as a function of normalized impedance ρ_L for the line-side inductor filter. Operation in the region beyond $\rho_L = \rho_{L,max}$ is not possible.*

Ac/Dc Conversion Ratio

With angle θ_1 known as a function of the normalized impedance ρ_L, it is a simple matter to derive the ac/dc conversion ratio. In dcm, equation (3.3.2) gives the peak ac/dc conversion ratio as a function of angle θ_1, which can then be plotted as a function of ρ_L. In ccm, the peak ac/dc conversion ratio is expressed as a function of θ_1 in equation (3.3.14), and angle θ_1 is expressed as a function of ρ_L in equation (3.3.20). Making use of a half-angle relation from trigonometry, the peak ac/dc conversion ratio in ccm can be written explicitly as a function of ρ_L:

$$M_{p,\mathrm{ccm}} = \frac{\sqrt{2}}{\pi}\sqrt{1+\sqrt{1-\left(\frac{\pi^2}{4}\rho_L\right)^2}} \qquad (3.3.23)$$

The results for operation in both dcm and ccm are plotted below in figure 3.12.

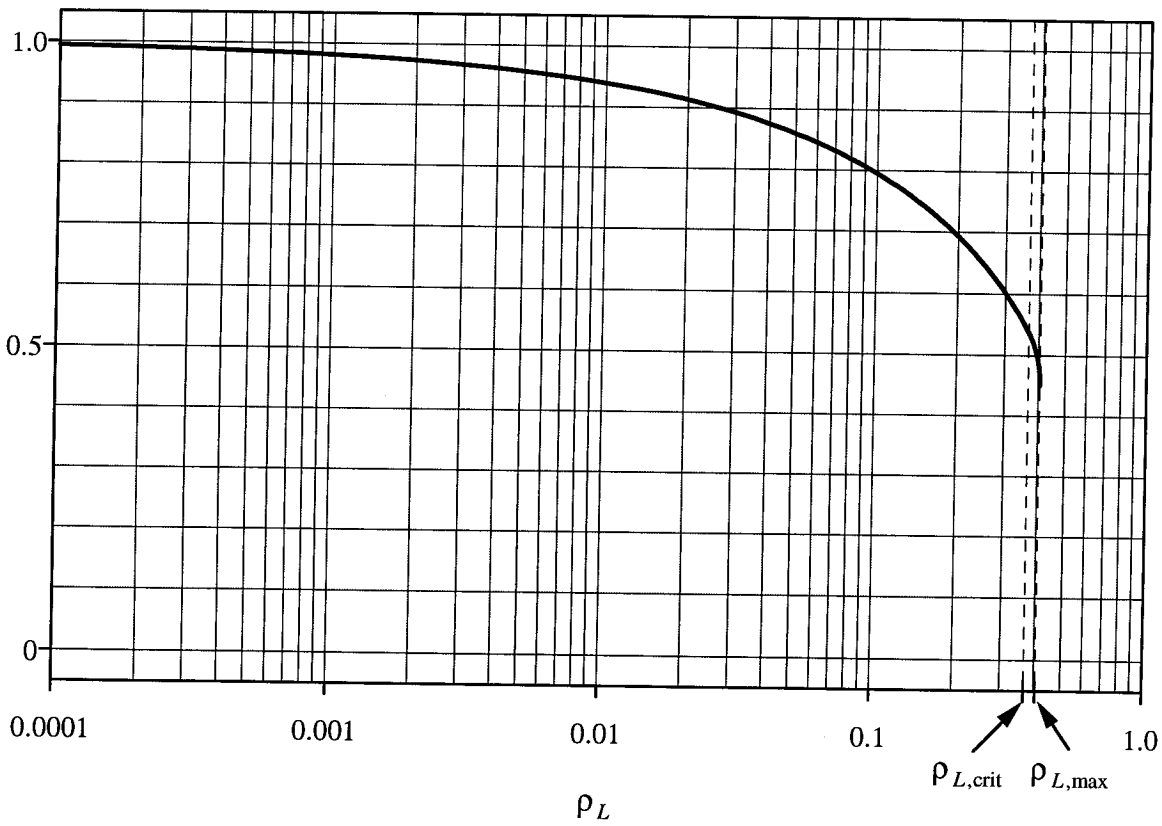


Figure 3.12: Peak ac/dc conversion ratio M_p as a function of normalized impedance ρ_L for the line-side inductor filter, for operation in both dcm and ccm.

Power Factor and Harmonics

The power factor and normalized input current harmonics can also be plotted as a function of normalized impedance ρ_L. First consider operation in dcm. The inductor current over the interval $\theta_1 \le \theta \le \pi + \theta_1$ is given by equation (3.3.7). The input current is the alternating periodic extension of the inductor current on this interval. Using the results of appendix A, the Fourier coefficients of the input current in dcm are, in integral form

$$a_{n,\mathrm{dcm}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\theta_2} i_L(\theta)\cos n\theta \, d\theta \; ; \; n \text{ odd} \\ 0 \; ; \; n \text{ even} \end{cases}$$

$$b_{n,\mathrm{dcm}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\theta_2} i_L(\theta)\sin n\theta \, d\theta \; ; \; n \text{ odd} \\ 0 \; ; \; n \text{ even} \end{cases} \qquad (3.3.24)$$

From these integrals, the Fourier coefficients of the fundamental component of the input current are given by

$$a_{1,\mathrm{dcm}} = I_{ideal}\frac{\sqrt{2}}{\pi\rho_L}\left[(\theta_1-\theta_2)(1+2\sin\theta_1\sin\theta_2)+\frac{1}{2}(\sin 2\theta_1-\sin 2\theta_2)+2\sin(\theta_2-\theta_1)\right]$$

$$b_{1,\mathrm{dcm}} = I_{ideal}\sqrt{2} \qquad (3.3.25)$$

The rms input current in dcm is

$$I_{rms,\mathrm{dcm}} = I_{ideal}\sqrt{\frac{2}{\pi}}\frac{1}{\rho_L}\left[\frac{1}{3}(\theta_2-\theta_1)^3\sin^2\theta_1+(\theta_2-\theta_1)\cos^2\theta_1+\frac{1}{2}(\theta_2-\theta_1)+\right.$$

$$\left.2(\theta_2-\theta_1)\sin\theta_1\sin\theta_2+\frac{1}{4}(\sin 2\theta_2-\sin 2\theta_1)-2\sin(\theta_2-\theta_1)-\frac{1}{2}(\theta_2-\theta_1)^2\sin 2\theta_1\right]^{\frac{1}{2}} \qquad (3.3.26)$$

Now consider operation in ccm. From appendix A, the Fourier coefficients of the input current are, in integral form

$$a_{n,\text{ccm}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\pi+\theta_1} i_L(\theta)\cos n\theta\, d\theta \ ; \ n \text{ odd} \\ 0 \ ; \ n \text{ even} \end{cases}$$

$$b_{n,\text{ccm}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\pi+\theta_1} i_L(\theta)\sin n\theta\, d\theta \ ; \ n \text{ odd} \\ 0 \ ; \ n \text{ even} \end{cases} \qquad (3.3.27)$$

The Fourier coefficients of the fundamental component of the input current are then

$$a_{1,\text{ccm}} = I_{ideal}\frac{\sqrt{2}}{\rho_L}\left[\frac{8}{\pi^2}\cos^2\theta_1 - 1\right]$$
$$b_{1,\text{ccm}} = I_{ideal}\sqrt{2} \qquad (3.3.28)$$

and the rms input current is given by

$$I_{rms,\text{ccm}} = I_{ideal}\frac{1}{\rho_L}\sqrt{1-\left[\frac{16}{\pi^2}-\frac{2}{3}\right]\cos^2\theta_1} \qquad (3.3.29)$$

where angle θ_1 is given as an explicit function of ρ_L in equation (3.3.21).

Using these results, the power factor, distortion factor, and displacement factor are computed using the results of chapter 2:

$$PF = \frac{I_{ideal}}{I_{rms}} \ ; \ DF = \frac{I_1}{I_{rms}} \ ; \ \cos\phi_1 = \frac{I_{ideal}}{I_1} \qquad (3.3.30)$$

and these results in both operating modes are plotted in figure 3.13.

The normalized input current harmonics

$$i_n = \frac{I_n}{I_{ideal}} \qquad (3.3.31)$$

are computed by evaluating equations (3.3.24) and (3.3.27) numerically, and the results are plotted in figure 3.14 as a function of the normalized impedance ρ_L.

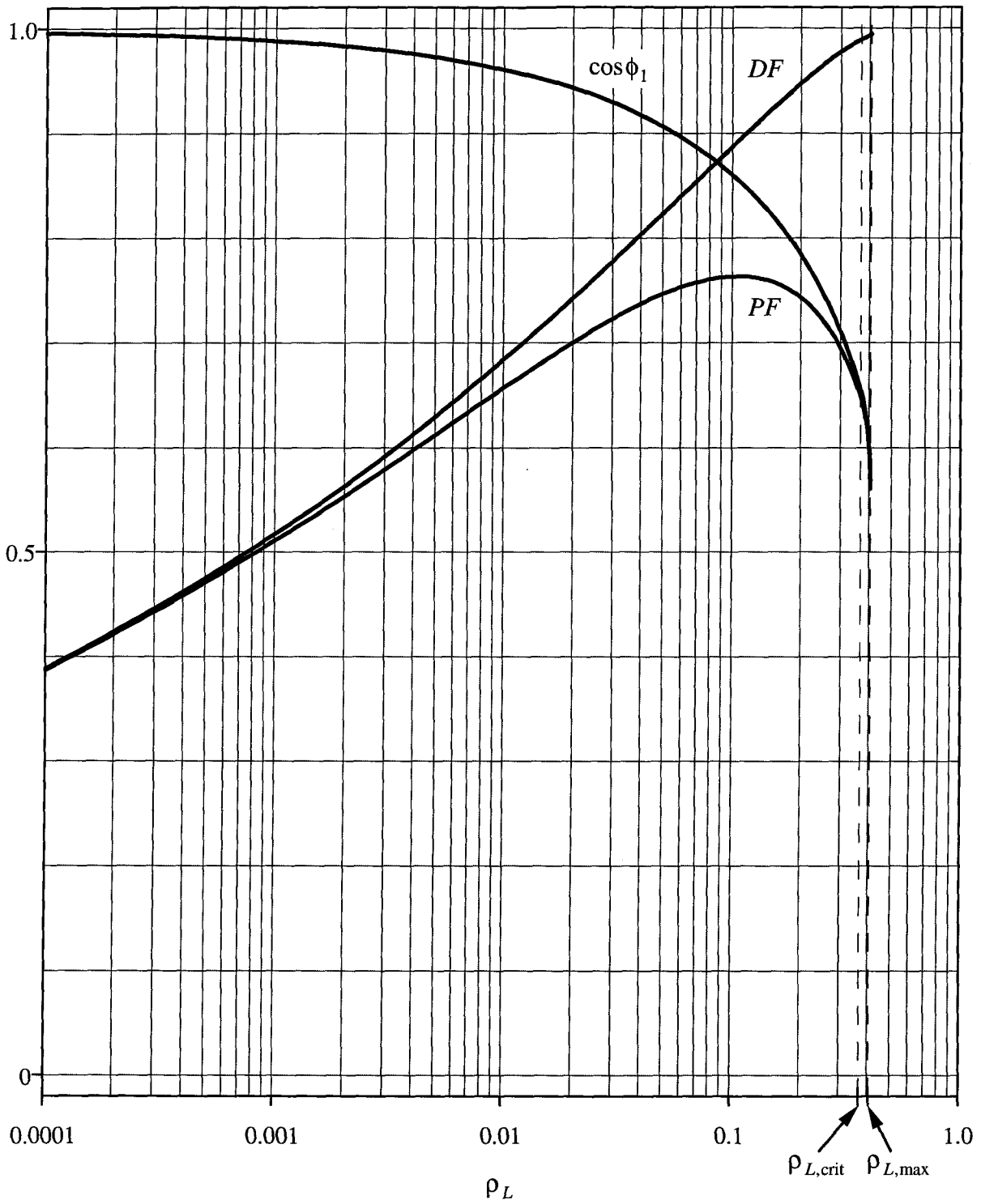


Figure 3.13: Power factor, distortion factor, and displacement factor for the line-side inductor filter as a function of normalized impedance ρ_L.

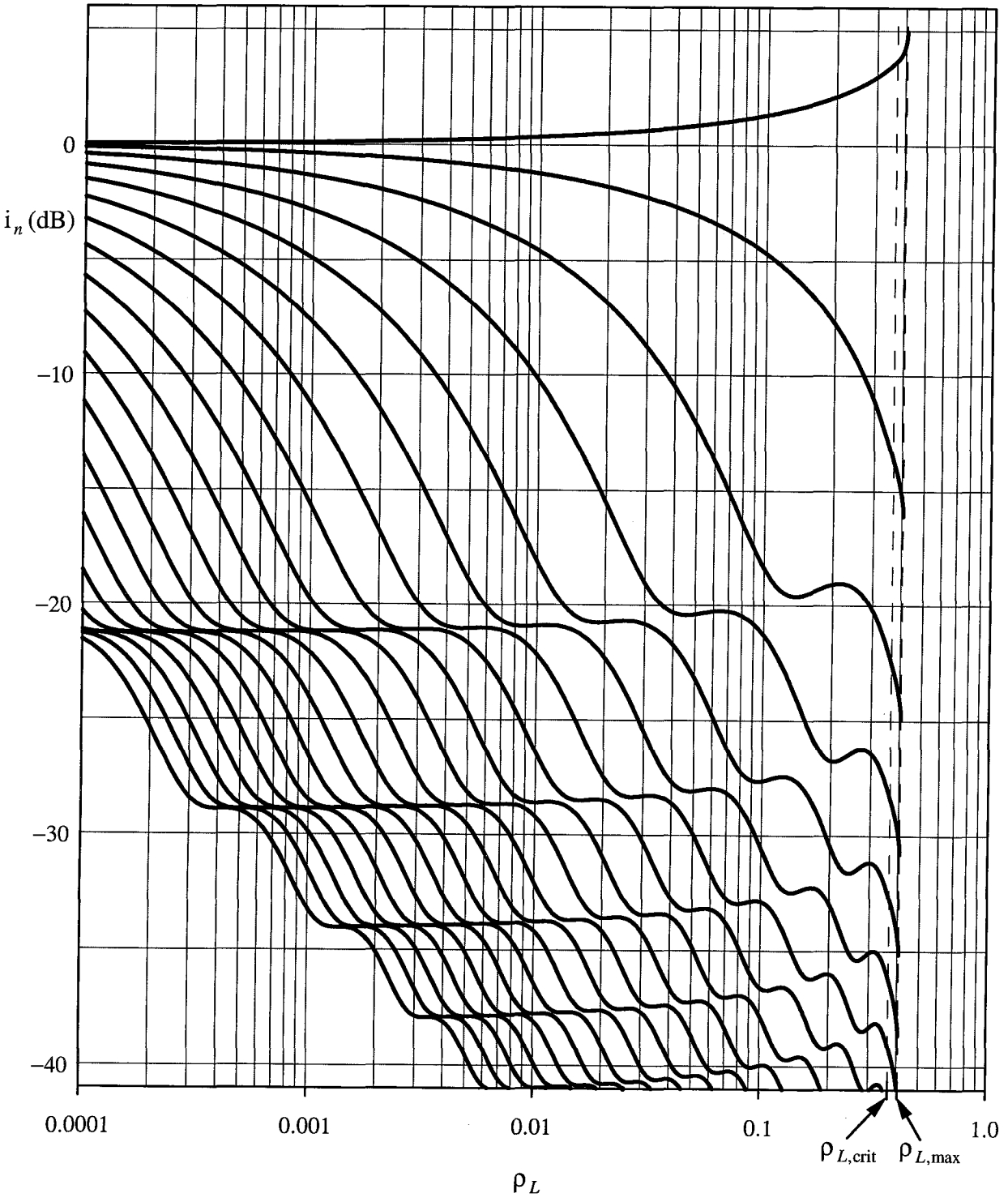


Figure 3.14: Normalized odd input current harmonics 1-39 as a function of normalized impedance ρ_L for the line-side inductor filter. The topmost curve is the fundamental, and odd harmonics 3-39 progress downward in order.

3.4 Load-Side Inductor Filter

It is shown in this section that the load-side inductor filter can behave either the same, or very different from the line-side inductor filter, depending upon the operating mode. The load-side inductor filter has three distinct operating modes, as opposed to two for the line-side inductor filter. These are: discontinuous conduction mode one (dcm1), discontinuous conduction mode two (dcm2), and the continuous conduction mode (ccm). Operation of the load-side filter in dcm1 is the same as operation of the line-side filter in dcm, except the range of operation in the load-side case is smaller. In contrast, operation of the load-side filter in dcm2 or ccm is unlike either operating mode of the line-side filter.

The key difference between operation of the load-side inductor filter and operation of the line-side inductor filter is the mechanism by which bridge rectifier commutation takes place. For the line-side inductor filter of the previous section, commutation occurs when the input *current* is zero. For the load-side inductor filter, commutation occurs when the input *voltage* is zero.

3.4.1 Continuous Conduction Mode

For the load-side inductor filter, the continuous conduction mode is characterized by inductor current which is never zero. This is different from the line-side inductor filter in ccm, where the inductor current has no dc component, and crosses zero as part of the normal ac cycle. For the load-side inductor filter in any operating mode, the inductor current has a dc component, and in ccm this component is large enough that the inductor current is never zero anywhere in the line cycle. Also, in any operating mode, the inductor current is unipolar, opening the possibility of pre-biasing the magnetic core in order to utilize the entire available core flux swing, thereby reducing the size of the inductor.

In ccm, the bridge rectifier is always conducting, and commutation of the bridge takes place when the input voltage crosses zero. The voltage waveform on the output side of the bridge rectifier is therefore a rectified sine wave, with peak voltage V_p. Since the average voltage across the inductor must be zero in steady-state, the dc output

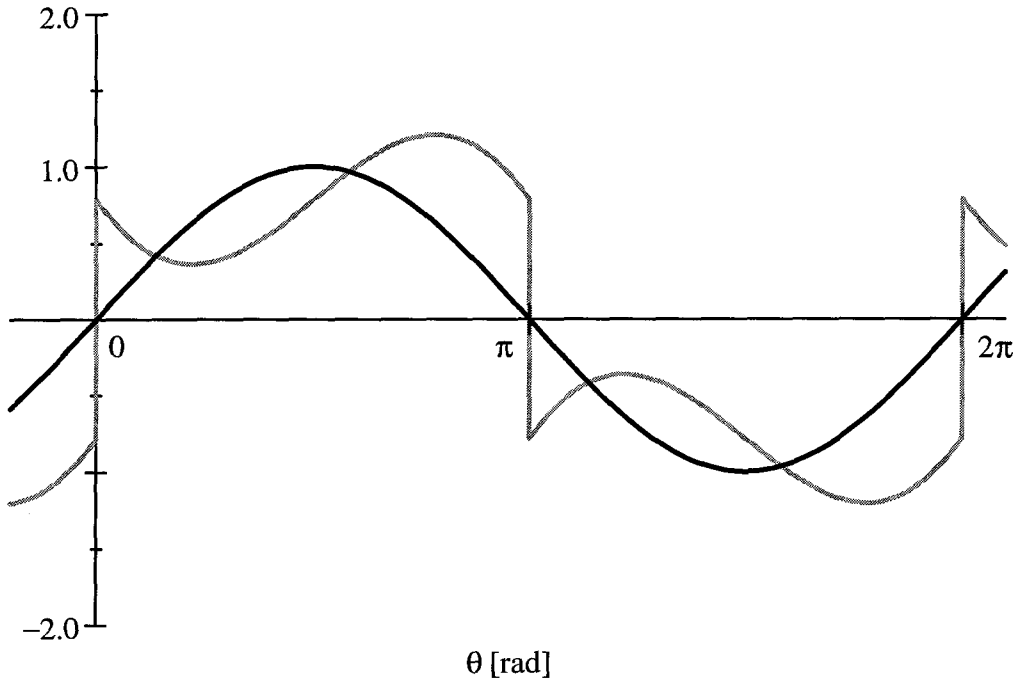


Figure 3.15: Normalized input voltage (black) and input current (grey) for the load-side inductor filter in ccm. ($\rho_L = 0.50$)

voltage must equal the average value of the rectified sine wave. Hence, the peak ac/dc conversion ratio is constant, given by

$$M_{p,\mathrm{ccm}} = \frac{2}{\pi} \tag{3.4.1}$$

The inductor current is again found by integrating the inductor voltage with respect to θ. The constant of integration is chosen to produce average output current $I_o = P/V_o$. This gives

$$i_L(\theta) = I_{ideal}\frac{\sqrt{2}}{\rho_L}\left[1 + \frac{\pi}{4}\rho_L - \cos\theta - \frac{2}{\pi}\theta\right] \tag{3.4.2}$$

for the complete half-cycle $0 \le \theta \le \pi$. The actual input current is the alternating periodic extension (appendix A) of this result, as illustrated in figure 3.15.

3.4.2 Discontinuous Conduction Mode One

For typical voltage and current waveforms for the load-side inductor filter in dcm1, refer to figure 3.9 for the line-side inductor filter. As in that example, provided that

angle $\theta_2 \leq \pi$, the operation of the two filters is identical. Angle $\theta_2 = \pi$ marks the boundary between the two operating modes dcm1 and dcm2. The critical value of angle θ_1, for which angle $\theta_2 = \pi$, can be determined from the transcendental relationship, equation (3.3.5):

$$\cos\theta_{1,\text{crit1}} + 1 - \sin\theta_{1,\text{crit1}}(\pi - \theta_1) = 0 \tag{3.4.3}$$

which is solved numerically and gives $\theta_{1,\text{crit1}} \cong 0.8105$ at the dcm1/dcm2 boundary. Using equation (3.3.10), the corresponding value of the normalized impedance at this boundary is $\rho_{L,\text{crit1}} \cong 0.1672$. Hence, the filter operates in dcm1 with the normalized impedance ρ_L in the range

$$0 < \rho_L \leq \rho_{L,\text{crit1}} \Rightarrow \text{dcm1} \tag{3.4.4}$$

The results from the analysis of the line-side filter in dcm apply to the load-side filter with ρ_L in this range, and are not repeated here.

3.4.3 Discontinuous Conduction Mode Two

As mentioned earlier, this mode is unlike either operating mode of the line-side inductor filter. Typical normalized input voltage and current waveforms for the load-side inductor filter operating in dcm2 are shown in figure 3.20. The relationship between the conversion ratio and angle θ_1 in dcm1 is still valid in dcm2:

$$M_{p,\text{dcm2}} = \sin\theta_1 \tag{3.4.5}$$

The inductor current is again found by integrating the voltage across the inductor with respect to θ. In the interval $\theta_1 \leq \theta < \pi$, the inductor voltage is given by the same expression as that in dcm1, and the inductor current in this interval is again given by equation (3.3.4). In the interval $\pi < \theta \leq \theta_2$, commutation of the bridge rectifier causes the polarity of the input voltage to reverse with respect to the inductor. Integrating the voltage across the inductor with respect to θ gives the inductor current for this interval, subject to the initial condition at $i_L(\pi)$, set forth by the end of the previous interval. Solving gives the inductor current over the complete half cycle $\theta_1 \leq \theta \leq \pi + \theta_1$:

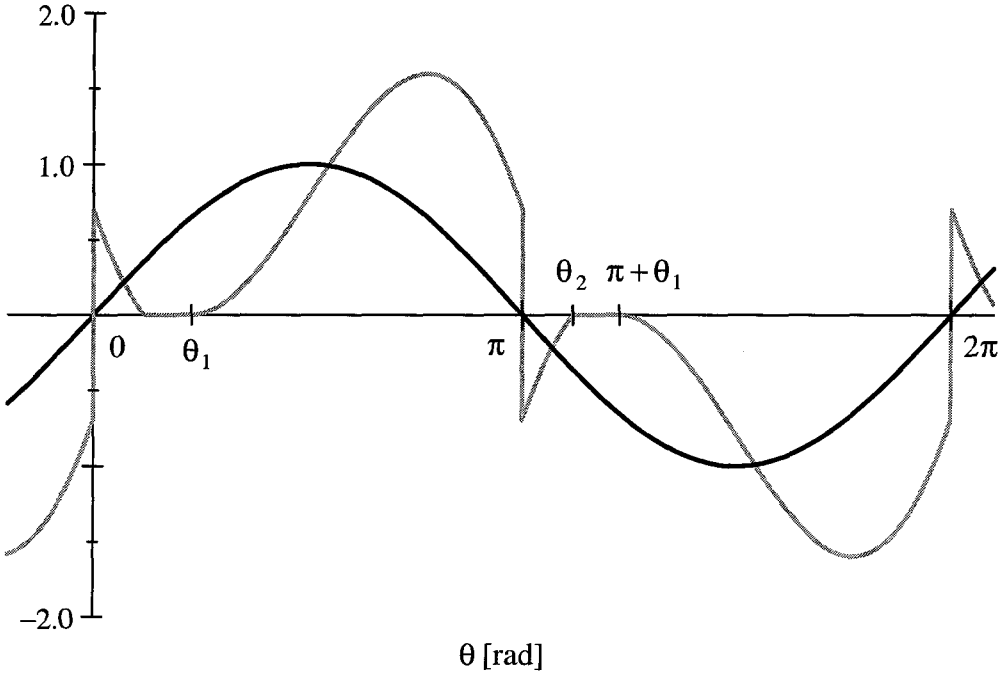


Figure 3.16: Normalized input voltage (black) and input current (grey) for the load-side inductor filter operating in dcm2. ($\rho_L = 0.23$)

$$i_L(\theta) = \begin{cases} I_{ideal}\dfrac{\sqrt{2}}{\rho_L}\left[\cos\theta_1 - \cos\theta - \sin\theta_1(\theta - \theta_1)\right] \;;\; \theta_1 \le \theta < \pi \\ I_{ideal}\dfrac{\sqrt{2}}{\rho_L}\left[\cos\theta_1 + \cos\theta - \sin\theta_1(\theta - \theta_1) + 2\right] \;;\; \pi < \theta \le \theta_2 \\ 0 \;;\; \theta_2 \le \theta \le \pi + \theta_1 \end{cases} \tag{3.4.6}$$

The transcendental relationship between angles θ_1 and θ_2 in dcm2 is found by setting $i_L(\theta_2) = 0$:

$$\cos\theta_1 + \cos\theta_2 - \sin\theta_1(\theta_2 - \theta_1) + 2 = 0 \tag{3.4.7}$$

Taking into account the commutation of the bridge rectifier, a complete half-cycle of the input current in dcm2 is given by

$$i(\theta)=\begin{cases} i_L(\theta)\ ;\ \theta_1 \le \theta < \pi \\ -i_L(\theta)\ ;\ \pi < \theta \le \theta_2 \\ 0\ ;\ \theta_2 \le \theta \le \pi+\theta_1 \end{cases} \tag{3.4.8}$$

and the actual input current is the alternating periodic extension (appendix A) of this result. Equating the output current with the average inductor current establishes the relationship between normalized impedance ρ_L and angles θ_1 and θ_2 in dcm2:

$$\rho_L = \frac{2}{\pi}\sin\theta_1\left[\sin\theta_1+\sin\theta_2+(\theta_2-\theta_1)\cos\theta_1-\frac{1}{2}(\theta_2-\theta_1)^2\sin\theta_1+2(\theta_2-\pi)\right] \tag{3.4.9}$$

To find the value of ρ_L at the dcm2/ccm boundary, equate the expressions for the peak ac/dc conversion ratio, since both must be valid at the boundary between the modes. This gives

$$\theta_{1,\text{crit2}} = \sin^{-1}\frac{2}{\pi} \tag{3.4.10}$$

Also at the dcm2/ccm boundary, angle $\theta_{2,\text{crit}}$ is given by

$$\theta_{2,\text{crit2}} = \pi+\theta_{1,\text{crit2}} \tag{3.4.11}$$

Substituting these angles in equation (3.4.9) gives the critical value of ρ_L at the dcm2/ccm boundary

$$\rho_{L,crit2} = \frac{4}{\pi}\left[\sqrt{1-\frac{4}{\pi^2}}+\frac{2}{\pi}\sin^{-1}\frac{2}{\pi}-1\right] \cong 0.2680 \tag{3.4.12}$$

Hence, the filter operates in dcm2 with ρ_L in the range

$$\rho_{L,\text{crit1}} < \rho_L < \rho_{L,\text{crit2}} \tag{3.4.13}$$

and operates in ccm with $\rho_L \ge \rho_{L,\text{crit2}}$.

3.4.4 Performance Characteristics

Like the previous filters studied, the performance characteristics of the load-side inductor filter can be assessed as a function of the normalized impedance parameter. Unlike the previous two filters, operation of the load-side inductor filter with a resistive

load is quite similar to operation with a constant power load. That is, for a given operating condition with the constant power load, a resistor can be chosen which preserves the large-signal dc operating point at the output. With this resistor as a load, the performance characteristics are unchanged from those with the constant power load.

Conduction Angle

In either of the discontinuous modes, angle θ_1 is the angle at which the inductor current begins to flow, and θ_2 is the angle at which the inductor current terminates. In ccm, the inductor current flows continuously, leaving angles θ_1 and θ_2 undefined. These angles are plotted in figure 3.17 as a function of the normalized impedance ρ_L, for operation in dcm1 and dcm2.

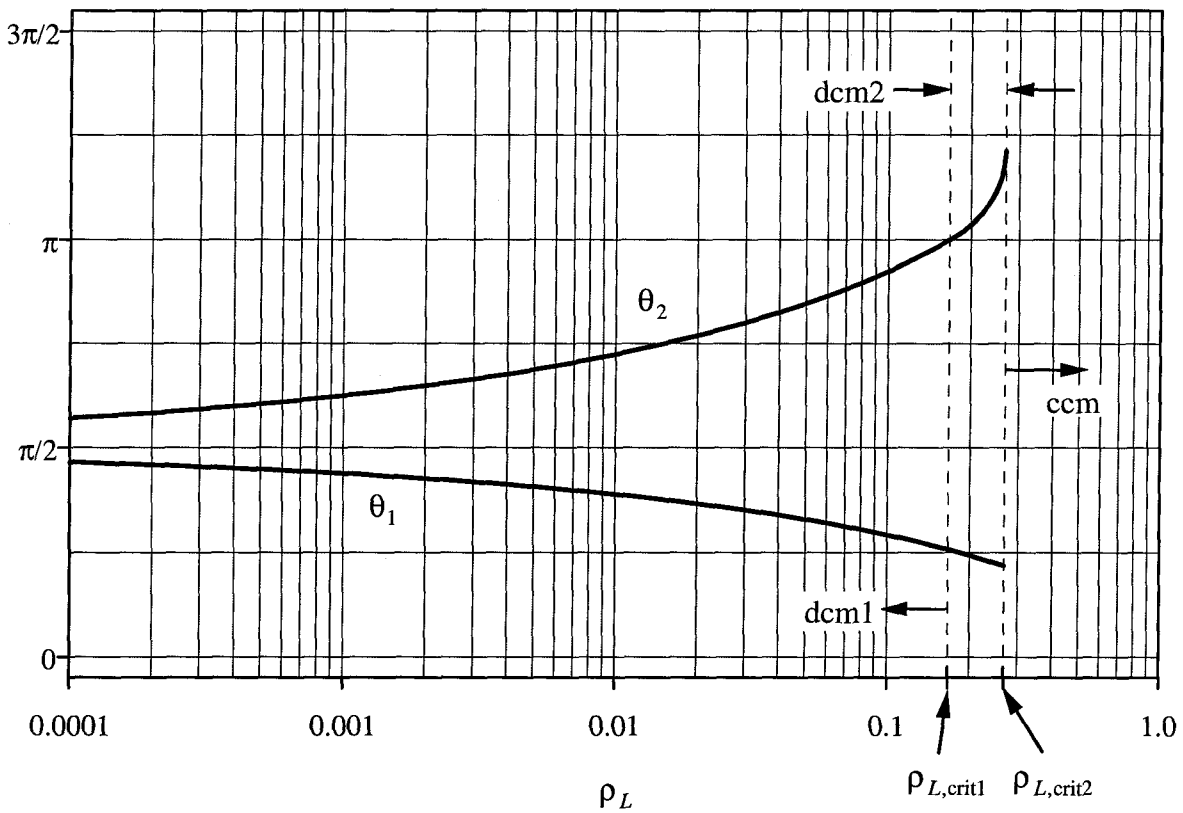


Figure 3.17: Turn-on angle θ_1 and turn-off angle θ_2 for the load-side inductor filter as a function of normalized impedance ρ_L. These angles are undefined in ccm, since the bridge conducts continuously.

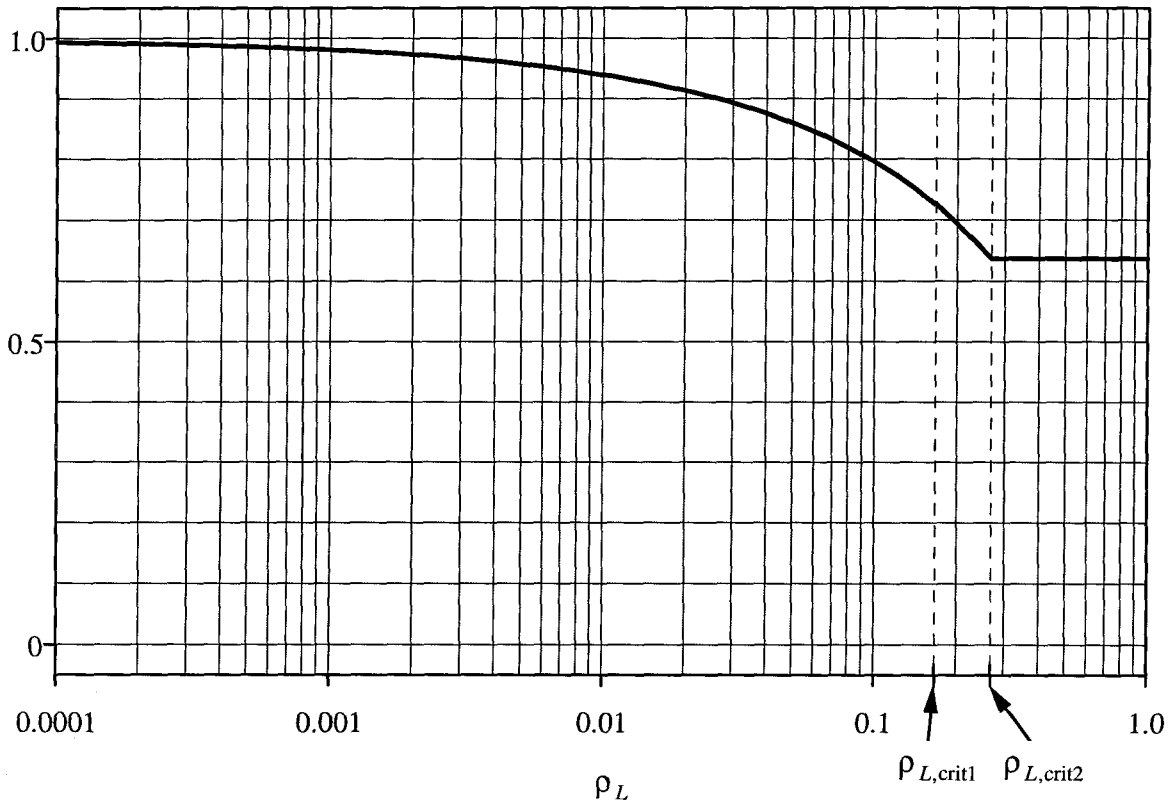


Figure 3.18: Peak ac/dc conversion ratio M_p as a function of the normalized impedance ρ_L for the load-side inductor filter in all three operating modes.

Ac/Dc Conversion Ratio

The peak ac/dc conversion ratio M_p is given by equations (3.3.2), (3.4.5), and (3.4.1) for operation in dcm1, dcm2, and ccm, respectively. It is plotted in figure 3.18 as a function of the normalized impedance ρ_L.

Power Factor and Harmonics

The power factor and input current harmonics of the load-side inductor filter in dcm1 are the same as those of the line-side inductor filter in dcm, over the entire dcm1 operating range. In dcm2, taking into account commutation of the bridge rectifier at $\theta = \pi$, the Fourier coefficients of the input current waveform are given by

$$a_{n,\mathrm{dcm2}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\pi} i_L(\theta)\cos n\theta\, d\theta - \dfrac{2}{\pi}\int_{\pi}^{\theta_2} i_L(\theta)\cos n\theta\, d\theta \;\; ; \;\; n \text{ odd} \\ 0 \;\; ; \;\; n \text{ even} \end{cases}$$

$$b_{n,\mathrm{dcm2}} = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_{\theta_1}^{\pi} i_L(\theta)\sin n\theta\, d\theta - \dfrac{2}{\pi}\int_{\pi}^{\theta_2} i_L(\theta)\sin n\theta\, d\theta \;\; ; \;\; n \text{ odd} \\ 0 \;\; ; \;\; n \text{ even} \end{cases} \qquad (3.4.14)$$

The Fourier coefficients of the fundamental component of the input current are then

$$a_{1,\mathrm{dcm2}} = I_{ideal}\frac{\sqrt{2}}{\pi\rho_L}\Big[(\theta_2-\theta_1)(2\sin\theta_1\sin\theta_2-1) - 4(\sin\theta_2-\sin\theta_1) - \frac{1}{2}(\sin 2\theta_2 - \sin 2\theta_1) - 2\sin(\theta_2-\theta_1)\Big] \qquad (3.4.15)$$

$$b_{1,\mathrm{dcm2}} = I_{ideal}\sqrt{2}$$

and the rms input current is given by the formidable expression

$$I_{rms,\mathrm{dcm2}} = I_{ideal}\sqrt{\frac{2}{\pi}\frac{1}{\rho_L}\Big[\theta_2-\theta_1+\frac{1}{3}(\theta_2-\theta_1)^3\sin^2\theta_1 + 4(\theta_2-\pi)(1+\cos\theta_1) + \frac{1}{2}(\theta_2-\theta_1)\cos 2\theta_1 - 2(\theta_2-\theta_1)\sin\theta_1\sin\theta_2 - 2((\theta_2-\theta_1)^2-(\pi-\theta_1)^2)\sin\theta_1 + 4(\sin\theta_2-\sin\theta_1) - \frac{1}{2}(\theta_2-\theta_1)^2\sin 2\theta_1 + 2\sin(\theta_2-\theta_1) + \frac{1}{4}(\sin 2\theta_2 - \sin 2\theta_1)\Big]^{\frac{1}{2}}} \qquad (3.4.16)$$

In ccm, the Fourier coefficients of the fundamental component of the input current are given by the comparatively simple expressions

$$a_{1,\mathrm{ccm}} = I_{ideal}\frac{\sqrt{2}}{\rho_L}\left[\frac{8}{\pi^2}-1\right]$$

$$b_{1,\mathrm{ccm}} = I_{ideal}\sqrt{2} \qquad (3.4.17)$$

and the Fourier coefficients of the higher harmonics can also be written in closed form

$$\left.\begin{aligned} a_{n,\mathrm{ccm}} &= I_{ideal}\,\frac{\sqrt{2}}{\rho_L}\,\frac{8}{\pi^2 n^2} \\ b_{n,\mathrm{ccm}} &= I_{ideal}\,\frac{\sqrt{2}}{n} \end{aligned}\right\} n = 3,5,7,\ldots \qquad (3.4.18)$$

The rms input current in ccm is given by

$$I_{rms,\mathrm{ccm}} = I_{ideal}\,\frac{\pi}{2\sqrt{2}}\sqrt{1+\frac{\frac{40}{3\pi^2}-\frac{128}{\pi^4}}{\rho_L^2}} \qquad (3.4.19)$$

From these results, the power factor, distortion factor, and displacement factor are computed using the usual formulas

$$PF = \frac{I_{ideal}}{I_{rms}} \;;\; DF = \frac{I_1}{I_{rms}} \;;\; \cos\phi_1 = \frac{I_{ideal}}{I_1} \qquad (3.4.20)$$

The simplicity of the results in ccm allows these expressions to be written in closed form, as a function of normalized impedance ρ_L.

$$PF = \frac{2\sqrt{2}}{\pi}\,\frac{1}{\sqrt{1+\frac{\frac{40}{3\pi^2}-\frac{128}{\pi^4}}{\rho_L^2}}} \qquad DF = \frac{2\sqrt{2}}{\pi}\sqrt{\frac{1+\frac{\left[\frac{8}{\pi^2}-1\right]^2}{\rho_L^2}}{1+\frac{\frac{40}{3\pi^2}-\frac{128}{\pi^4}}{\rho_L^2}}} \qquad (3.4.21)$$

$$\cos\phi_1 = \frac{1}{\sqrt{1+\frac{\left[\frac{8}{\pi^2}-1\right]^2}{\rho_L^2}}}$$

In dcm2, the power factor, distortion factor, and displacement factor are evaluated using equations (3.4.15) and (3.4.16). These results for all three operating modes are plotted in figure 3.19. The normalized input current harmonics for all three operating modes are plotted in figure 3.20. Because of the radical change that occurs, a magnified view of the harmonics around the dcm2 operating region is given in figure 3.21.

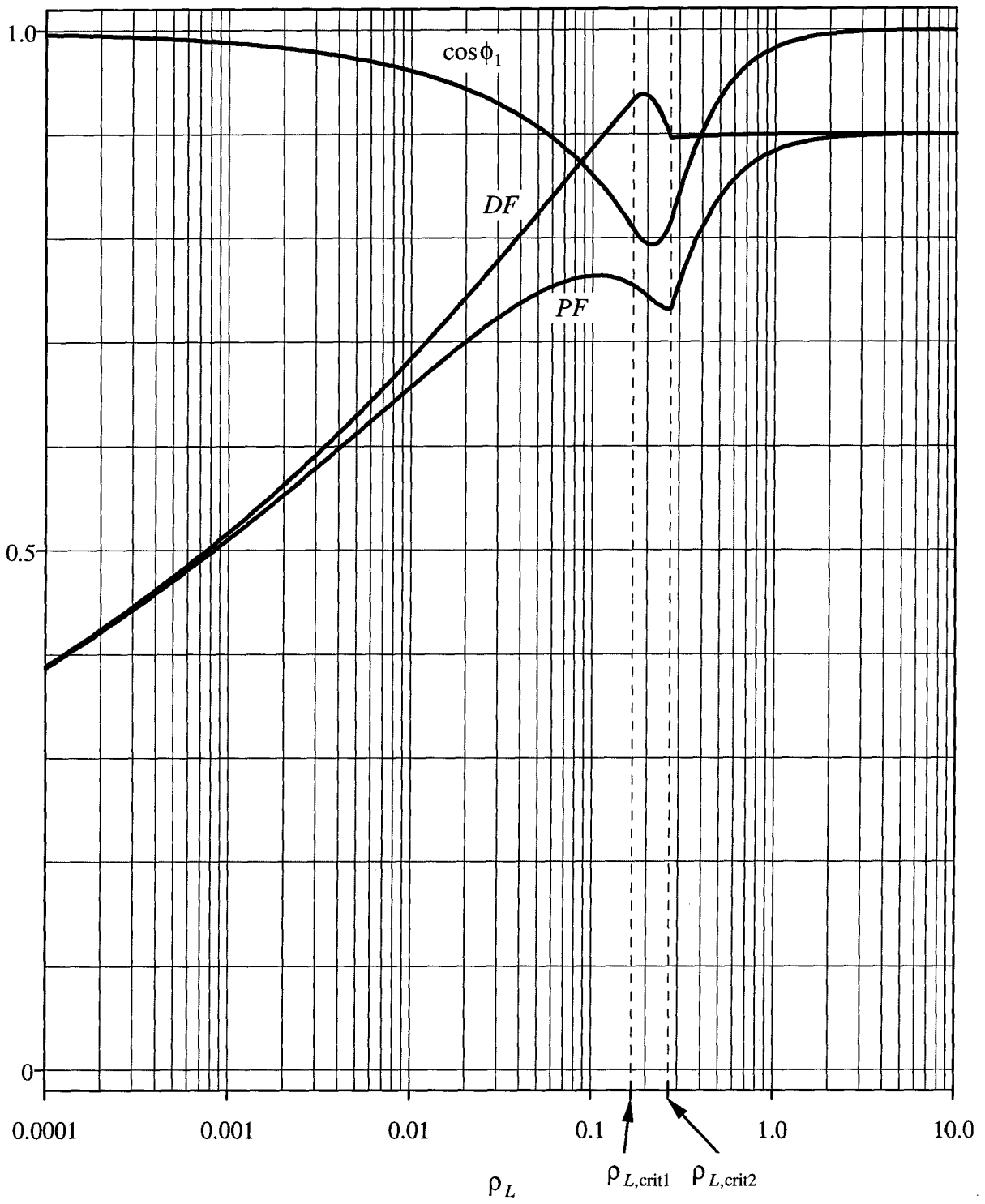


Figure 3.19: Power factor, distortion factor, and displacement factor for the load-side inductor filter as a function of normalized impedance ρ_L.

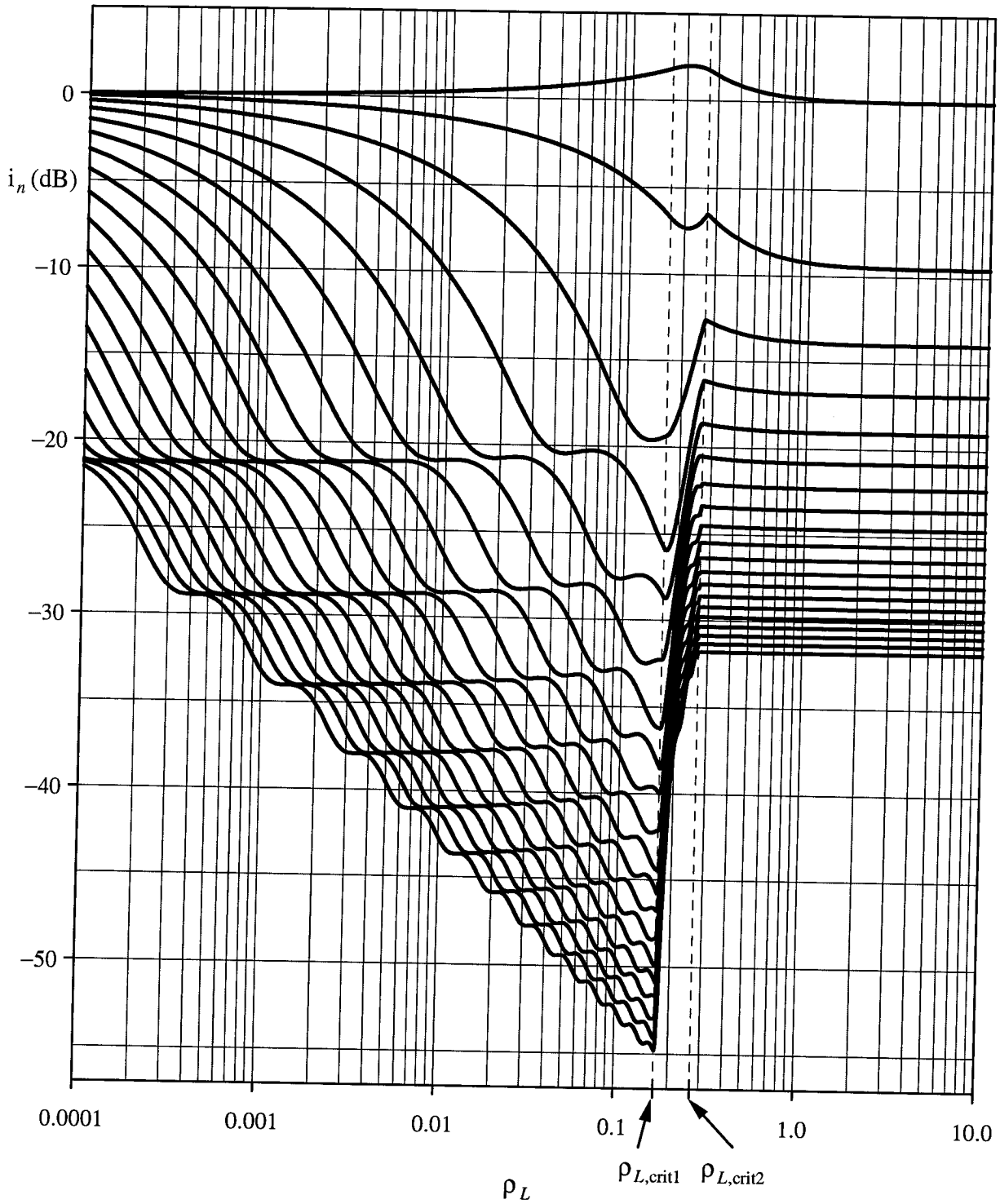


Figure 3.20: Normalized odd input current harmonics 1-39 for the load-side inductor filter as a function of normalized impedance ρ_L. The topmost curve is the fundamental, and odd harmonics 3-39 progress downward in order.

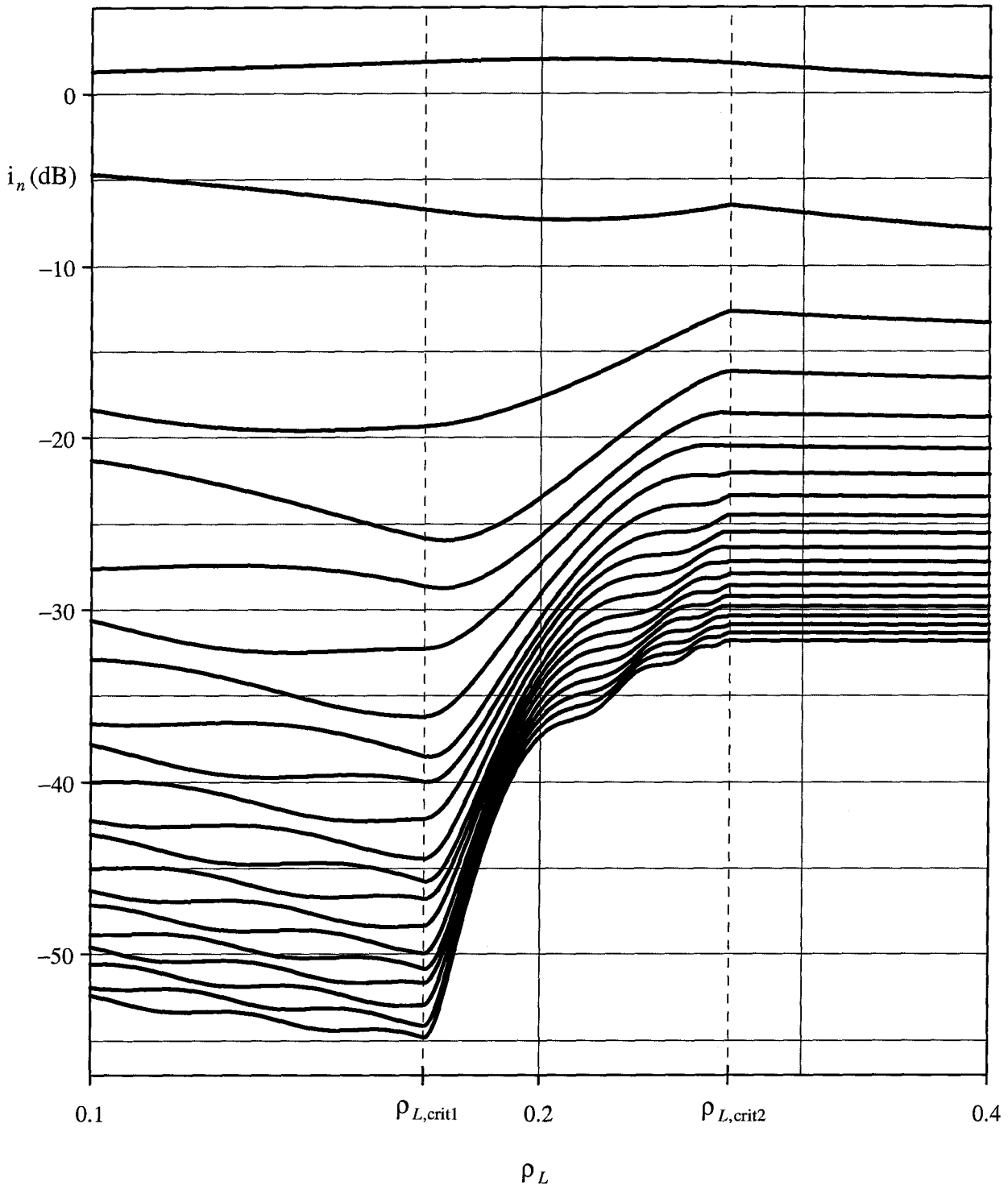


Figure 3.21: Expanded plot of the normalized odd input current harmonics around the dcm2 region of operation for the load-side inductor filter. The topmost curve is the fundamental, and odd harmonics 3-39 progress downward.

3.5 Resonant Filter

The resonant filter possesses the interesting property that the power factor can be made arbitrarily close to unity, achieving unity power factor in the limiting case of infinite resonant inductance. The resonant filter is shown below in figure 3.22. The circuit resembles the line-side inductor filter, with a capacitor added in series to resonate with the inductor. The resonant capacitor and inductor values are chosen such the resonant frequency and the line frequency are equal

$$\omega_l = \omega_0 = \frac{1}{\sqrt{LC}} \tag{3.5.1}$$

Since the resonant component values are constrained by this equation, there is only one degree of freedom in choosing these values. Qualitatively, it is the purpose of the resonant "tank" to promote the conduction of current at the line-frequency, and to oppose the conduction of current at the higher harmonic frequencies. The "characteristic resistance" R_0 of the resonant circuit is defined

$$R_0 \equiv \sqrt{\frac{L}{C}} = \omega_0 L = \frac{1}{\omega_0 C} \tag{3.5.2}$$

The normalized impedance for the resonant filter is the ratio

$$\rho_R = \frac{R_0}{R_{ideal}} \tag{3.5.3}$$

and the performance characteristics of this filter can be assessed as a function of this parameter alone. The output capacitor is assumed to be large enough that the output voltage may be considered constant.

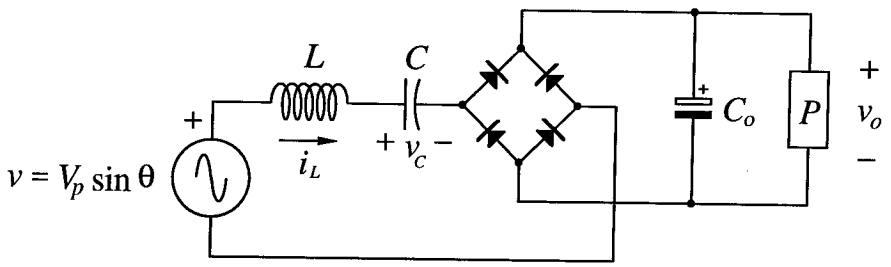


Figure 3.22: Resonant filter.

The resonant filter has two operating modes, called the continuous conduction mode (ccm) and the discontinuous conduction mode (dcm). In ccm, the bridge rectifier is always conducting, and in dcm, the bridge is open for part of the line cycle. In ccm, the input current harmonics are very small, but for low frequency utility line applications, operation in this mode requires a large resonant inductor.

3.5.1 Continuous Conduction Mode

In ccm, the bridge rectifier conducts continuously, with commutation taking place every half-cycle. The voltage on the ac side of the bridge is therefore a square wave with (normalized) period 2π, and peak amplitude equal to the output voltage. An equivalent circuit in ccm is shown below in figure 3.23. The fundamental component of the voltage across the LC section must be zero, since the impedance of this section at the fundamental frequency is zero. Hence, the fundamental component of each voltage source in the equivalent circuit must be equal in both magnitude and phase. The square wave voltage, v_{bridge}, is therefore in exact time phase with the input voltage, and admits a Fourier series representation of the form

$$v_{bridge}(\theta) = V_o \frac{4}{\pi} \sum_{n=1,3,5,\ldots} \frac{1}{n} \sin n\theta \tag{3.5.4}$$

Equating the amplitude of the fundamental component of the square wave with the amplitude of the sinusoidal input voltage, the peak ac/dc conversion ratio in ccm is

$$M_{p,\mathrm{ccm}} = \frac{\pi}{4} \tag{3.5.5}$$

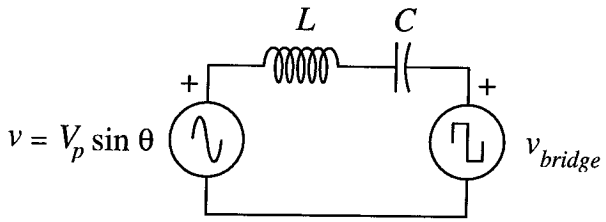


Figure 3.23: Equivalent circuit for the resonant filter in ccm. The input side of the bridge rectifier presents a square wave voltage to the input circuit.

The current during the interval $0 \le \theta \le \pi$ is described by the second order differential equation

$$i_L'' + i_L = \frac{V_p}{R_0}\cos\theta \tag{3.5.6}$$

Homogeneous solutions are of the form

$$i_{L,h} = A\cos\theta + B\sin\theta \tag{3.5.7}$$

where A and B are constants to be determined. A particular solution is

$$i_{L,p} = \frac{V_p}{2R_0}\theta\sin\theta \tag{3.5.8}$$

From the initial condition $i_L(0) = 0$, constant A is zero. A second condition is derived by equating average inductor current and the output current over a half cycle

$$\frac{1}{\pi}\int_0^{\pi} i_L(\theta)d\theta = \frac{P}{V_o} \tag{3.5.9}$$

Applying this condition, constant B is found to be

$$B = \frac{\pi}{2}\left[\frac{P}{V_o} - \frac{V_p}{2R_0}\right] \tag{3.5.10}$$

The total solution may then be written in terms of the ideal current

$$i_L(\theta) = I_{ideal}\sqrt{2}\left[1 - \frac{\pi}{4\rho_R} + \frac{\theta}{2\rho_R}\right]\sin\theta \tag{3.5.11}$$

In order to maintain conduction of the bridge rectifier in ccm, this current must remain positive throughout the entire half cycle $0 \le \theta \le \pi$. Since $i_L(0) = 0$, it is also necessary that

$$i_L'(0) \ge 0 \tag{3.5.12}$$

to maintain operation in ccm. Equality occurs at the critical boundary between dcm and ccm. Differentiating the expression for the inductor current, equation (3.5.11), and applying this condition gives the critical value of ρ_R at the dcm/ccm boundary

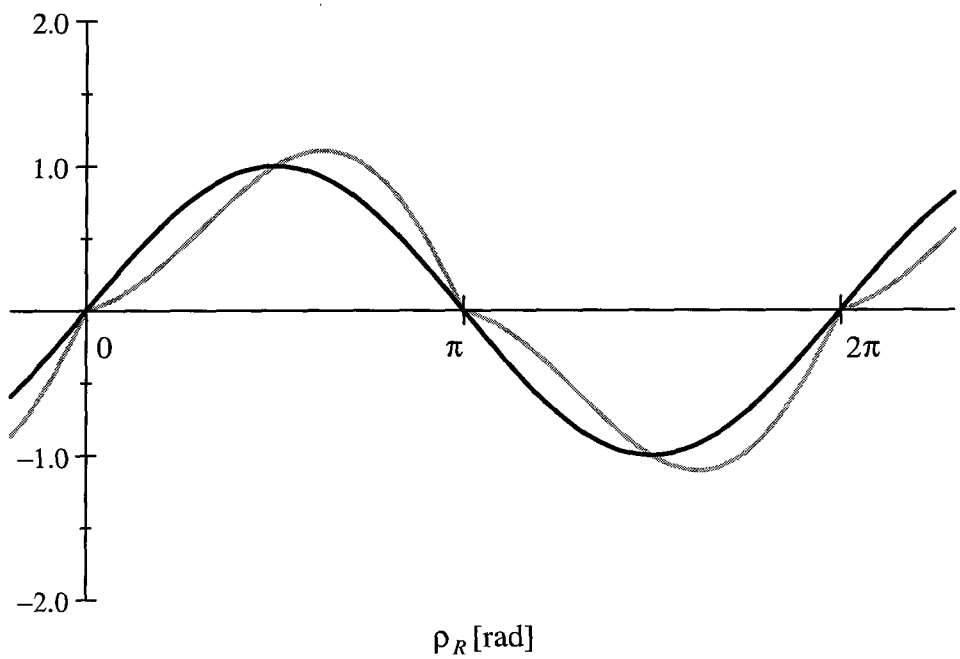


Figure 3.24: Normalized input voltage (black) and input current (grey) for the resonant filter in ccm. ($\rho_R = 1.0$)

$$\rho_{R,\text{crit}} = \frac{\pi}{4} \cong 0.7854 \tag{3.5.13}$$

Hence, the filter operates in ccm when $\rho_R \geq \rho_{R,\text{crit}}$, and in dcm when $\rho_R < \rho_{R,\text{crit}}$.

3.5.2 Discontinuous Conduction Mode

In dcm, the bridge rectifier is open for part of the line cycle. Let θ_1 be the angle at which the bridge starts to conduct. While the bridge is conducting, the inductor current is again described by differential equation (3.5.6). However, the initial conditions in this case are different, given by

$$\begin{aligned} i_L(\theta_1) &= 0 \\ i_L'(\theta_1) &= 0 \end{aligned} \tag{3.5.14}$$

The second condition is derived from the fundamental *i-v* relationship for an inductor, by realizing that at $\theta = \theta_1$, the voltage across the inductor is zero, and the result follows. Starting from the same homogeneous and particular solutions as those for the ccm case, initial conditions (3.5.14) give constants A and B for operation in dcm

$$A = \frac{V_p}{2R_0}\sin^2\theta_1$$
$$B = -\frac{V_p}{2R_0}(\theta_1 + \sin\theta_1\cos\theta_1) \tag{3.5.15}$$

The inductor current in dcm over the interval $\theta_1 \le \theta \le \theta_2$ may then be written

$$i_L(\theta) = \frac{V_p}{2R_0}\left[(\theta - \theta_1)\sin\theta - \sin\theta_1\sin(\theta - \theta_1)\right] \tag{3.5.16}$$

Setting $i_L(\theta_2) = 0$ gives the transcendental relation between angles θ_1 and θ_2 in dcm

$$(\theta_2 - \theta_1)\sin\theta_2 - \sin\theta_1\sin(\theta_2 - \theta_1) = 0 \tag{3.5.17}$$

To find the conversion ratio in dcm, the resonant capacitor voltage needs to be determined. The capacitor voltage is found from the integral

$$v_C(\theta) = v_C(\theta_1) + \frac{1}{\omega_l C}\int_{\theta_1}^{\theta} i_L(\theta')d\theta' \tag{3.5.18}$$

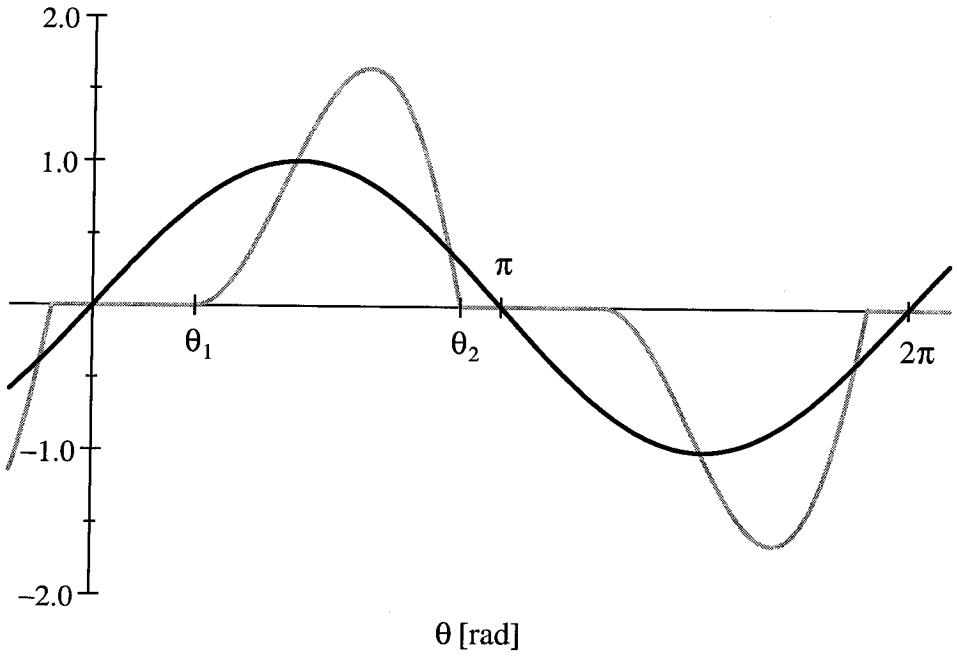


Figure 3.25 Normalized input voltage (black) and input current (grey) for the resonant filter in dcm. ($\rho_R = 0.16$)

The alternating periodic nature of the system requires that in steady-state

$$v_C(\theta_2) = -v_C(\theta_1) \tag{3.5.19}$$

Performing the integration, we find

$$v_C(\theta) = \frac{V_p}{4}\Big[\sin\theta_1\big(2\cos(\theta-\theta_1) - \cos(\theta_2-\theta_1) - 2\big) - 2(\theta-\theta_1)\cos\theta + 2\sin\theta + (\theta_2-\theta_1)\cos\theta_2 - \sin\theta_2\Big] \tag{3.5.20}$$

and evaluating at $\theta = \theta_1$:

$$v_C(\theta_1) = \frac{V_p}{4}\Big[(\theta_2-\theta_1)\cos\theta_2 - \sin\theta_1\big(\cos(\theta_2-\theta_1) - 2\big) - \sin\theta_2\Big] \tag{3.5.21}$$

At $\theta = \theta_1$, the bridge rectifier just turns on, and the voltage across the inductor at this instant is zero. Thus, the output voltage is given by

$$V_o = V_p \sin\theta_1 - v_C(\theta_1) \tag{3.5.22}$$

which is solved to give the peak ac/dc conversion ratio in terms of angles θ_1 and θ_2:

$$M_p = \frac{1}{4}\Big[\sin\theta_1\big(\cos(\theta_2-\theta_1) + 2\big) + \sin\theta_2 - (\theta_2-\theta_1)\cos\theta_2\Big] \tag{3.5.23}$$

Equating the average inductor current over a half cycle with the output current

$$\frac{1}{\pi}\int_{\theta_1}^{\theta_2} i_L(\theta)\,d\theta = \frac{P}{V_o} \tag{3.5.24}$$

establishes the relationship between normalized impedance ρ_R and angles θ_1 and θ_2, valid in dcm

$$\rho_R = \frac{1}{4\pi}\Big[\sin\theta_1\big(\cos(\theta_2-\theta_1) + 2\big) + \sin\theta_2 - (\theta_2-\theta_1)\cos\theta_2\Big] \times \Big[\sin\theta_1\big(\cos(\theta_2-\theta_1) - 2\big) + \sin\theta_2 - (\theta_2-\theta_1)\cos\theta_2\Big] \tag{3.5.25}$$

3.5.3 Performance Characteristics

As with the other passive filters studied, the performance characteristics are assessed as a function of the normalized impedance.

Conduction Angle

In dcm, angles θ_1 and θ_2 are found as a function of normalized impedance ρ_L by solving equations (3.5.17) and (3.5.25) numerically. When operating in ccm, angle θ_1 equals zero and angle θ_2 equals π, regardless of the value of the normalized impedance ρ_L. The results in both operating modes are plotted below in figure 3.26.

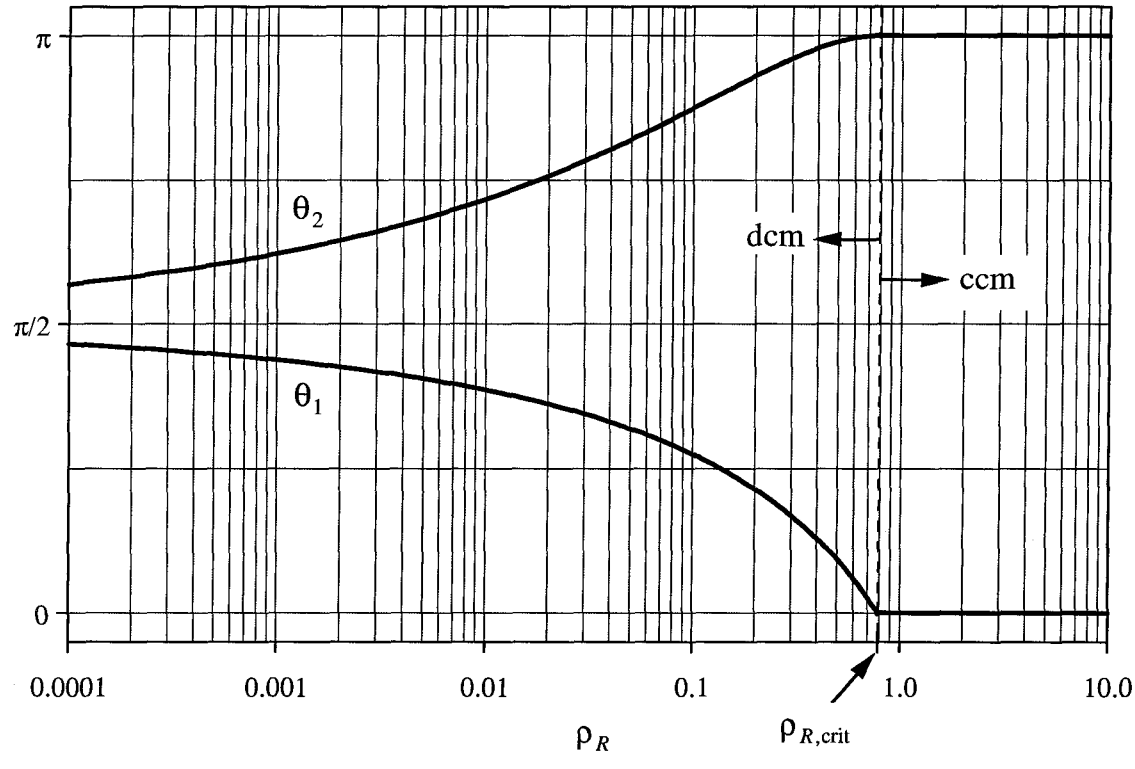


Figure 3.26: Turn-on angle θ_1 and turn-off angle θ_2 as a function of normalized impedance ρ_R for the resonant filter.

Ac/Dc Conversion Ratio

With angles θ_1 and θ_2 known as a function of ρ_L, equations (3.5.5) and (3.5.23) are used to plot the peak ac/dc conversion ratio M_p as a function of ρ_L, as shown below in figure 3.27.

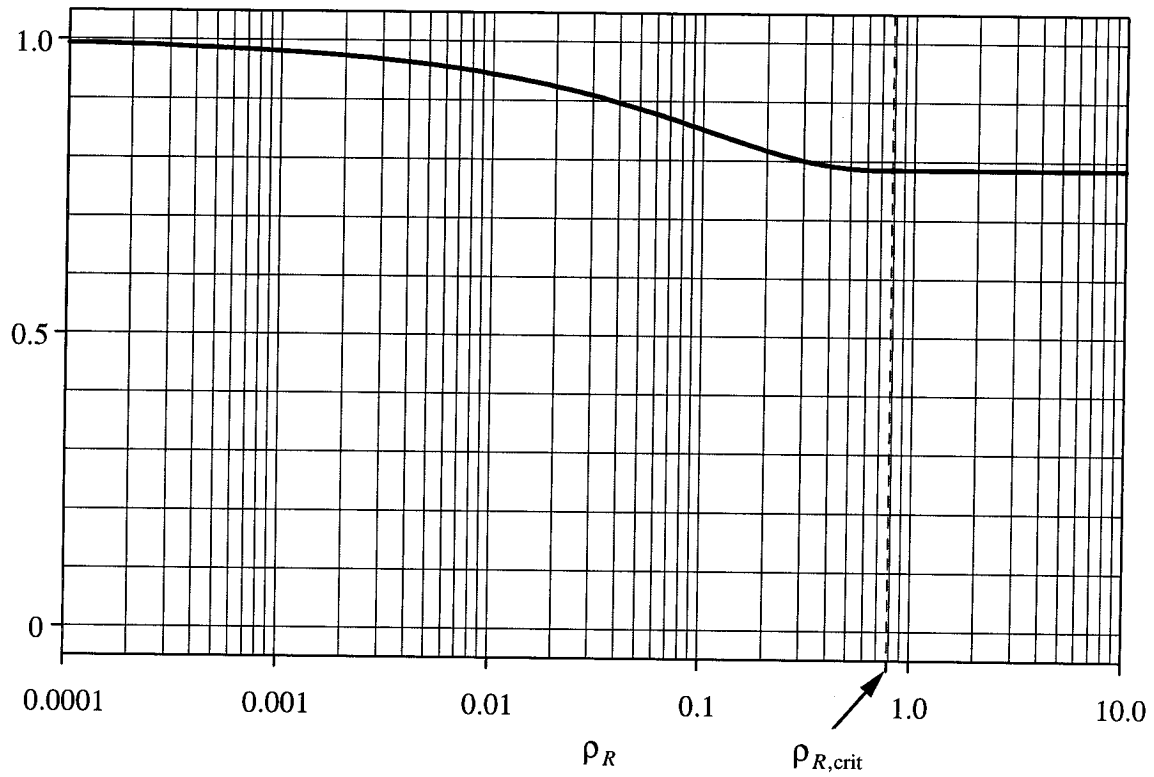


Figure 3.27: Peak ac/dc conversion ratio M_p as a function of normalized impedance ρ_R for the resonant filter.

Power Factor and Harmonics

First, consider operation in dcm. Using equation (3.5.16), the inductor current in the interval $0 \le \theta \le \pi$ may be written in terms of the ideal current as

$$i_L(\theta) = \begin{cases} I_{ideal} \dfrac{1}{\sqrt{2}\rho_R} \left[(\theta - \theta_1)\sin\theta - \sin\theta_1 \sin(\theta - \theta_1) \right] \; ; \; \theta_1 \le \theta \le \theta_2 \\ 0 \; ; \; \theta_2 \le \theta \le \pi + \theta_1 \end{cases} \tag{3.5.26}$$

The actual input current is the alternating periodic extension (see appendix A) of this result. The Fourier coefficients of the fundamental component of the input current in dcm are then

$$a_{1,\mathrm{dcm}} = I_{ideal}\frac{\sqrt{2}}{4\pi\rho_R}\Big[(\theta_2-\theta_1)(1-\cos 2\theta_2-\cos 2\theta_1)+ (\sin 2\theta_2-\sin 2\theta_1)-\frac{1}{2}\sin 2(\theta_2-\theta_1)\Big] \qquad (3.5.27)$$

$$b_{1,\mathrm{dcm}} = I_{ideal}\sqrt{2}$$

The rms input current in dcm is given by

$$I_{rms,\mathrm{dcm}} = I_{ideal}\sqrt{\frac{2}{\pi}}\frac{1}{4\rho_R}\Big[\frac{2}{3}(\theta_2-\theta_1)^3-(\theta_2-\theta_1)^2(\sin 2\theta_2+\sin 2\theta_1)+ (\theta_2-\theta_1)\big(1+\cos 2(\theta_2-\theta_1)-2\cos 2\theta_2-\cos 2\theta_1\big)+ \frac{5}{4}\sin 2\theta_2-\sin 2\theta_1+\frac{1}{4}\sin(2\theta_2-4\theta_1)-\sin 2(\theta_2-\theta_1)\Big]^{\frac{1}{2}} \qquad (3.5.28)$$

In ccm, the inductor current in the interval $0\le\theta\le\pi$ is given by equation (3.5.11), and the actual input current is the alternating periodic extension of this result. The Fourier coefficients of the fundamental component of the input current are computed using the results of appendix A, and are given by the comparatively simple expressions

$$a_{1,\mathrm{ccm}} = I_{ideal}\left(-\frac{1}{2\sqrt{2}\rho_R}\right)$$
$$b_{1,\mathrm{ccm}} = I_{ideal}\sqrt{2} \qquad (3.5.29)$$

The rms input current in ccm can also be written as a function of ρ_R in closed form

$$I_{rms,\mathrm{ccm}} = I_{ideal}\sqrt{1+\frac{\pi^2-6}{48\rho_R^2}} \qquad (3.5.30)$$

From these results, the power factor, distortion factor, and displacement factor are computed from the usual formulas

$$PF = \frac{I_{ideal}}{I_{rms}} \;;\; DF = \frac{I_1}{I_{rms}} \;;\; \cos\phi_1 = \frac{I_{ideal}}{I_1} \tag{3.5.31}$$

In ccm, it is possible to write the expressions explicitly as functions of ρ_R:

$$PF = \frac{1}{\sqrt{1+\frac{\pi^2-6}{48\rho_R^2}}} \;;\; DF = \sqrt{\frac{1+\frac{1}{16\rho_R^2}}{1+\frac{\pi^2-6}{48\rho_R^2}}} \;;\; cos\phi_1 = \frac{1}{\sqrt{1+\frac{1}{16\rho_R^2}}} \tag{3.5.32}$$

and these results for operation in both dcm and ccm are plotted in figure 3.28.

In dcm, the normalized input current harmonic coefficients are found by evaluating the integrals numerically. In ccm, however, they are available in closed form, and are given by

$$\left.\begin{aligned} a_{n,\text{ccm}} &= I_{ideal}\frac{\sqrt{2}}{\rho_R}\frac{1}{(n^2-1)} \\ b_{n,\text{ccm}} &= 0 \end{aligned}\right\} \; n = 3,5,7,.... \tag{3.5.33}$$

The normalized input current harmonics for both operating modes are plotted as a function of the normalized impedance ρ_R in figure 3.29.

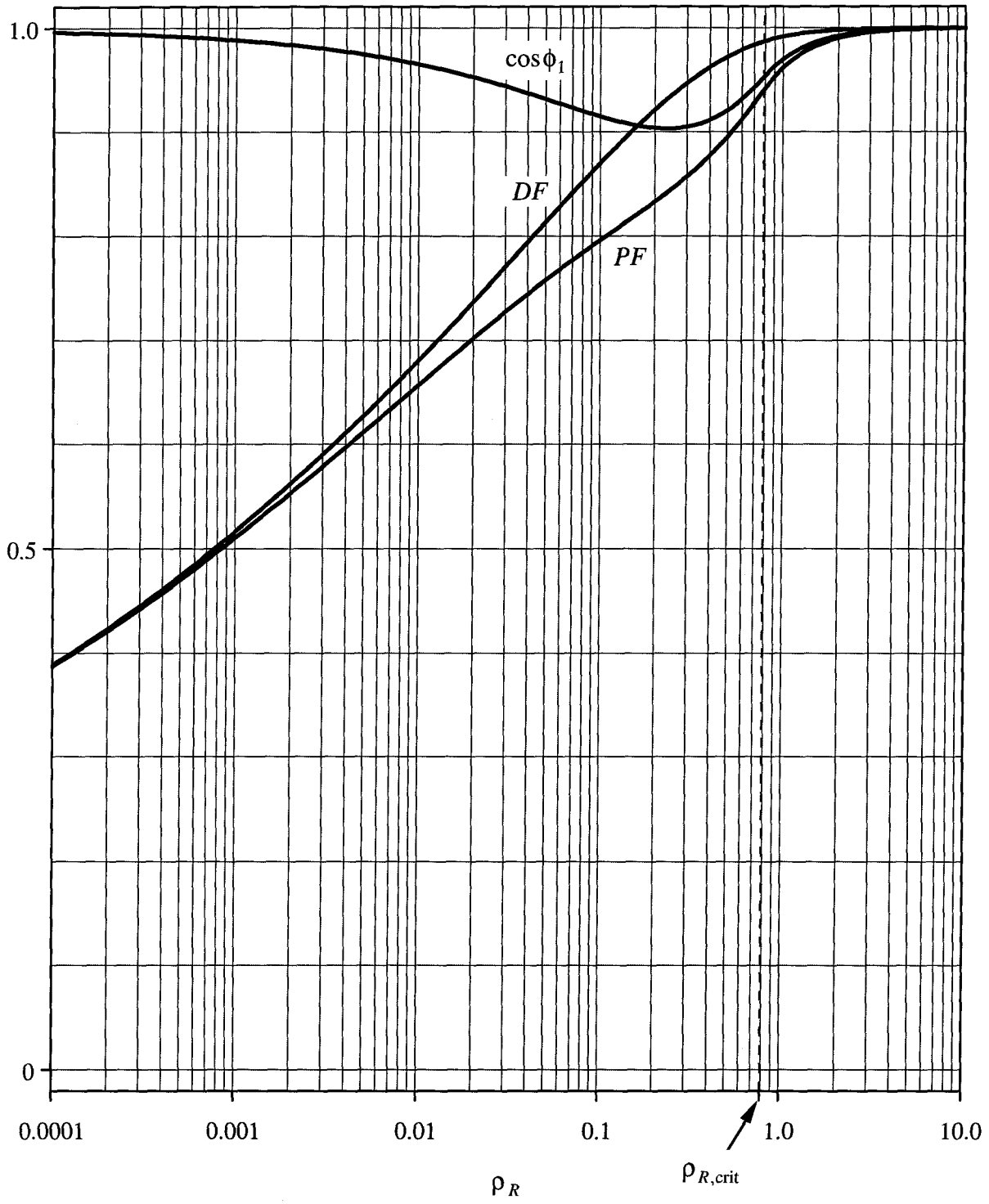


Figure 3.28: Power factor, distortion factor, and displacement factor as a function of normalized impedance ρ_R for the resonant filter.

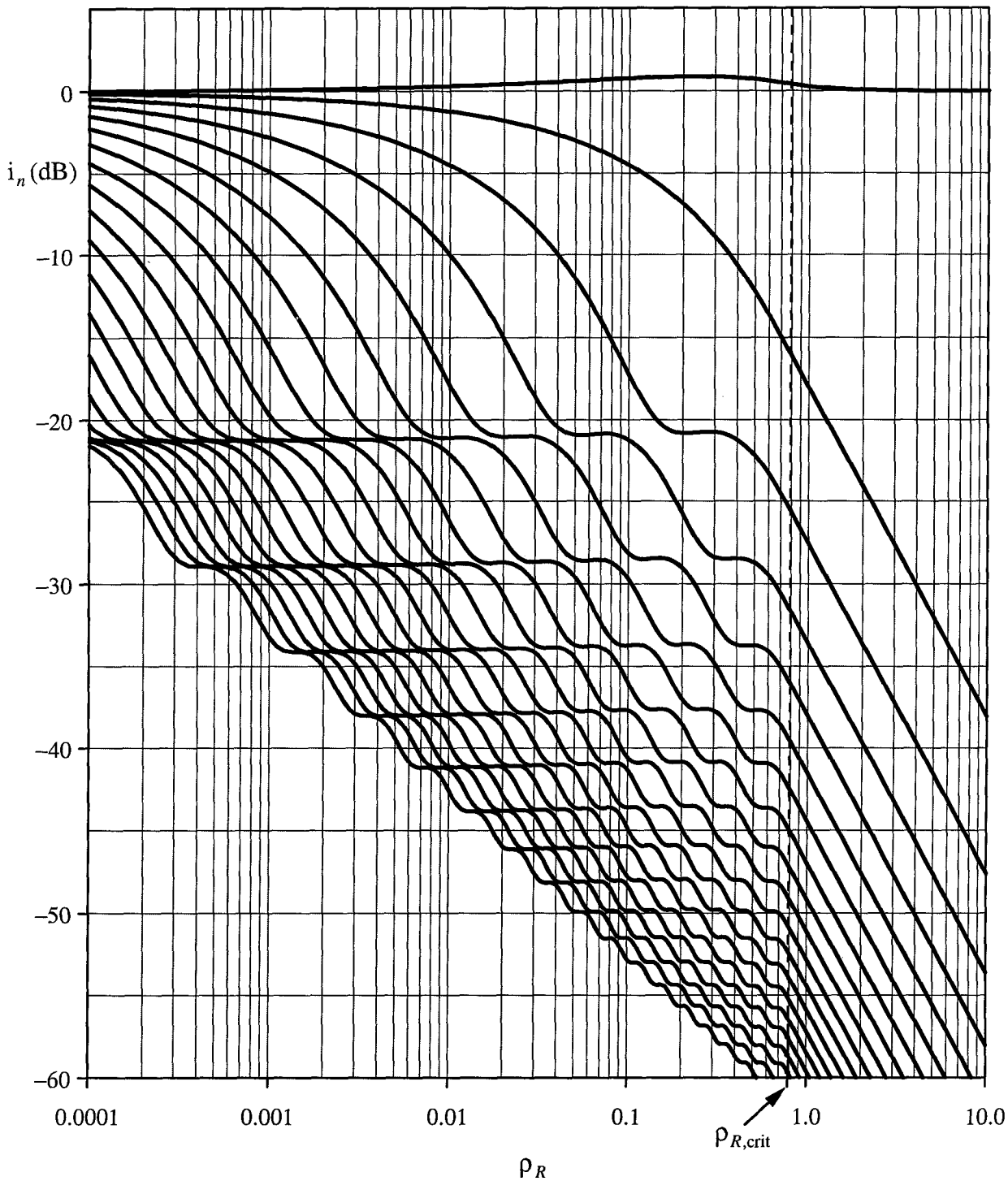


Figure 3.29: Normalized odd input current harmonics 1-39 for the resonant filter as a function of normalized impedance ρ_R. The topmost curve is the fundamental, and odd harmonics 3-39 progress downward in order.

3.6 Discussion

With the performance characteristics established, compliance of a design with a given performance specification can be established. The performance of the capacitor filter is poor, regardless of the operating condition, and it should be dismissed for any high power factor application. The performance of the inductor and resonant filters is, however, much better, and these circuits are candidates for use in applications requiring high power factor.

In order to be useful in low frequency utility line applications, the passive filter must be designed to comply with the performance specifications, while employing an inductor of reasonable size and weight. Smaller inductors correspond to lower values of the normalized impedance ρ. For low values of ρ, say $\rho = 0.03$, reasonable performance can be obtained with either of the inductor filters, or the resonant filter. For values of ρ in this neighborhood, these filters operate well into dcm for the case of the line-side inductor filter and the resonant filter, and well into dcm1 for the case of the load-side inductor filter. In this region, the performance characteristics of both inductor filters is identical because circuit operation in dcm (line-side inductor filter) and dcm1 (load-side inductor filter) is identical. For the resonant filter, operation well into dcm implies that the value of the resonant inductor is relatively small, and the corresponding value of the resonant capacitor is therefore relatively large. Because the resonant capacitor is large, its voltage is relatively constant throughout the line period. Note that if one replaces the resonant capacitor with a short circuit, the resonant filter reduces simply to the line-side inductor filter. With this in mind, it is not difficult to imagine why the operation and performance characteristics of the resonant filter in this region are almost exactly the same as those of both the inductor filters. Thus, for the same inductor, the performance characteristics of all three filters is nearly identical. The cost of the additional capacitor required by the resonant filter is therefore unwarranted for operation in this region. However, the resonant filter is useful in high frequency buss applications [40], where it can provide very high power factor, in very little space, using only a few components.

Comparing the inductor filters, the key differences are: (1) the line-side inductor filter provides lower harmonics over a wider operating range than the load-side inductor

filter, (2) the line-side inductor filter is power limited, whereas the load-side inductor filter is not, and (3), the line-side inductor filter suffers from having an inductor in series with the input, the current in which has no path to flow in if the input is suddenly removed. The load-side filter suffers from no such problem, since the bridge rectifier provides the necessary current path.

Another level of sophistication is achieved by the addition of a capacitor or capacitors to the inductor filter configurations. Several passive rectifier circuits of this type can be found in [39], but a full analysis of these circuits is not presently available. The methods used in this chapter can be used to analyze the performance of these circuits, but it is necessary to vary the value of the additional capacitor and the value of the inductor simultaneously. The performance of these filters can then be evaluated by plotting the desired performance characteristics as a function of both the normalized inductor impedance, and the normalized capacitor impedance, as a surface in a three-dimensional plot.

Chapter 4

Energy Storage

In this chapter, the necessity of a single-phase rectifier circuit to store energy is examined. As a starting point, the ideal rectifier of chapter 2 is used, because of its simplicity. Since the power flowing into the ideal rectifier is varying in time, and the power flowing out is, by assumption, constant, energy storage within the rectifier itself must account for the difference. The energy storage element or elements within the rectifier accumulate energy during intervals when the instantaneous input power is greater than the load power, and release energy during intervals when the instantaneous input power is less than the load power. For proper circuit operation, the rectifier must store at least enough energy to support the load with constant power throughout the entire line period.

The managing of stored energy within the rectifier for this purpose is called load balancing [9]. Most practical rectifier circuits in fact store much more energy than the minimum necessary for load balancing. There are several reasons for this. First, many power supply specifications require a "minimum hold-up time," through which the output is required to remain operative during an input voltage dropout. The duration of this dropout is typically several line periods, necessitating storage of considerably more energy than that required for load balancing. Yet another reason for storing excess energy is in the event that the load power suddenly changes, the rectifier needs to have enough headroom to balance the input and output power until the controller adjusts to the new operating condition. Finally, a real rectifier cannot achieve the ideal properties set forth by the assumptions of the ideal rectifier, and excess stored energy is necessary to overcome these deficiencies.

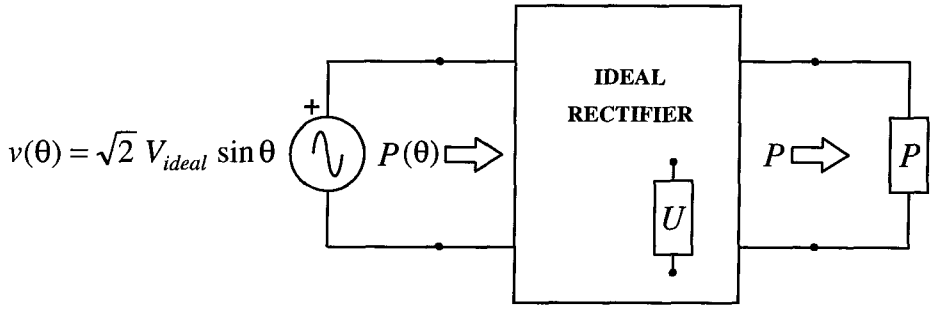


Figure 4.1: Power flow in the ideal rectifier circuit. The energy storage element(s) internal to the rectifier are necessary for load balancing.

4.1 Load Balancing

The managing of stored energy within the rectifier in order to compensate for the difference between input power and output power is called load balancing. In the ideal rectifier circuit of figure 4.1, the power flow into the ideal rectifier is the difference between the input and output power

$$P_r(\theta) = P(\theta) - P \tag{4.1.1}$$

Since the ideal rectifier operates with unity input power factor, this difference is given by

$$P_r(\theta) = 2V_{ideal} I_{ideal} \sin^2\theta - P \tag{4.1.2}$$

Because the ideal rectifier is lossless, the average power absorbed by the rectifier is zero. Taking the average over one period leads to

$$V_{ideal} I_{ideal} = P \tag{4.1.3}$$

which is a statement equating average input power and output power. Using a well-known trigonometric identity, the instantaneous rectifier power is then

$$P_r(\theta) = -P\cos 2\theta \tag{4.1.4}$$

The power flow into the rectifier is equal to the time rate-of-change of the stored energy

$$P_r(\theta) = \omega_l \frac{d}{d\theta} U_r(\theta) \tag{4.1.5}$$

Integrating with respect to the normalized time variable θ gives the energy stored in the rectifier

$$U_r(\theta) = U_r(0) - \frac{P}{2\omega_l}\sin 2\theta \tag{4.1.6}$$

Since the stored energy cannot be negative, we require

$$U_r(0) \geq \frac{P}{2\omega_l} \tag{4.1.7}$$

When these quantities are equal, the stored energy is the minimum required for load balancing. The average energy stored in the rectifier is the time-average of the instantaneous rectifier energy taken over one period. This gives

$$\overline{U}_r = \frac{1}{2\pi}\int_{-\pi}^{\pi} U_r(\theta)\, d\theta = U_r(0) \tag{4.1.8}$$

Thus, when the stored energy is the minimum required for load balancing, the average value of the energy stored in the rectifier is

$$\overline{U}_{r,\min} = \frac{P}{2\omega_l} \tag{4.1.9}$$

We define the normalized stored energy u as the ratio of the average value of the actual energy stored to the average value of the energy stored when the energy stored is the minimum required for load balancing

$$\mathrm{u} \equiv \frac{\overline{U}_r}{\overline{U}_{r,\min}} \tag{4.1.10}$$

The instantaneous value of the energy stored in the rectifier, equation (4.1.4), can now be written in terms of the normalized stored energy as

$$U_r(\theta) = \frac{P}{2\omega_l}(\mathrm{u} - \sin 2\theta) \tag{4.1.11}$$

Thus, the case $u = 1$ corresponds to the energy stored being the minimum required for load balancing, and larger values of u in the ten-to-twenty range are typical of those found in practical rectifier circuits.

4.2 Single Element Load Balancing

If a single element within the ideal rectifier is designated as the energy storage element, then the terminal voltage and current of that element can be written in terms of the normalized stored energy u. Let us assume for the moment that the energy storage element is a capacitor. Equating the energy stored in the rectifier with the capacitor energy, gives the capacitor voltage

$$v_C(\theta) = \sqrt{\frac{P}{\omega_l C}}\sqrt{u - \sin 2\theta} \tag{4.2.1}$$

For $u >> 1$, this expression may be approximated by

$$v_C(\theta) \cong \sqrt{\frac{uP}{\omega_l C}}\left[1 - \frac{1}{2u}\sin 2\theta\right] \tag{4.2.2}$$

Thus, under the conditions set forth by the ideal rectifier, and when $u >> 1$, the capacitor voltage consists primarily of a large dc component, and a small ac ripple component at twice the line frequency

$$v_C(\theta) \cong V_C + \tilde{v}_C \sin 2\theta \tag{4.2.3}$$

where the dc component of the capacitor voltage can be approximated by

$$V_C \cong \sqrt{\frac{uP}{\omega_l C}} \tag{4.2.4}$$

and the ac ripple component at twice the line frequency is then approximately

$$\tilde{v}_C \cong -\frac{P}{2\omega_l C V_C} \tag{4.2.5}$$

The ripple ratio for the capacitor voltage is given by the ratio of one-half of the peak-to-peak ripple voltage to the average capacitor voltage

$$\mathcal{R} \equiv \frac{v_{C,\max} - v_{C,\min}}{2V_C} \tag{4.2.6}$$

This is given by the following exact expression as a function of the normalized stored energy u:

$$\mathcal{R} = \frac{\sqrt{1+\frac{1}{u}} - \sqrt{1-\frac{1}{u}}}{\frac{2}{\pi}\int_0^{\pi} \sqrt{1-\frac{1}{u}\sin 2\theta}\, d\theta} \tag{4.2.7}$$

However, inspection of equation (4.2.2) or (4.2.7) shows that for $u >> 1$, the ripple ratio can be approximated by

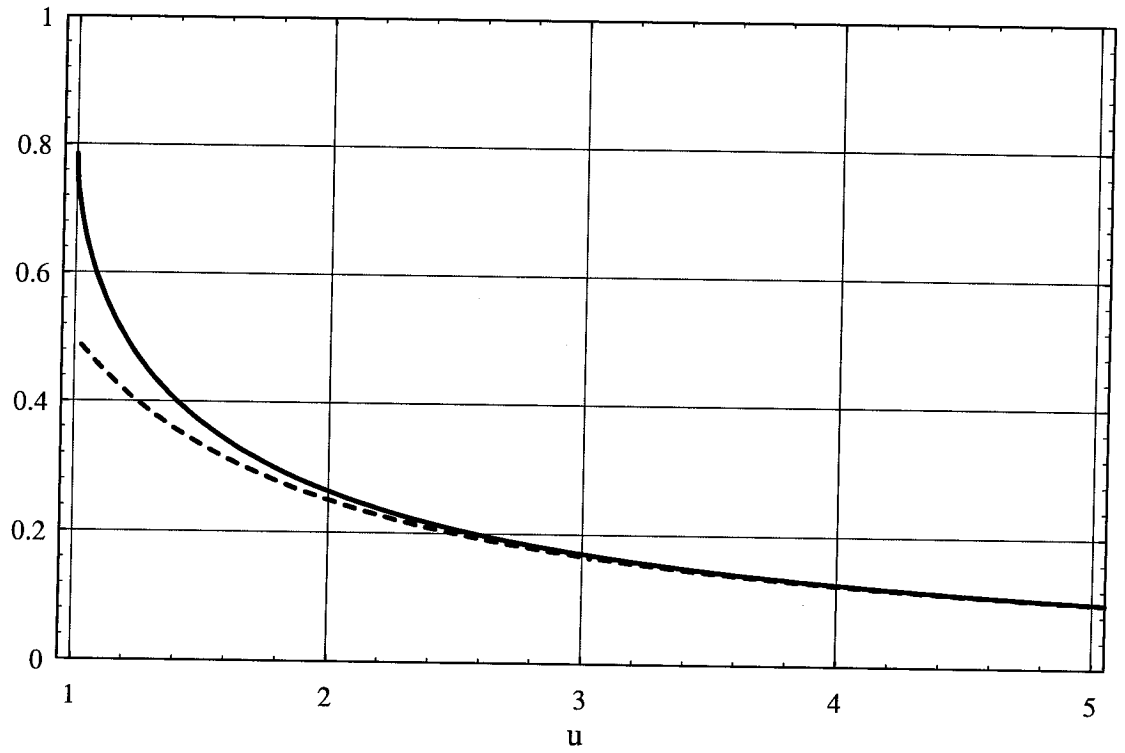


Figure 4.2: Capacitor voltage ripple ratio $\mathcal{R}$ (solid), and the approximation given by equation (4.2.8) (dashed) as a function of the normalized stored energy u, *for the single element energy storage capacitor.*

$$\mathcal{R} \cong \frac{1}{2u} \tag{4.2.8}$$

which is plotted in figure 4.2 along with the exact expression computed by numerically evaluating equation (4.2.7). The error of this approximation is seen to be quite small for $u \geq 3$, and is even more accurate for values of u in the typical range of ten-to-twenty.

The capacitor current could be found by differentiating the capacitor voltage with respect to θ, but is easily obtained by dividing the instantaneous capacitor power, equation (4.1.4), by the instantaneous capacitor voltage, equation (4.2.1). This results in

$$i_C(\theta) = -\sqrt{\omega_l CP}\,\frac{\cos 2\theta}{\sqrt{u - \sin 2\theta}} \tag{4.2.9}$$

Which, when $u >> 1$, can be approximated by

$$i_C(\theta) \cong -\frac{P}{V_C}\left[\cos 2\theta + \frac{1}{4u}\sin 4\theta\right] \tag{4.2.10}$$

The capacitor current thus consists primarily of a large ac component at twice the line frequency, and a relatively small ac component at four times the line frequency which is inversely proportional to the normalized stored energy u. For most practical purposes, we may ignore the component at four times the line frequency, and consider only the large component at twice the line frequency.

Now, let us assume that the single energy storage element is instead an inductor. We needn't derive the expressions for the inductor current and inductor voltage from first principles. Instead, we can take advantage of the duality between the capacitor and the inductor as energy storage elements. Making the following substitutions into the equations of this section:

$$\begin{aligned} C &\rightarrow L \\ v_C &\rightarrow i_L \\ i_C &\rightarrow v_L \end{aligned} \tag{4.2.11}$$

we find the exact as well as approximate expressions for the inductor current, inductor voltage, and inductor current ripple ratio, for the ideal rectifier with a single inductor as the energy storage element.

Chapter 5

Pwm Switches in Continuous Conduction Mode

In this chapter, several new pwm switch models are introduced. These models are easily and naturally inserted into a pwm converter by replacing the transistor and diode switches, terminal-by-terminal, with equivalent averaged switch models. This circuit-oriented approach is shown to yield results which are identical to those obtained via the mathematical approach of state-space averaging, with far less effort. Using this method, the analysis of a pwm converter is likened to the analysis of a standard linear transistor amplifier.

The original pwm switch model [20] was developed while searching for a simplified approach to the modeling of quasi-resonant converters. At that time, it was realized that the action of the switches in all pwm converters is fundamentally the same, regardless of the specific converter topology. Since then, several refinements and extensions have been developed [18], including pwm switches in for converters in the discontinuous conduction mode [19], and even a pwm converter synthesis procedure based on pwm switches [22,23]. Based on these developments, the pwm switch concept is indeed a very powerful one, and its usefulness has not yet been fully realized.

5.1 Definition of an Ideal Pwm Converter

The term "pwm" (pulse-width modulation) itself is used here not to describe any particular control scheme, but rather to distinguish a class of switching converters possessing quasi-rectangular switch waveforms. That is, when a converter belonging to this class operates in ccm, the voltage and current waveforms appearing on the switches are rectangular, except perhaps for switching ripple which may be impressed upon them. Note that the switching ripple needn't necessarily be small, provided that ccm is

maintained. For a converter operating in ccm, since the pwm switch is based on the averaging of the switch waveforms, the switching ripple does not cause any difficulty in the analysis. Hence, a switch waveform with ripple is equivalent to some rectangular waveform with no ripple, with its amplitude adjusted to give the same average value.

The following definition and theorems describes what will henceforth be referred to as an ideal pwm converter. Proof of these theorems may be found in [1].

Definition: An ideal pwm converter is a 100% efficient dc/dc power converter, consisting of only the following elements, and also satisfying theorems 1 and 2 below:

1. A single ideal transistor switch Q.
2. A single ideal diode rectifier D.
3. A single input voltage source v_g.
4. A set of LTI capacitors $\mathcal{C} = \{C_i,\ i = 1,\ldots,n_C\}$.
5. A set of LTI inductors $\mathcal{L} = \{L_i,\ i = 1,\ldots,n_L\}$; no coupling is allowed.
6. A load consisting of a LTI resistor R and/or a constant power load P (in parallel), which is in a loop of capacitors, or in a cut-set of inductors.

Theorem 1: In an ideal pwm converter, the transistor Q, the diode D, and a (possibly empty) set of capacitors $\mathcal{C}_{off}$ with total voltage v_{off} form a loop. The source v_g may also be in the loop, with its voltage included in v_{off}.

Theorem 2: In an ideal pwm converter, the transistor Q, the diode D, and a set of inductors $\mathcal{L}_{on}$ with total current i_{on} form a cut-set.

The definition states that an ideal pwm converter is completely efficient. This implies that, besides the load, all components in the ideal pwm converter are free of losses. Thus, the transistor Q and diode D switch instantaneously, and have no conduction loss in the on-state, nor loss due to leakage in the off-state. Also, the inductors and capacitors are ideal lossless elements. Later, in sections 5.4 and 5.5, we relax these restrictions, and demonstrate a pwm switch model valid for pwm converters with lossy resistive elements.

5.2 Pwm Switches for Ideal Pwm Converters

Theorems 1 and 2 provide the fundamental picture of the operation of the switches in an ideal pwm converter depicted in figure 5.1. Kirchhoff's Voltage Law around the loop of Theorem 1 gives

$$v_Q + v_D = v_{off} \tag{5.2.1}$$

Thus, when transistor Q is on, $v_Q = 0$ and $v_D = v_{off}$, and when diode D is on, $v_D = 0$ and $v_Q = v_{off}$. Simply stated, the voltage across each switch is zero while it is on, and v_{off} while it is off. As an aside, we conclude that in an ideal pwm converter, the voltage stress on the transistor and the diode is the same. For the cut-set of Theorem 2, Kirchhoff's Current Law gives

$$i_Q + i_D = i_{on} \tag{5.2.2}$$

When transistor Q is on, $i_Q = i_{on}$ and $i_D = 0$, and when diode D is on, $i_D = i_{on}$ and $i_Q = 0$. Thus, the current flowing in each switch is i_{on} while it is on, and zero while it is off.

It is important to point out that the reference directions for the voltages and currents $\{v_Q,\ i_Q,\ v_D,\ i_D,\ v_{off},\ i_{on}\}$ are chosen so that all quantities are positive. This choice results in the so called "passive convention" of voltage and current orientation for the transistor, but the "non-passive convention" for the diode. Recall that the orientation of the voltage and current in the passive convention implies that the instantaneous power (i-v product) absorbed by an element is positive, and that delivered by an element negative. The confusion that this violation of the passive convention might cause is the price paid for the simplicity of knowing that all of the aforementioned quantities are positive.

The duty ratio d is defined as the fraction of the switching period T_s that the transistor Q is on. We then define the duty ratio complement $d' = 1 - d$ as the fraction of the switching period that the transistor Q is off. If we denote the average taken over a switching period by $\langle \cdot \rangle$, we find by inspection of the waveforms in figure 5.1:

$$\begin{aligned} \langle i_Q \rangle &= d\langle i_{on} \rangle & \qquad & \langle i_D \rangle = d'\langle i_{on} \rangle \\ \langle v_Q \rangle &= d'\langle v_{off} \rangle & \text{and} \qquad & \langle v_D \rangle = d\langle v_{off} \rangle \end{aligned} \tag{5.2.3}$$

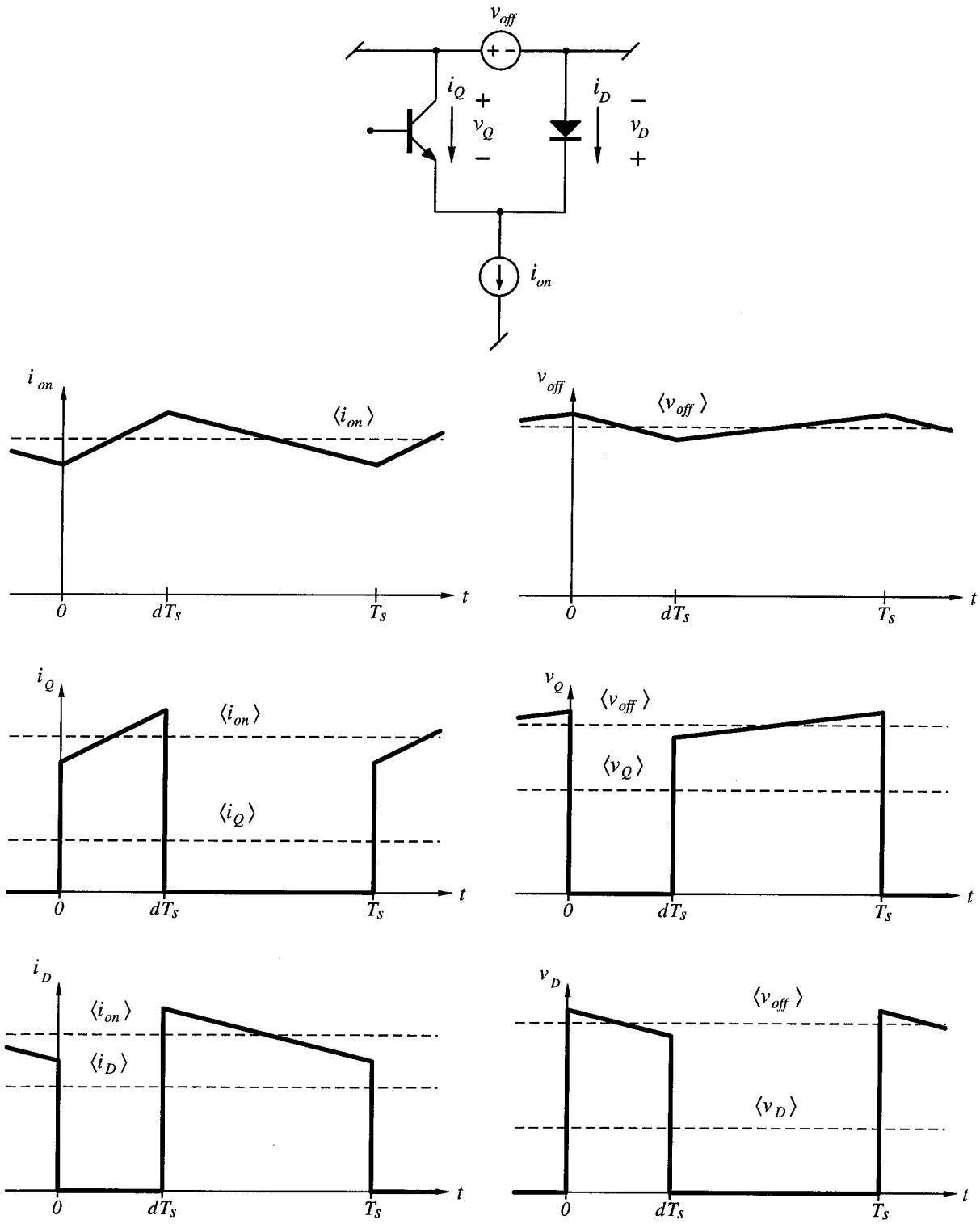


Figure 5.1: Relationship between the switches, switch voltages, and switch currents, fundamental to the operation of any pwm converter.

Taking the ratio of the average currents, and also the ratio of the average voltages, we find

$$\frac{\langle i_Q \rangle}{\langle i_D \rangle} = \frac{d}{d'} \quad \text{and} \quad \frac{\langle v_Q \rangle}{\langle v_D \rangle} = \frac{d'}{d} \tag{5.2.4}$$

But these are exactly the equations which relate the voltage and current in an ideal transformer. Thus, the average values of the transistor and diode voltage and current are related via the ideal transformer equations, as depicted below in figure 5.2. Although the ideal transformer is normally a linear circuit element, this transformer representation is nonlinear, due to the fact that the duty-ratio, and thus the turns-ratio, is time-varying.

The ideal transformer in figure 5.2 has two equivalent circuit representations utilizing dependent sources. One uses a dependent current source to represent the primary winding, and a dependent voltage source to represent the secondary winding. In the other equivalent circuit, a dependent voltage source is used to represent the primary winding, and a dependent current source to represent the secondary winding. An equivalent circuit representation utilizing two voltage sources is incorrect, because it leaves the currents undetermined. Similarly, an equivalent circuit representation utilizing two current sources is incorrect because it leaves the voltages undetermined. Both valid equivalent circuit representations are shown in figure 5.3. These equivalent circuit representations are continuous, since they are based on average switch quantities, but nonlinear, since they depend on the duty ratio and average switch quantities in a nonlinear manner.

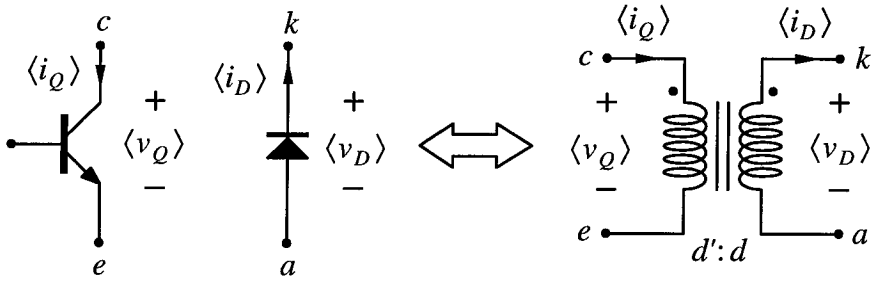


Figure 5.2: The average switch voltages and currents are identical to those of the ideal transformer with turns ratio d':d.

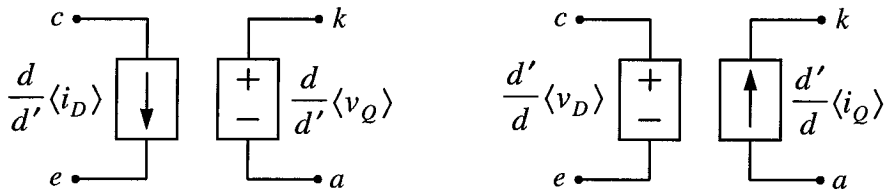


Figure 5.3: Two dependent source nonlinear pwm switch equivalent circuits representing the relationships between the average switch voltages, average switch currents, and duty the ratio.

Although these models are nonlinear, they can be very useful in their present form, since they are completely self contained. That is, the voltage and current generators depend only on quantities within the switch model itself, and not on external (converter) quantities. Also, since no small-signal assumption was made in their derivation, they correctly model the dc, large-signal, and small-signal circuit behavior. Hence, they may be connected in place of the switches in any ideal pwm converter for the purpose of simulating converter performance. Because these are continuous averaged models, circuit simulations utilizing them are extremely efficient.

Making use of relationships (5.2.3), the generator gains in the equivalent circuits of figure 5.3 can be expressed in terms of v_{off} and i_{on}, as shown below in figure 5.4. These equivalent circuits are named the d-model, and the d'-model. The d-model is given its name because each generator in the d-model reflects the characteristic switch quantity on the d-interval. That is, on the d-interval, the transistor Q is on, and is therefore represented by a current source; the diode is off, and is therefore represented by a voltage source. Note that on this interval, the transistor voltage and diode current

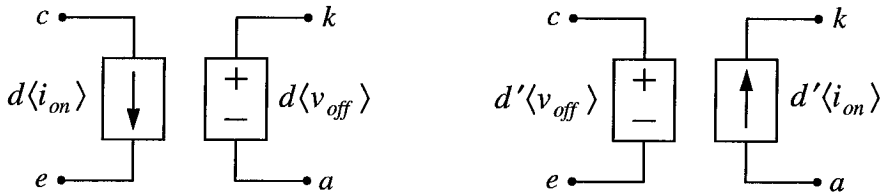


Figure 5.4: Two dependent source nonlinear equivalent circuits representing the relationships between the switch off-voltage, on-current, and duty ratio for an ideal pwm converter operating in continuous conduction mode.

are both zero. Similarly, for the d'-model, each generator reflects the characteristic switch quantity on the d'-interval. The transistor is therefore represented by a voltage source, and the diode by a current source. On this interval, the transistor current and diode voltage are both zero.

Either model can be used to represent the average behavior of the switches in any ideal pwm converter operating in ccm. Note that both models are nonlinear, since they involve products of time-varying circuit quantities. However, no small-signal assumption has been made in their derivation, and both are therefore useful in their present form for modeling and simulation of small-signal or large-signal converter behavior, in applications such as ac/dc rectifier circuits or dc/dc converter circuits.

5.3 Dc and Small-Signal Ac Models for Pwm Switches

In dc/dc applications, the pwm converter operates in a manner such that its incremental dynamics can be analyzed via a perturbation of the converter states about the steady-state (dc) operating point. In ac/dc rectifier applications, however, the operating point varies over a wide range, since the input voltage is varying over a wide range in a low-frequency sinusoidal manner. In these rectifier circuits, as long as the variation of the operating point is slow compared with the bandwidth of the closed loop control system, it is possible to consider the dynamics of the power circuit in a quasi-static manner [9]. Hence, a linearized pwm switch model can be useful in the analysis of ac/dc systems in the same way that it is useful in dc/dc systems.

Consider the d-model in figure 5.4. The model is perturbed according to

$$\begin{aligned} d &= D + \hat{d} \\ \langle i_{on} \rangle &= I_{on} + \hat{i}_{on} \\ \langle v_{off} \rangle &= V_{off} + \hat{v}_{off} \end{aligned} \tag{5.3.1}$$

where capital letters are used to denote steady-state (dc) quantities and carats are used to denote a small-signal perturbation. Substituting into the d-model of figure 5.4, and discarding the nonlinear product terms (products of two small quantities are considered negligible), we arrive at the linear model in figure 5.5(a).

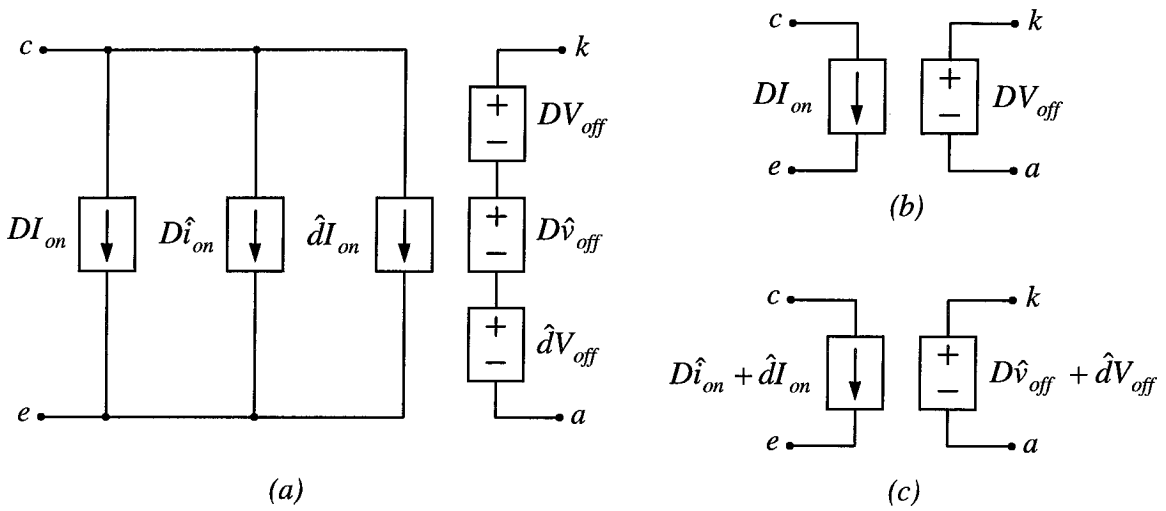


Figure 5.5: (a) Perturbed and linearized version of the pwm switch d-model, (b) its dc equivalent circuit model, and (c) its ac equivalent circuit model.

Under steady-state conditions, the perturbation quantities are zero. Thus, the linear model in figure 5.5(a) reduces to the dc model of figure 5.5(*b*) in steady-state. This equivalent circuit model is easily substituted terminal-by-terminal into the pwm converter to establish the dc operating point. To make things even easier, in steady-state, the average voltage across any inductor in the converter must be zero. Therefore, in the dc equivalent circuit, the inductors may be replaced by short circuits. In a dual manner, in steady-state, the average current through a capacitor in the converter is also zero. Therefore, in the dc equivalent circuit, the capacitors in the converter may be replaced by open circuits. Hence, all that remains in the dc equivalent circuit of an ideal pwm converter is the input source, the dc model of the pwm switches, and the load.

With the dc operating point established, the generators of the dc model can be considered as independent dc sources in the complete linearized model of figure 5.5(a). The rules of superposition therefore apply, and these independent dc sources can be suppressed in the complete linearized model, resulting in the small-signal linear ac model of figure 5.5(c). This linear ac model is easily inserted into the converter, terminal-by-terminal, to study the small-signal ac dynamic converter behavior. Before proceeding with an example, this same procedure of perturbation, linearization, and

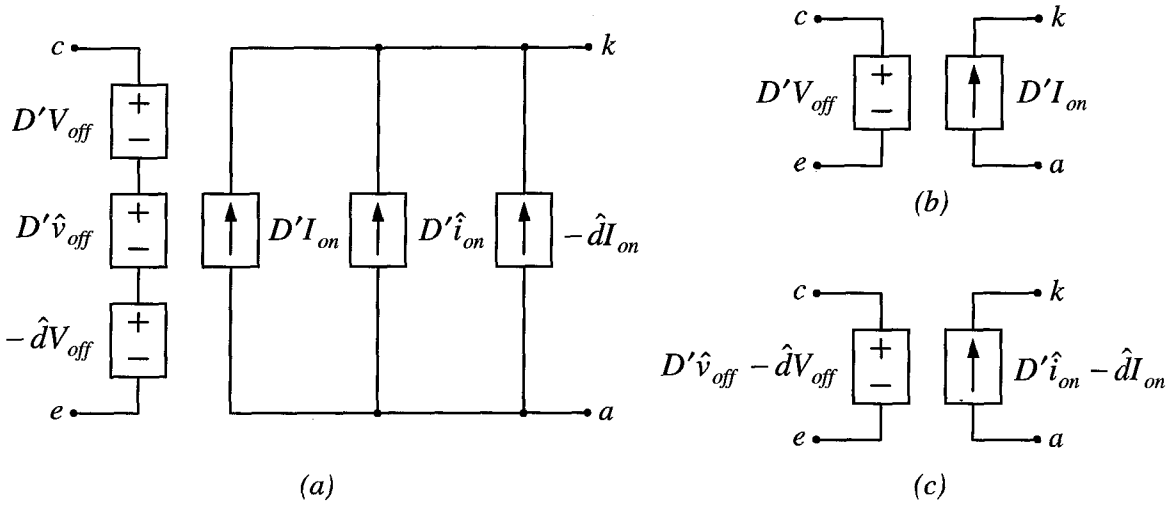


Figure 5.6: (a) Perturbed and linearized version of the pwm switch d'-model, (b) its dc equivalent circuit model, and (c) its ac equivalent circuit model.

separation into ac and dc equivalent circuits is applied to the d'-model of figure 5.4, resulting in the equivalent circuits for the d'-model, shown above in figure 5.6.

Either the d-model or the d'-model may be used to analyze the dc and small-signal ac behavior of any ideal pwm converter. However, the model for which the analysis is simplest varies depending on the converter in question. Large-signal behavior can be modeled using either of the large-signal nonlinear models in figure 5.4, or even those in figure 5.3. For the purpose of simulation, the models of figure 5.3 have the advantage that the model's voltage and current generators depend only on voltages and currents within the switch model itself, rather than voltages and currents in the converter. Each model can therefore be implemented in the simulator as a self-contained sub-circuit, which is easily inserted into any ideal pwm converter for simulation. Although these nonlinear pwm switch models are well-suited for large-signal simulations, they are of course well-suited for small-signal simulations as well.

Example: Ideal Dc/Dc Boost Converter

To demonstrate the power and simplicity of the method of pwm switches, and also to compare the results with those obtained by the method state-space averaging [2],

consider the problem of deriving the control-to-output transfer function of the ideal boost converter shown below in figure 5.7(a):

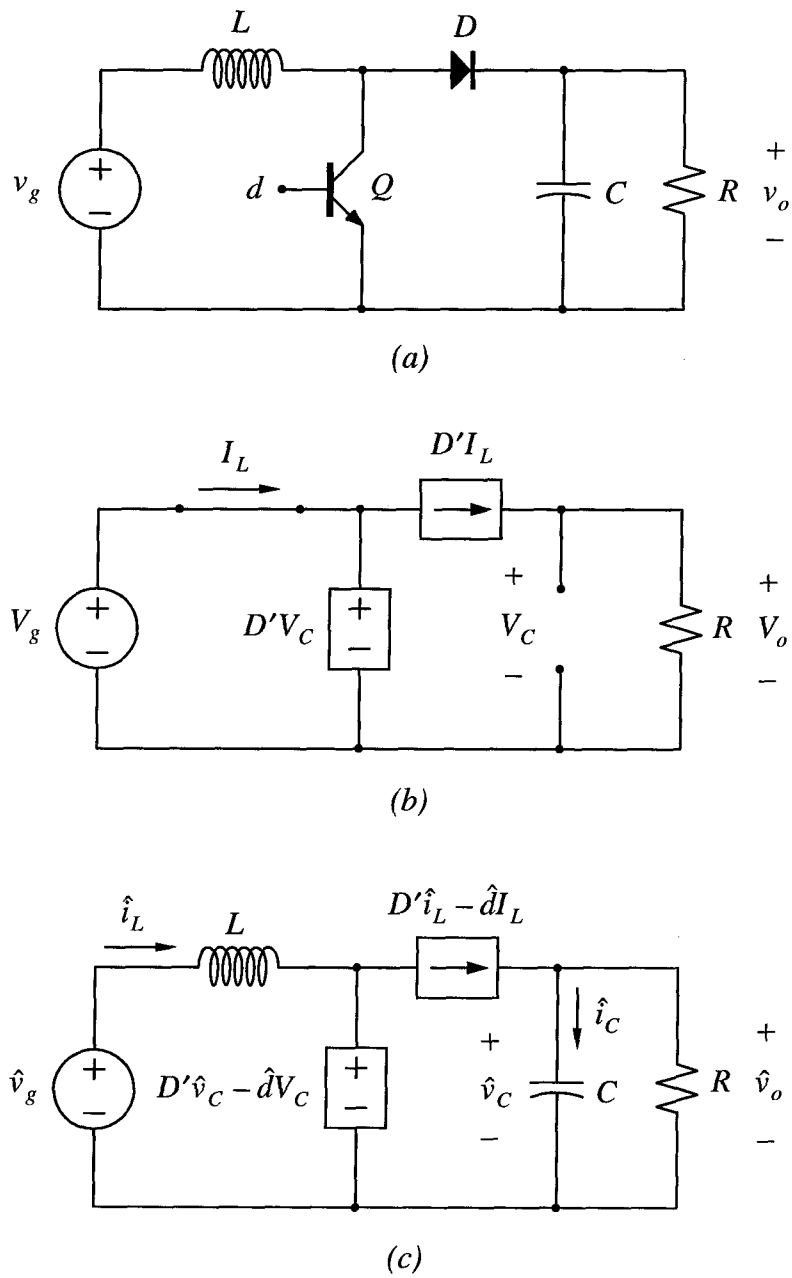


Figure 5.7: *(a) Ideal dc/dc boost converter used to demonstrate the application of the pwm switch, (b) the dc equivalent circuit, and (c), the linear small-signal ac equivalent circuit.*

The first step in the analysis is that of identifying v_{off} and i_{on}. The off-voltage v_{off} forms a loop with transistor Q and diode D. When diode D is conducting, the transistor is off, and the voltage across it is simply the capacitor voltage v_C. Thus, we have $v_{off} = v_C = v_o$. The on-current i_{on} forms a cut-set with transistor Q and diode D. When the transistor is on, its current is the inductor current i_L. Thus we have $i_{on} = i_L = i_g$.

Now we have the choice of using the d-model or the d'-model. For the boost converter, the d'-model is particularly simple, so we will use it here. The dc model of the pwm switches is substituted for the converter switches, resulting in the dc equivalent circuit in figure 5.7(b). This gives immediately

$$M \equiv \frac{V_o}{V_g} = \frac{1}{D'} \qquad \text{and} \qquad I_o = D'I_L \Rightarrow I_L = \frac{V_o}{D'R} \tag{5.3.2}$$

In the ac circuit model of figure 5.7(c), using superposition, the dc components have been removed, making the initial conditions of all converter states zero. This makes the writing of the equations-of-state in the Laplace transform domain particularly easy. Since we are interested in the control-to-output transfer function, we may set $\hat{v}_g = 0$. The equations-of-state for the boost converter are then written by inspection

$$\begin{aligned} sL\hat{i}_L(s) &= \hat{d}(s)V_C - D'\hat{v}_C(s) \\ sC\hat{v}_C(s) &= D'\hat{i}_L(s) - \hat{d}(s)\frac{V_o}{D'R} - \frac{\hat{v}_C(s)}{R} \end{aligned} \tag{5.3.3}$$

Solving the first of these equations for $\hat{i}_L(s)$, and then substituting in the second gives the desired result

$$\frac{\hat{v}_o}{\hat{d}}(s) = \frac{V_g}{D'^2} \frac{1 - s\dfrac{L}{D'^2R}}{1 + s\dfrac{L}{D'^2R} + s^2\dfrac{LC}{D'^2}} \tag{5.3.4}$$

which is the same result obtained by the method of state-space averaging. The pwm switch method gives the correct answer using a circuit-oriented approach, with very little work. In the derivation of the pwm switch, however, we limited ourselves to "ideal" pwm converters, and the pwm switch model in its present form yields results

which are incorrect when applied to converters with lossy resistive elements. In the following two sections, we examine this problem and provide a remedy.

5.4 Pwm Switches for Converters with Series Resistive Elements

If the converter contains a capacitor or capacitors with equivalent series resistance (esr), or if resistive elements appear in series with elements in the converter, then the off-voltage v_{off} needn't be equal for the transistor and diode switches. To be precise, if the converter in question has series resistive elements in the v_{off} loop, then the off-voltage of the two switches will differ. Theorem 1 in section 5.1 defines the v_{off} loop for an ideal pwm converter as a loop containing the transistor Q, the diode D, a (possibly empty) set of capacitors C_{off}, and possibly v_g. For the present case of non-ideal pwm converters, we need to add to this list series resistors.

Consider the boost converter shown in figure 5.8(a), with equivalent series resistors (esr's) R_L and R_C. The v_{off} loop consists of elements Q, D, R_C, and C. Note that series resistor R_L is not in the v_{off} loop, and will therefore not affect v_{off}. With series resistor R_C in the v_{off} loop, the off-voltage must be specified separately for the transistor and diode. Over one switching period, $0 \le t \le T_s$, we have in general

$$v_{off} = \begin{cases} v_{D,off} \; ; \; 0 \le t < dT_s \\ v_{Q,off} \; ; \; dT_s < t \le T_s \end{cases} \tag{5.4.1}$$

For the boost converter in figure 5.8(a), the off-voltage for the transistor and diode are easily written in terms of the converter states by inspection

$$\begin{aligned} v_{Q,off} &= \frac{R}{R+R_C} v_C + R_C \| R \, i_L \\ v_{D,off} &= \frac{R}{R+R_C} v_C \end{aligned} \tag{5.4.2}$$

which are clearly not equal. On the other hand, the current in each switch is still the same when the switch is on, equal to the inductor current i_L. Thus the relationships

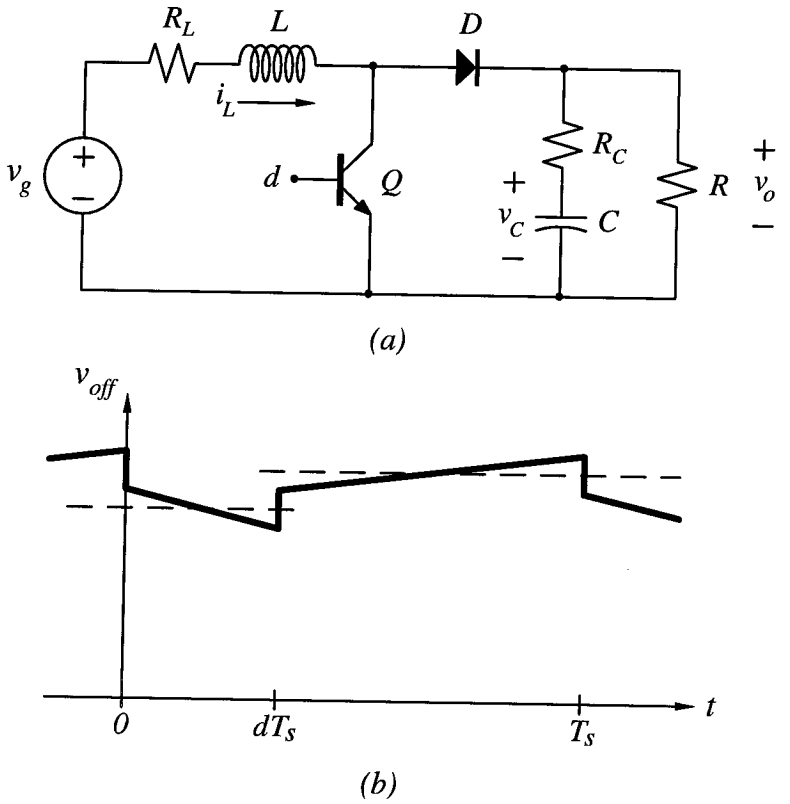


Figure 5.8: *(a) Boost converter with series resistors R_L and R_C, and (b) off-voltage v_{off}, typical of pwm converters with series resistors in the v_{off} loop.*

$$\langle i_Q \rangle = d\langle i_{on} \rangle \quad \text{and} \quad \langle i_D \rangle = d'\langle i_{on} \rangle \tag{5.4.3}$$

are still valid. Reflecting the change of the off-voltages into the d-model of figure 5.4, a new pwm switch model, valid for converters with series resistors in the v_{off} loop, is simply that of figure 5.9, where the diode is properly represented by a voltage source reflecting its average voltage over one switching period, and the transistor by a current source reflecting its average current over one switching period. Thus, in the d-model, each switch is represented by an equivalent source with value equal to the average value of the characteristic quantity of that switch in the d-interval. The ac and dc models shown in figure 5.9(b) and (c) follow from the same perturbation and linearization steps used in section 5.3 for the ideal pwm converter case.

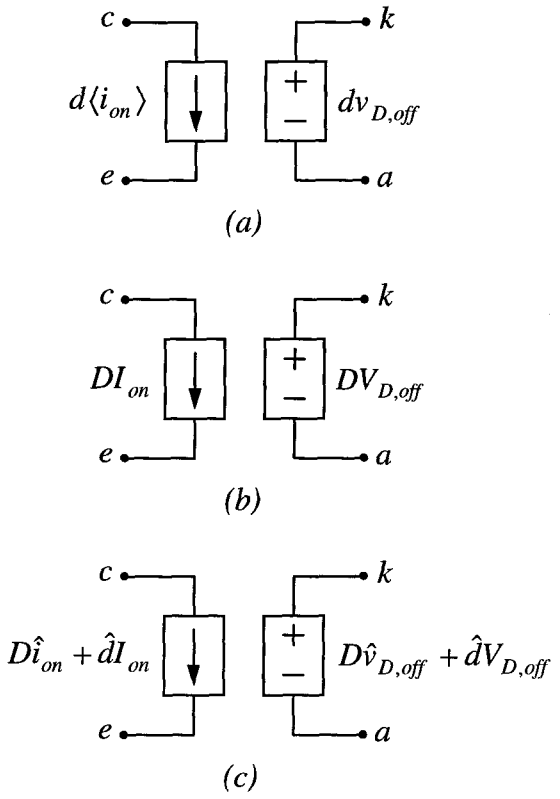


Figure 5.9: The pwm switch d-model, valid for converters utilizing elements with series resistors in the v_{off} loop. (a) Complete large-signal, nonlinear model, (b) dc model, and (c), small-signal, linear ac model.

In the d'-model, recall that each switch is represented by a generator reflecting its characteristic quantity during the d'-interval, averaged over the switching period. Thus, the transistor is represented by a voltage source with voltage equal to the average transistor voltage, and the diode is represented by a current source with current equal to the average diode current. Because the off-voltage for the diode and transistor switches is different, the generators representing these voltages have been adjusted in the model to reflect the change. Because the on-current is unaffected by the addition of the series resistors, no adjustment to the current generators in the model is necessary. Thus, for pwm converters with series resistors in the v_{off} loop, the d'-model shown in figure 5.10 may be used to analyze the dc and small-signal ac behavior.

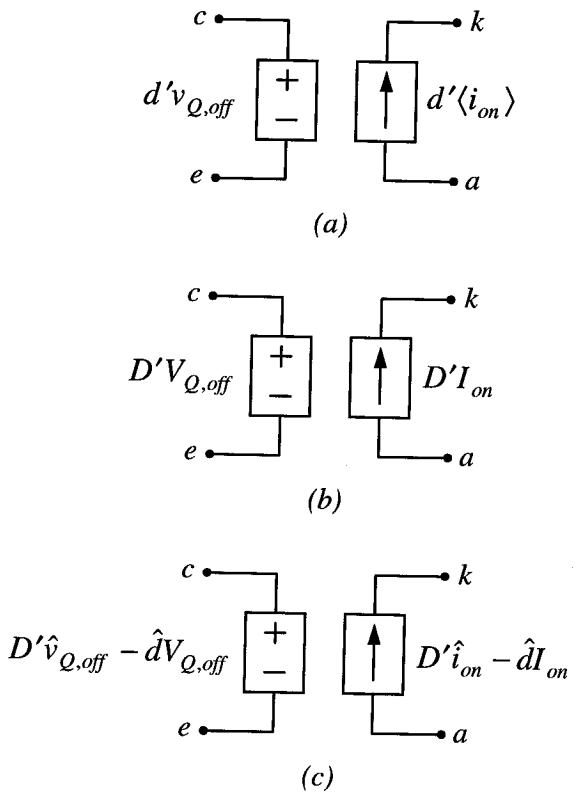


Figure 5.10: The pwm switch d'-model, valid for converters utilizing elements with series resistors in the v_{off} loop. (a) Complete large-signal, nonlinear model, (b) dc model, and (c), small-signal, linear ac model.

Example: Boost Converter with Equivalent Series Resistors

As an example, consider the problem of finding the dc conversion ratio M of the boost converter with equivalent series resistors (esr's) shown in figure 5.8(a). Arbitrarily choosing the d'-model for the analysis, the resulting dc equivalent circuit model is shown in figure 5.11, formed simply by replacing the transistor and diode switches with the dc pwm switch models in figure 5.10(b). The steady-state value of the transistor off-voltage, $V_{Q,off}$, is found easily from equation (5.4.2). Examining the dc circuit model, the steady-state values of the converter states are immediately apparent by inspection

$$V_C = V_o$$

$$I_L = \frac{V_o}{D'R} \tag{5.4.4}$$

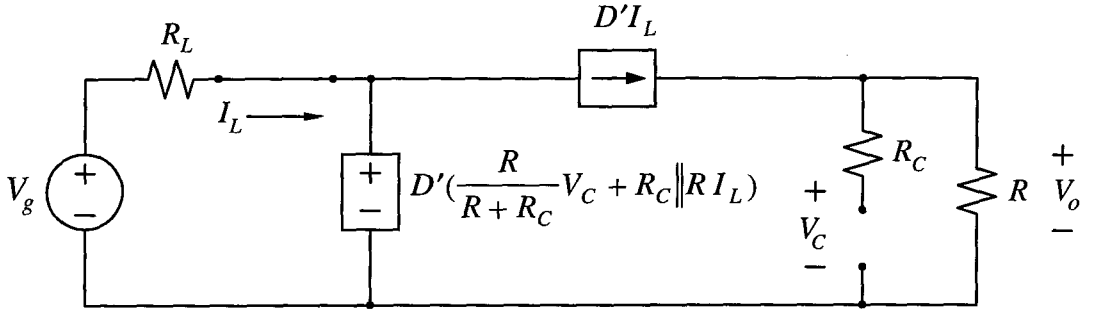


Figure 5.11: Equivalent dc circuit model of the boost converter with equivalent series resistors R_L and R_C, using the d'-model.

Solving for the dc conversion ratio, we find in only a few steps

$$M \equiv \frac{V_o}{V_g} = \frac{1}{D'} \frac{D'^2 R}{D'^2 R + R_L + DD' R_C \| R} \tag{5.4.5}$$

which is the same result reported in [2], obtained by the method of state-space averaging. If instead we had chosen to use the d-model rather than the d'-model, the results are identical. Clearly, the circuit-oriented approach of the pwm switch gives equivalent results much faster and easier than state-space averaging, and is less prone to err. In addition, since the pwm switch is a circuit-oriented approach, it provides insight into circuit operation obscured by the equation-oriented approach of state-space averaging.

5.5 Pwm Switches for Converters with Parallel Resistive Elements

Next, consider the less frequently encountered case of resistors in parallel with an element. This case is the dual of the series resistor case. Thus, in a dual manner, if a parallel resistive element is included in the i_{on} cut-set, then the on-current i_{on} in the transistor and diode will be different. In practical converters, such a resistor might be added in parallel with an inductor to provide damping of a high-Q converter resonance, or the resistor might be included to model loss due to hysteresis in the inductor core. For pwm converters with parallel resistors in the i_{on} cut-set, the on-current must be specified separately for the transistor and diode. Thus, over one switching period, $0 \le t \le T_s$, we have

$$i_{on} = \begin{cases} i_{Q,on} \; ; \; 0 \le t < dT_s \\ i_{D,on} \; ; \; dT_s < t \le T_s \end{cases} \tag{5.5.1}$$

Reflecting this change into the d-model of figure 5.9, we arrive at the general model shown below in figure 5.12, valid for converters with *both* series resistors in the v_{off} loop, and parallel resistors in the i_{on} cut-set. Note that the current generator representing the transistor has been adjusted to reflect the average transistor current, and the voltage generator representing the diode has been adjusted to reflect the average diode voltage. Similarly, the resulting general d'-model for converters with series resistors in the v_{off} loop, and parallel resistors in the i_{on} cut-set is shown on the following page in figure 5.13.

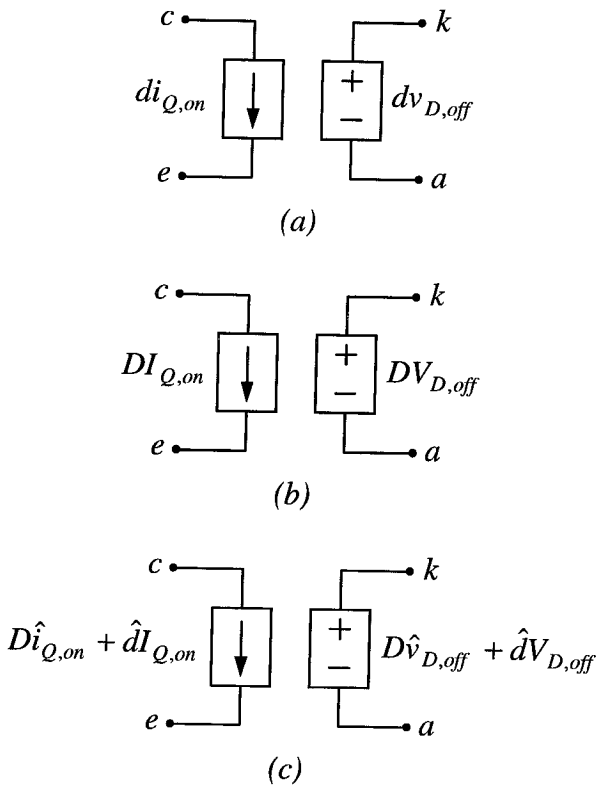


Figure 5.12: The general pwm switch d-model, for converters with series resistors in the v_{off} loop, and parallel resistors in the i_{on} cut-set. (a) large-signal nonlinear model, (b) dc model, and (c) small-signal linear ac model.

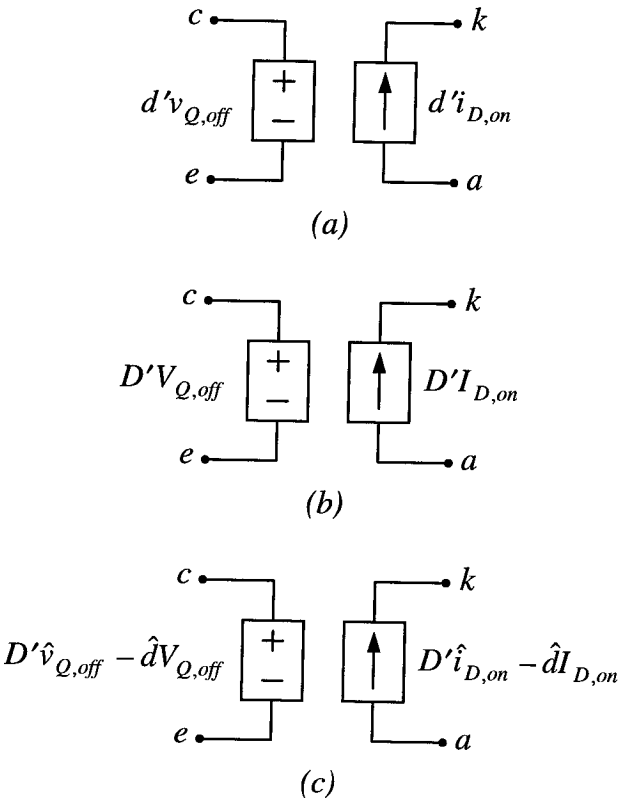


Figure 5.13 *The general pwm switch d' -model, for converters with series resistors in the v_{off} loop, and parallel resistors in the i_{on} cut-set. (a) large-signal nonlinear model, (b) dc model, (c) small-signal linear ac model.*

Example: Boost Converter with Parallel Resistor

Consider the boost converter in figure 5.14, with resistor R_P in parallel with the inductor. This resistor is clearly a member of the i_{on} cut-set, which leads to different expressions for the on-current in the transistor and the diode, as given by

$$\begin{aligned} i_{Q,on} &= i_L + \frac{v_g}{R_P} \\ i_{D,on} &= i_L + \frac{v_g - v_C}{R_P} \end{aligned} \qquad (5.5.2)$$

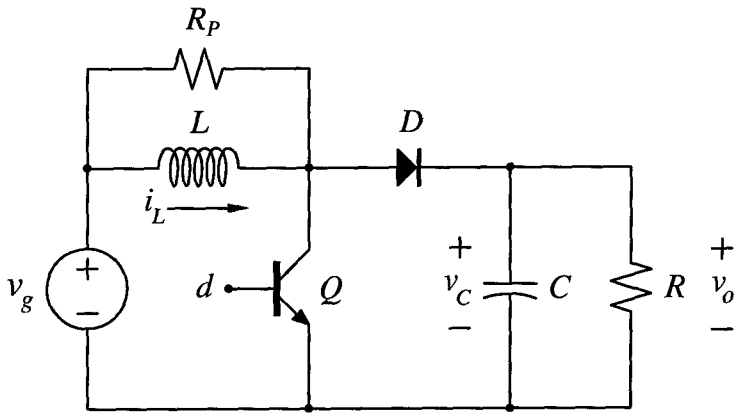


Figure 5.14: Boost converter with resistor R_P in parallel with the inductor.

Suppose we would like to derive the control-to-output transfer function for this converter. Again, arbitrarily choosing the d'-model, we begin by finding the dc operating point. The dc operating point is established by substituting the dc model of the switches, shorting the inductor, and removing the capacitor. This gives the steady-state dc operating point of the converter states

$$I_L = \frac{V_g}{D'^2}\left[\frac{1}{R} + \frac{DD'}{R_P}\right]$$
$$V_C = V_o = \frac{V_g}{D'} \tag{5.5.3}$$

It is seen from the second equation that the dc conversion ratio is unaffected by the additional parallel resistor. This observation makes sense, since in the dc model, resistor R_P is effectively shorted by the inductor.

Next, substitute the ac model of the switches into the converter, which results in the ac equivalent circuit of figure 5.15. As shown in the figure, the ac equivalent circuit can be broken into two "half-circuits," since the voltage generator representing the transistor appears effectively in series with the current generator representing the diode. Also note that because the present purpose is to derive only the control-to-output transfer function, the source representing the input voltage perturbation has been suppressed.

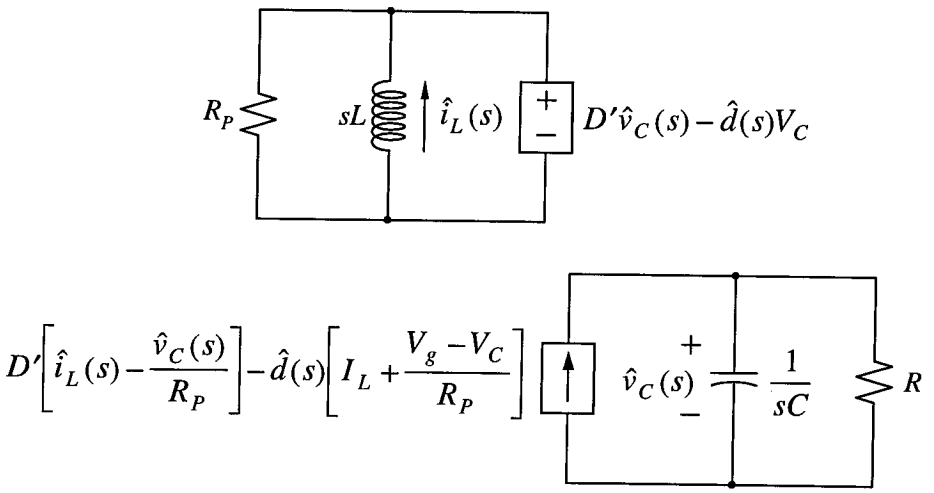


Figure 5.15: Equivalent ac circuit model for deriving the control-to-output transfer function for the boost converter with resistor R_P in parallel with the inductor.

Solving the upper half circuit for $\hat{i}_L(s)$ in terms of $\hat{v}_C(s)$, and substituting this result into the lower half circuit gives the desired control-to-output transfer function

$$\frac{\hat{v}_o}{\hat{d}}(s) = \frac{V_g}{D'^2} \frac{1 - s\frac{L}{D'^2 R}}{1 + sL\left[\frac{1}{D'^2 R} + \frac{1}{D' R_P}\right] + s^2 \frac{LC}{D'^2}} \tag{5.5.4}$$

which is exactly the same result obtained by the method of state-space averaging.

Once again, the pwm switch method yields the same results as those obtained by state-space averaging, with far less effort. The state-space averaging method is well suited for computer-aided analysis, but for hand-written analysis, the pwm switch is more efficient and provides more insight into circuit operation. Also note that state-space averaging is the method to which the pwm switch is compared to verify its validity.

5.6 Application of the Pwm Switch in Ac/Dc Rectifier Circuits

In ac/dc rectifier circuits, because the input voltage continually varies in time, the operating point of the converter continually varies in time as well. However, the

incremental models developed in this chapter are still useful, provided the operating point changes slowly with respect to the bandwidth of the closed loop control system. Hence, conditions for stability anywhere in the line cycle may be determined from the incremental dynamics at the relevant operating point. This assumption is known as the quasi-static approximation [9].

As an example, consider the ccm boost rectifier circuit below in figure 5.16. The inner current loop is a wide bandwidth control loop, which forces the average inductor current i_L to track the input voltage v_g, thereby achieving high power factor. Since the current loop is a wide bandwidth control system, and the operating point is changing in accordance with the line frequency, the incremental dynamics of the loop can be analyzed using the quasi-static approximation. Series resistor R_L has been included to illustrate its damping effect on the converter poles.

For analysis of the current loop, the transfer function of interest is the small-signal control-to-inductor current transfer function $\hat{i}_L/\hat{d}$. To find this transfer function, substitute the ac small-signal d'-model of the switches into the converter. This results in the small-signal ac model in figure 5.17(b). Solving for the control-to-inductor current transfer function, we find

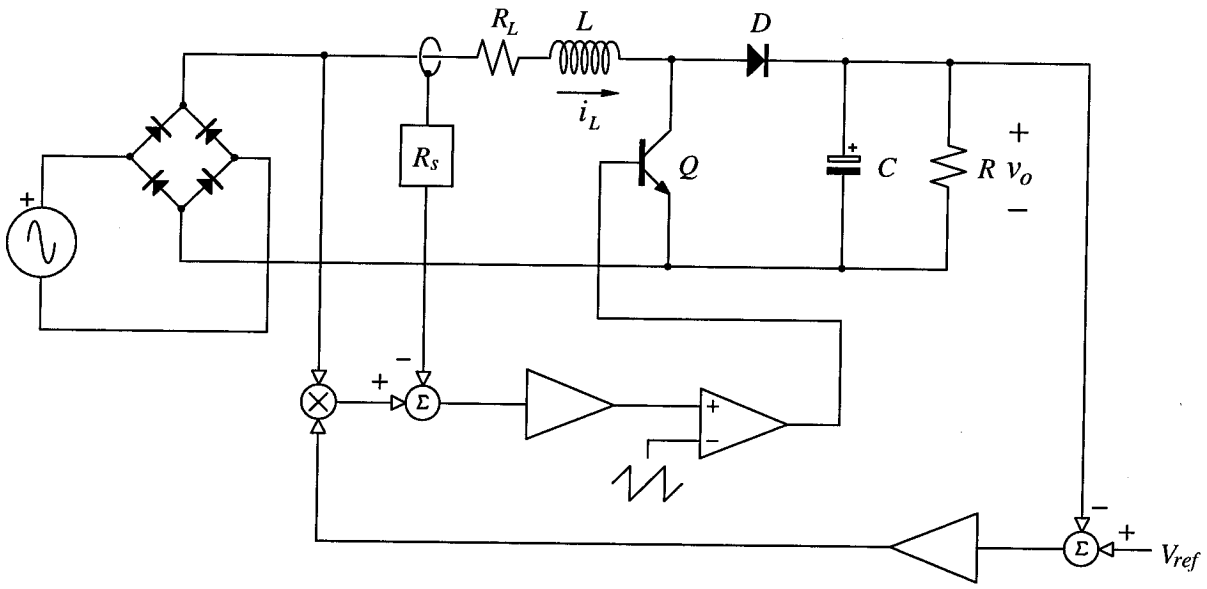


Figure 5.16: Block diagram of the popular ccm boost rectifier with wide bandwidth current loop and narrow bandwidth voltage loop.

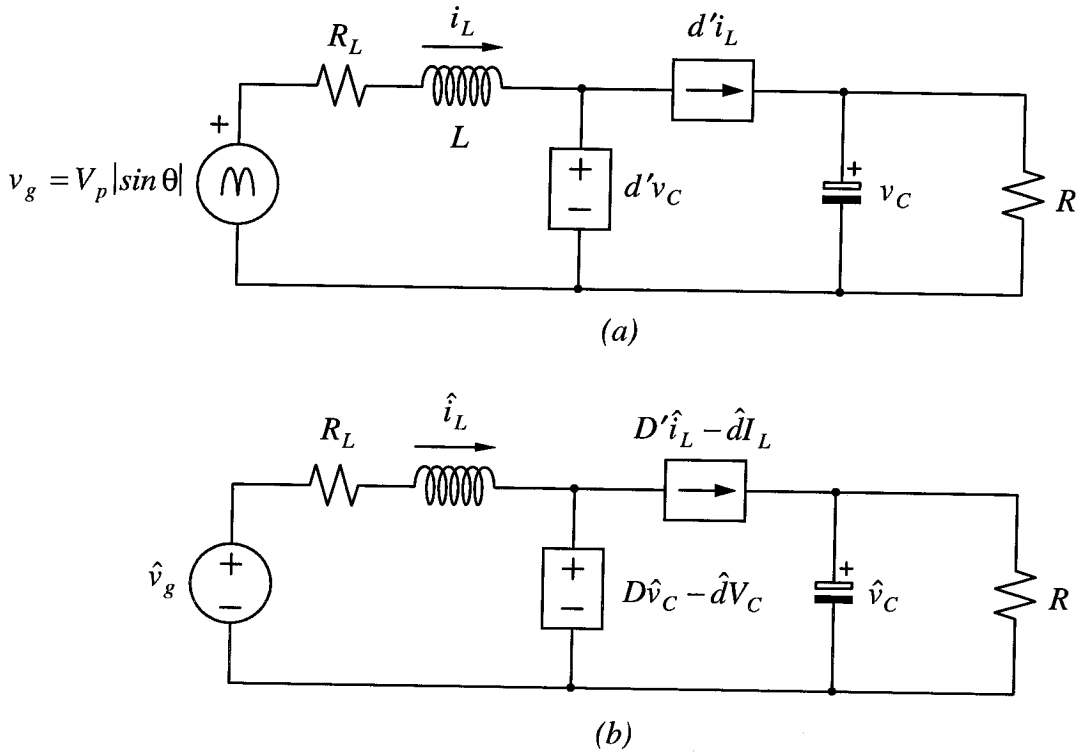


Figure 5.17: The ccm boost rectifier circuit: (a) large-signal, nonlinear, continuous, averaged model, (b) small-signal, linear averaged model

$$\frac{\hat{i}_L}{\hat{d}}(s) = \frac{V_C}{FR}\,(1 + D'I_L R/V_C)\,\frac{1 + s\dfrac{RC}{1 + D'I_L R/V_C}}{1 + s\left[\dfrac{L}{FR} + \dfrac{R_L C}{F}\right] + s^2\dfrac{LC}{F}} \tag{5.6.1}$$

where the operating point has not yet been specified, and the factor F is defined

$$F \equiv D'^2 + \frac{R_L}{R} \tag{5.6.2}$$

The instantaneous operating point varies as a function of the normalized time variable θ, and is defined at any time in the line cycle by the large-signal value of the state variables and the duty ratio complement at that instant:

$$\text{operating point} = \left\{I_L(\theta), V_C(\theta), D'(\theta)\right\} \tag{5.6.3}$$

Under the quasi-static approximation, the incremental dynamics of the system can be evaluated at each point in the line period, if the operating point is known. It is difficult if not impossible to derive this dependence exactly, but we can determine the operating point approximately, and this approximation will suffice to determine the incremental dynamics of the transfer function of interest.

If we assume that the current loop is well designed, then the inductor current should track the rectified input voltage closely, providing near-unity input power factor. The inductor current therefore varies approximately according to

$$I_L(\theta) \cong I_p |sin\,\theta| \tag{5.6.4}$$

Next, assuming that the output capacitor is sized for load balancing, and is sufficiently large to provide small output voltage ripple at twice the line frequency, the large-signal value of the capacitor voltage is in fact approximately constant

$$V_C(\theta) = V_o \cong \text{constant} \tag{5.6.5}$$

The peak inductor current I_p can be expressed in terms of known circuit quantities by equating the average input power with the dc output power, which gives

$$I_p = \frac{2M_p V_o}{R} \tag{5.6.6}$$

The large-signal variation of the duty ratio complement is determined by assuming that the line frequency component of the voltage across the inductor is approximately zero. From the large-signal model in figure 5.17(a), assuming that the capacitor voltage is constant, the large-signal variation of the complementary duty ratio is approximately

$$D'(\theta) \cong \frac{|sin\,\theta|}{M_p} \tag{5.6.7}$$

The approximate operating point variations can now be substituted into the incremental control-to-inductor current transfer function, equation (5.6.1), to show how the incremental dynamics vary over the line period:

$$\frac{\hat{i}_L}{\hat{d}}(s) = \frac{V_o}{R} \; \frac{(1+2|sin\,\theta|)}{F(\theta)} \; \frac{1 + s\dfrac{RC}{1+2|sin\,\theta|}}{1 + s\left[\dfrac{L}{F(\theta)R} + \dfrac{R_L C}{F(\theta)}\right] + s^2 \dfrac{LC}{F(\theta)}} \tag{5.6.8}$$

where the variation of the factor $F(\theta)$ is given by

$$F \equiv \frac{sin^2\,\theta}{M_p^2} + \frac{R_L}{R} \tag{5.6.9}$$

Under normal circuit operation, the factor F can vary between the extreme values of R_L/R when $D' = 0$, and $1 + R_L/R$ when $D' = 1$. Since, for high efficiency, $R_L << R$, we may write

$$F_{min} = \frac{R_L}{R} \quad ; \quad F_{max} \cong 1 \tag{5.6.10}$$

The lower bound, F_{min}, occurs when the duty ratio complement is zero (zero crossings), and the upper bound, F_{max}, occurs when the duty ratio complement is unity (peaks of the line cycle). Note that F achieves its lower bound value at every zero crossing, regardless of the value of the peak line voltage. The upper bound is achieved at the peaks of the line cycle, but only when the peak line voltage and output voltage are equal. However, it is standard design practice to design the rectifier circuit so that the output voltage just a little larger than the peak line voltage, under worst-case conditions. Thus, it is reasonable to assume that F will vary over the full range in (5.6.10), under normal operation. It is informative to express the transfer function in inverted pole-zero form [41]. The control-to-inductor current transfer function is then written

$$\frac{\hat{i}_L}{\hat{d}}(s) = \frac{V_o}{sL} \; \frac{1 + \dfrac{\omega_1}{s}}{1 + \dfrac{1}{Q}\left(\dfrac{\omega_0}{s}\right) + \left(\dfrac{\omega_0}{s}\right)^2} \tag{5.6.11}$$

where the corner frequencies and quality factor are given by

$$\omega_0 = \sqrt{\frac{F(\theta)}{LC}} \quad \omega_1 = \frac{1+2|\sin\theta|}{RC} \quad Q = \sqrt{F(\theta)}\, Q_1 \| Q_2 \quad Q_1 = R\sqrt{\frac{C}{L}} \quad Q_2 = \frac{1}{R_L}\sqrt{\frac{L}{C}} \tag{5.6.12}$$

Because the factor F varies over the range specified in (5.6.10), the resonant corner frequency ω_0 assumes minimum and maximum values according to

$$\omega_{0min} = \sqrt{\frac{R_L}{R}} \frac{1}{\sqrt{LC}} \qquad \omega_{0max} = \frac{1}{\sqrt{LC}} \tag{5.6.13}$$

which occur when the duty ratio complement is zero and unity, respectively. For typical component values, quality factor $Q_2 << Q_1$, and Q_2 therefore dominates the parallel combination $Q_1 \| Q_2$. Thus, the quality factor assumes minimum and maximum values, approximately given by

$$Q_{min} \cong \frac{1}{\sqrt{R_L R}} \sqrt{\frac{L}{C}} \qquad Q_{max} \cong \frac{1}{R_L} \sqrt{\frac{L}{C}} \tag{5.6.14}$$

which also occur when the duty ratio complement is zero and unity, respectively. For typical component values in rectifier applications, Q_{max} is usually not particularly large. Because Q_{min} is much smaller than Q_{max}, Q_{min} is almost certainly less than one-half. The poles associated with Q_{min} therefore split into two real poles, with values

$$\omega_{01} = Q_{min} \omega_{0min} \cong \frac{1}{RC} \qquad \omega_{02} = \frac{\omega_{0min}}{Q_{min}} \cong \frac{R_L}{L} \tag{5.6.15}$$

The control-to-inductor current transfer function magnitude is sketched in figure 5.17(a) and (b) under two different load conditions. The shaded region represents the area through which the asymptotes sweep under normal operation as the duty ratio varies over the full range $0 \le D \le 1$.

The most important observation is that the high frequency asymptote is static with respect to changes in the line voltage and the load. The high frequency approximation of the control-to-inductor current transfer function can therefore be written

$$\left. \frac{\hat{i}_L}{\hat{d}}(s) \right|_{hf} \cong \frac{V_o}{sL} \tag{5.6.16}$$

The fact that this approximation is invariant under changes in line and load makes the design of the current feedback loop and achieving high closed loop bandwidth easy [27].

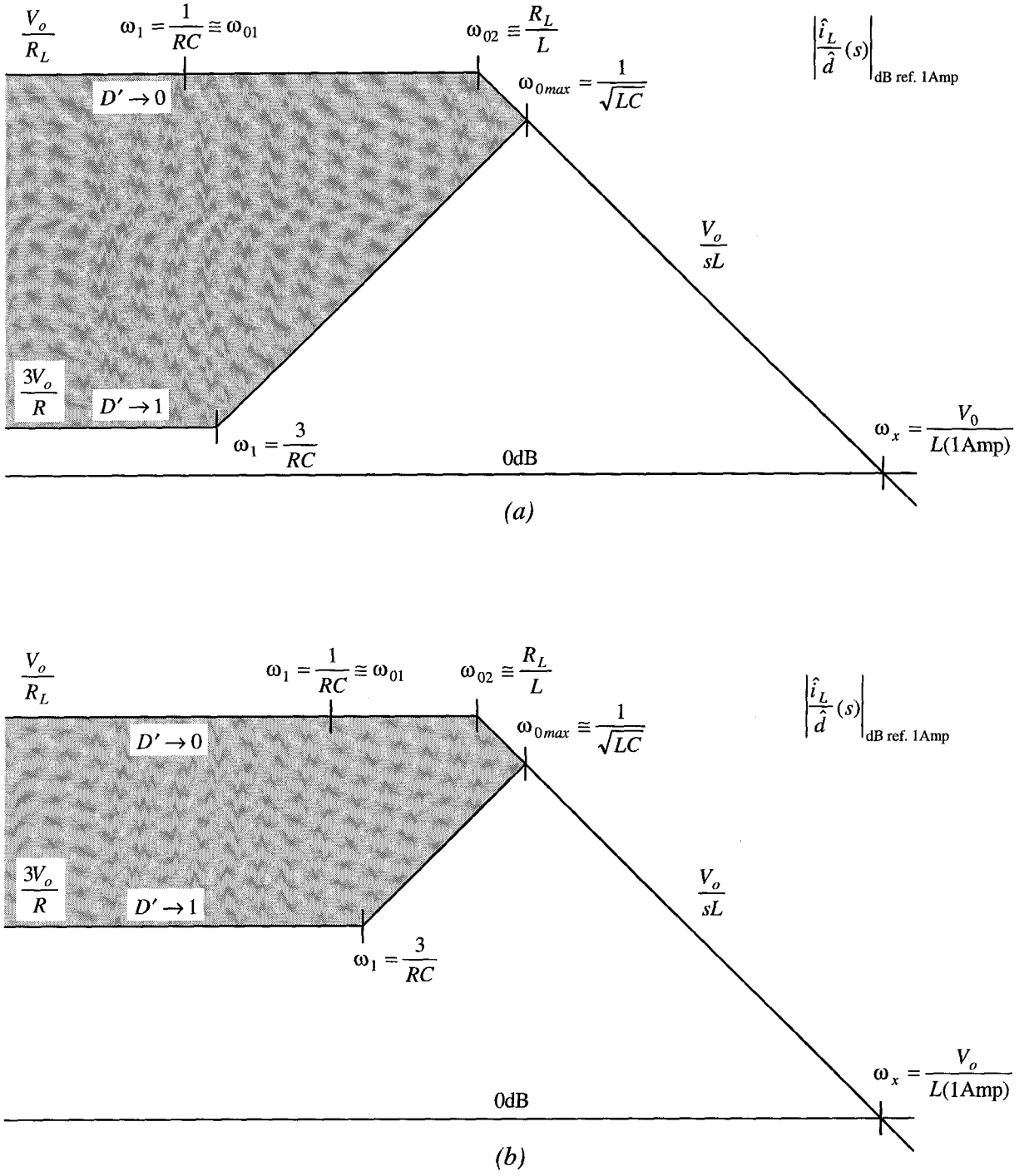


Figure 5.18: Control-to-inductor current transfer function for the boost rectifier circuit in figure 5.16: (a) large load resistor R (light load), and (b) small load resistor R (heavy load). The shaded areas indicate the locus of the asymptotes as the duty ratio varies over the full range $0 \le D' \le 1$.

Chapter 6

Pwm Switches in Discontinuous Conduction Mode

In years past, the discontinuous conduction mode (dcm) was viewed by many power circuit designers as a mode of operation to be avoided, due to higher ripple currents and altered control characteristics when operating in this mode. Therefore, most pwm power converters were designed to operate exclusively in the continuous conduction mode (ccm). However, a converter operating in dcm possesses certain properties which are especially useful in ac/dc rectifier circuits. One such property is the alleviation of the high switching loss in the power transistor caused by the reverse-recovery of the power diode. Also, in dcm, the altered control characteristics actually turn out to be advantageous, opening up new control possibilities. For these reasons, ac/dc rectifier circuits employing converters operating in dcm have gained popularity amongst power circuit designers and researchers alike.

In chapter 5, a generic pwm converter circuit (figure 5.1) was developed which exhibits the salient properties of the switching action fundamental to the operation of any ideal pwm converter in ccm. In this chapter, we extend this concept to ideal pwm converters operating in dcm. Recall, from chapter 5, the transformer-like relationship between the transistor and diode switches operating in ccm. In this chapter, it is shown that crossing the boundary from ccm to dcm dramatically changes this relationship, making possible simple control strategies for ac/dc rectifier circuits utilizing converters operating in dcm, not possible with the same converters operating in ccm.

In ccm, the off-voltage v_{off} and on-current i_{on} are both constrained to have small ripple. To be precise, to operate in ccm, the ripple component of the off-voltage v_{off} and on-current i_{on} must be small enough so that both v_{off} and i_{on} are never zero in the course of the switching cycle. If the ripple component of on-current i_{on} is large enough

that i_{on} falls to zero in the course of the switching cycle, and off-voltage v_{off} does not, then the converter operates in the "discontinuous inductor current mode" (dicm) [10]. This operating mode is also often referred to simply as the "discontinuous conduction mode" (dcm). This simplification owes partly to the fact that the dcm (dicm) was the first discontinuous operating mode discovered, and partly to the fact that it is certainly the most frequently encountered discontinuous operating mode.

In a dual manner, if the ripple component of the off-voltage v_{off} is large enough that v_{off} falls to zero in the course of the switching cycle, and the on-current i_{on} does not, then the converter operates in the "discontinuous capacitor voltage mode" (dcvm). Finally, if both the on-current i_{on} and off-voltage v_{off} fall to zero in the course of the switching cycle, the converter operates in the "discontinuous quasi-resonant mode" (dqrm). Because of its importance in current shaping applications with constant voltage energy storage, the emphasis here is on dicm, and dcvm and dqrm will not be discussed further. Also, the discontinuous inductor current mode will henceforth be referred to simply as the discontinuous conduction mode (dcm).

6.1 Pwm Switches in Discontinuous Conduction Mode

Recall how in ccm the switches operate in complementary fashion such that when the transistor is on, the diode is off, and vice-versa. Conduction of on-current i_{on} thus alternates between the transistor and diode, one of which conducts always. Hence, in ccm, there are only two intervals to consider; one called the d-interval, during which the transistor is on and the diode is off, and the other called the d'-interval, during which the diode is on and the transistor is off.

In dcm, there are three intervals to consider. In the first interval, called the d-interval or "charging" interval, the transistor is on and the diode is off, analogous to the d-interval in ccm. The second interval is called the d_2-interval or "decay" interval, during which the diode is on and the transistor is off, analogous to the d' interval in ccm. The third interval is called the d_3-interval or "idle" interval, during which both the transistor and diode are off. It is important to note that this third interval arises not because there is any topological difference between the converter operating in ccm and the converter

operating in dcm, but rather because the converter is operated with large ripple in on-current i_{on}.

Because on-current i_{on} is responsible for the determination of the operating mode, we need to look at this current more carefully. The generic pwm converter circuit from chapter 5 appears in figure 6.1(a), with on-current i_{on} and off-voltage v_{off} indicated. Equivalent inductance L_{on} is used to represent the effect all of the inductors in the i_{on} cut-set, and is given by

$$L_{on} = L_1 \| L_2 \| \ldots \| L_n \quad \text{where} \quad L_{on} = \{L_1, L_2, \ldots, L_n\} \tag{6.1.1}$$

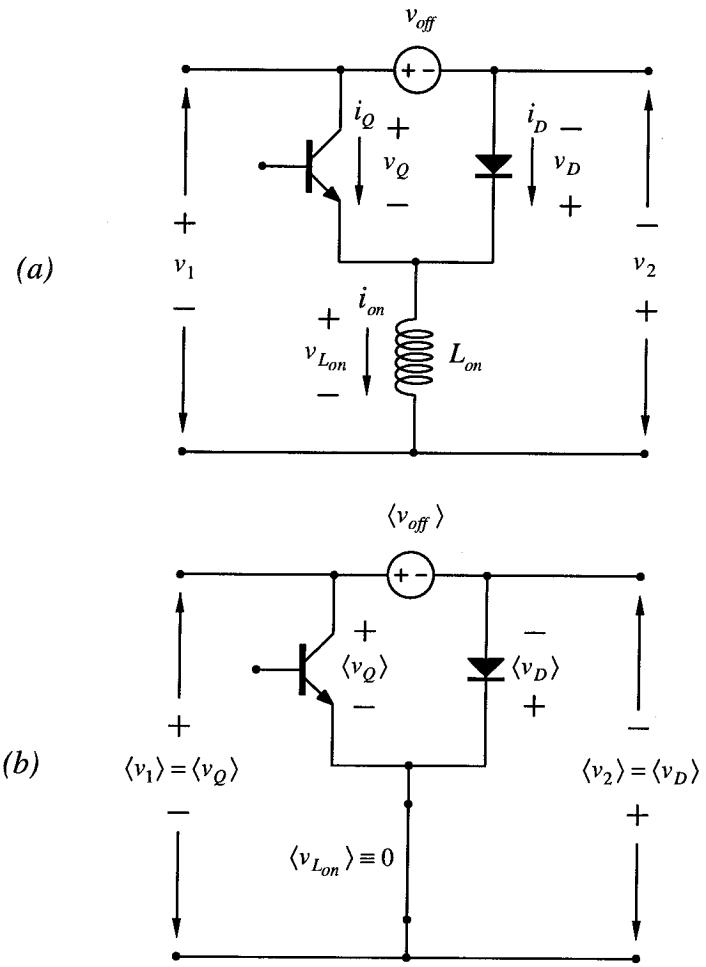


Figure 6.1: (a) Generic two switch pwm converter circuit, and (b), the same circuit after invoking the switching frequency average operator.

The inductors $L_1, L_2, \ldots, L_n$ comprising the i_{on} cut-set can be represented by a single inductance L_{on} in the generic circuit because all inductors in the i_{on} cut-set share the identical voltage waveform [4].

Invoking the switching frequency average operator on the circuit of figure 6.1(a), we arrive at the averaged circuit of figure 6.1(b). It is clear from the averaged circuit that average voltage $\langle v_1 \rangle$ is equal the average transistor voltage, and average voltage $\langle v_2 \rangle$ is equal to the average diode voltage. By assumption, voltages v_1 and v_2 are constrained to have small ripple, and therefore v_1 and v_2 can be thought of as stiff dc voltages. The voltage across the equivalent inductance over one switching cycle is therefore

$$v_{L_{on}} = L_{on}\frac{di_{on}}{dt} = \begin{cases} \langle v_Q \rangle & ; \ 0 \le t \le dT_s \\ -\langle v_D \rangle & ; \ dT_s \le t \le (d+d_2)T_s \\ 0 & ; \ (d+d_2)T_s \le t \le T_s \end{cases} \tag{6.1.2}$$

Typical voltage and current waveforms for the switches and equivalent inductance are shown in figure 6.2. From the geometry of the waveforms, the average currents can be expressed

$$\begin{aligned} \langle i_{on} \rangle &= \frac{1}{2}(d+d_2)I_{pk} \\ \langle i_Q \rangle &= \frac{1}{2}dI_{pk} \\ \langle i_D \rangle &= \frac{1}{2}d_2 I_{pk} \end{aligned} \tag{6.1.3}$$

where the peak current I_{pk} is given by

$$I_{pk} = \frac{\langle v_Q \rangle}{L_{on}}dT_s \tag{6.1.4}$$

We already have enough information to compute the average transistor current

$$\langle i_Q \rangle = \frac{1}{2}dI_{pk} = \frac{d^2 T_s}{2L_{on}}\langle v_Q \rangle \tag{6.1.5}$$

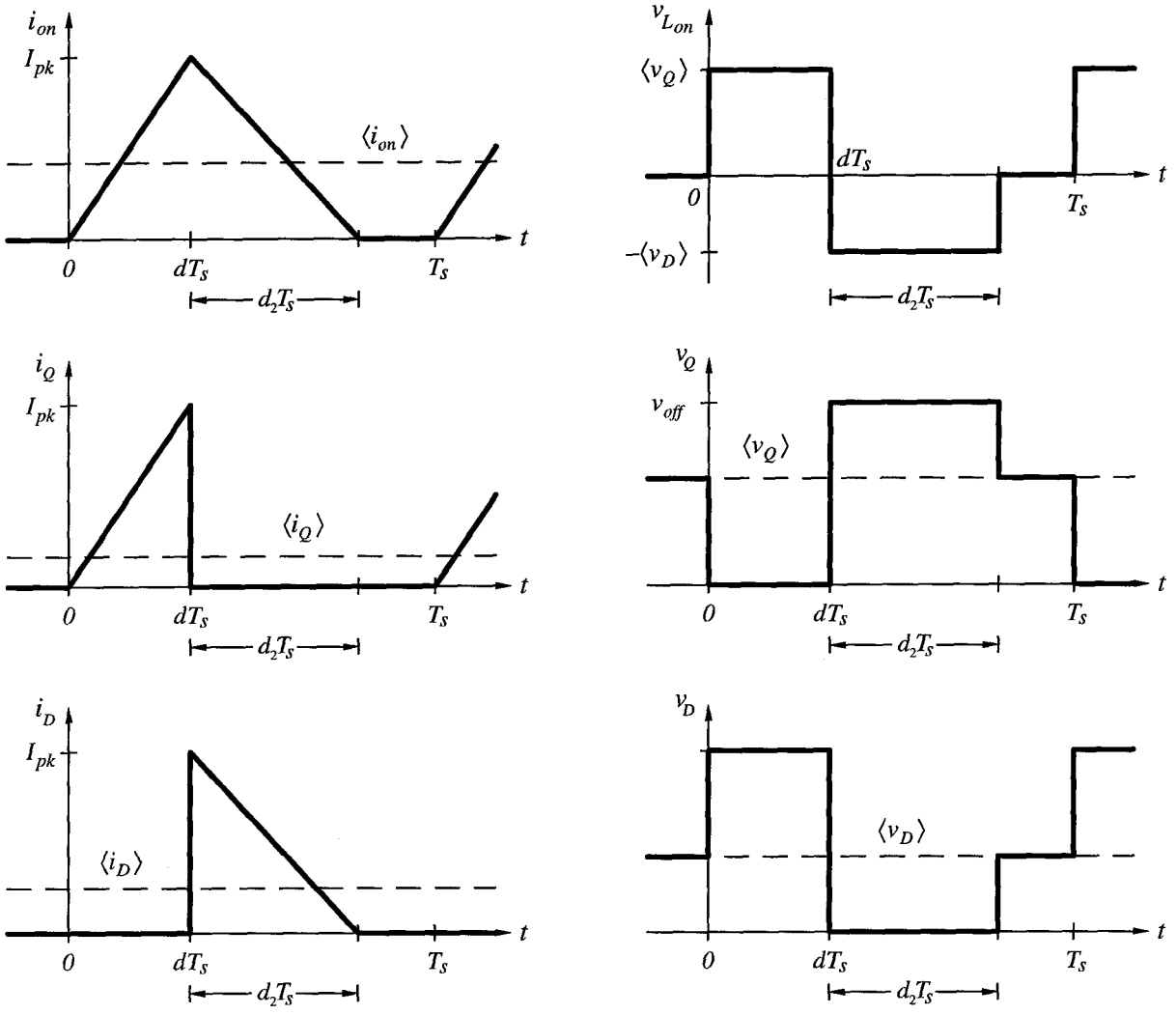


Figure 6.2: Ideal pwm switch and inductor waveforms in dcm.

This is a most remarkable result. It says that the average transistor current is related to the average transistor voltage by a controllable factor, and is independent of the average diode voltage and current. In contrast, recall how in ccm the average current in the transistor and diode are intimately tied via the ideal transformer relationships. This property in dcm makes possible control strategies for ac/dc rectifier applications not possible with converters operating in ccm.

From the geometry of the on-current waveform, decay interval d_2 can be written

$$d_2 = d\frac{\langle v_Q \rangle}{\langle v_D \rangle} \tag{6.1.6}$$

The average diode current is then easily computed

$$\langle i_D \rangle = \frac{1}{2} d_2 I_{pk} = \frac{d^2 T_s}{2L_{on}} \frac{\langle v_Q \rangle^2}{\langle v_D \rangle} \tag{6.1.7}$$

Taking the ratio of $\langle i_D \rangle$ to $\langle i_Q \rangle$, and combining with equation (6.1.6) gives

$$\frac{\langle i_D \rangle}{\langle i_Q \rangle} = \frac{\langle v_Q \rangle}{\langle v_D \rangle} = \frac{d_2}{d} \tag{6.1.8}$$

This is very similar to the ccm case in chapter 5, where it was shown that the average switch voltage and current in ccm are related by the ideal transformer equations. A comparison is depicted below in figure 6.3. However, the ideal transformer equivalent circuit in dcm is not immediately useful like it is in ccm. In dcm, the decay interval d_2 is a consequence of average voltages $\langle v_Q \rangle$ and $\langle v_D \rangle$, not vice-versa. Thus, the value of d_2 "adjusts" to accommodate average voltages $\langle v_Q \rangle$ and $\langle v_D \rangle$. This is in sharp contrast to the transformer equivalent circuit in ccm, where the fixed duty ratio fixes the relationship between the average voltage and current in the switches. For this reason, in dcm, we will find a dependent source equivalent circuit representation of equations (6.1.5) and (6.1.7) more useful. The resulting continuous nonlinear equivalent circuit model for pwm switches operating in dcm is shown in figure 6.4.

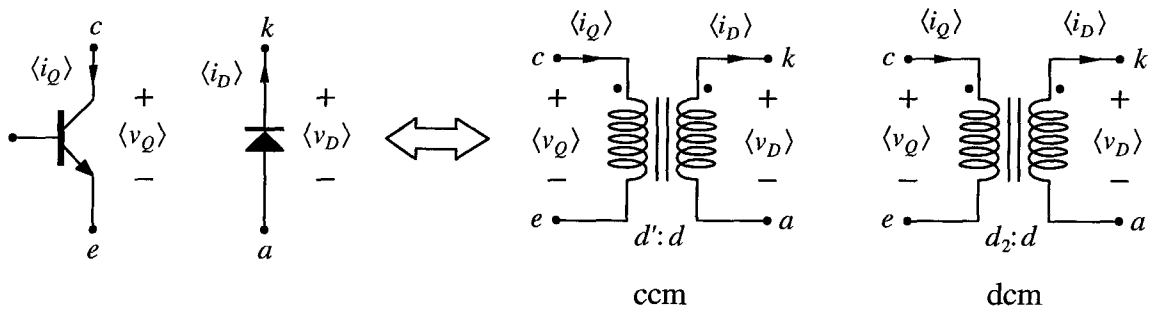


Figure 6.3: Pwm switches, and a comparison of the ideal transformer equivalent circuits in ccm and dcm.

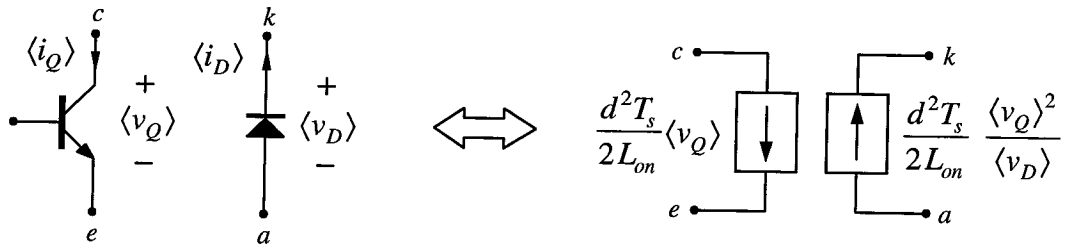


Figure 6.4: Nonlinear dependent source equivalent circuit model of pwm switches in dcm, suitable for small-signal and large-signal converter modeling.

Now, consider the equivalent inductance L_{on}. Invoking the switching frequency average operator on the inductor voltage gives

$$\langle v_{L_{on}} \rangle = \langle L_{on} \frac{d}{dt} i_{on} \rangle = L_{on} \frac{d}{dt} \langle i_{on} \rangle \tag{6.1.9}$$

where we have taken advantage of the linearity of the switching frequency average and differentiation operators. In dcm however, over any switching cycle, the volt-seconds applied to the inductor must be zero. Thus, we have

$$\langle v_{L_{on}} \rangle \equiv 0 \tag{6.1.10}$$

This result implies the disappearance of the converter state associated with i_{on}, thereby reducing the system order by one [3]. For pwm converters with a single inductor, this means that the inductor may be replaced by a short circuit in the averaged model.

In the derivation of this nonlinear model, no small-signal assumption was made, and it is therefore useful for both small-signal and large-signal converter modeling. Though the model is nonlinear, it is however continuous, making it extremely efficient for use in computer simulations.

6.2 Dc and Small-Signal Ac Models for Pwm Switches in Dcm

The same process of perturbation and linearization used for the ccm case in chapter 5 can be applied to the nonlinear pwm switch model in dcm to develop equivalent dc a nd small-signal linear ac models. Perturbation and linearization of the nonlinear model in figure 6.4 yields a complete linear model, which can be further broken down into a dc

model and a linear small-signal ac model. To begin, the nonlinear model of figure 6.4 is perturbed according to

$$d = D + \hat{d} \quad \langle v_Q \rangle = V_Q + \hat{v}_Q \quad \langle v_D \rangle = V_D + \hat{v}_D \tag{6.2.1}$$

which, after linearization and separation into dc and ac components, yields the dc and small-signal ac equivalent circuits shown below in figure 6.5, which are similar to those derived in [19].

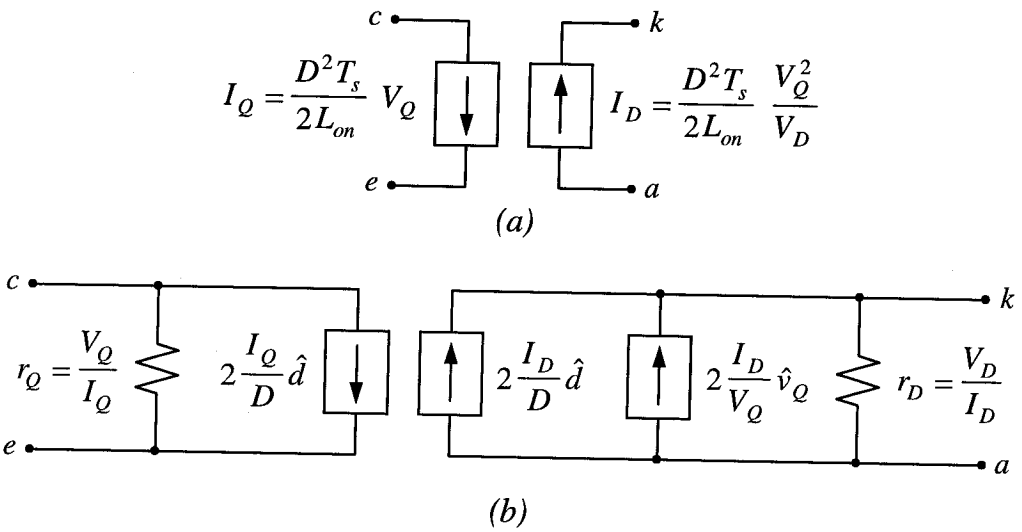


Figure 6.5: (a) Dc circuit model, and (b) small-signal ac circuit model of pwm switches operating in dcm.

Example: Ideal Buck-Boost Converter in Dcm

As an example, consider the problem of deriving the small-signal control-to-output transfer function for the ideal buck-boost dc/dc converter in dcm. The derivation of the pwm switch for converters in dcm is based on the generic pwm converter in figure 6.1. By assumption there are no lossy elements in the converter, and therefore the pwm switch as derived applies only to ideal pwm converters. In chapter 5, the pwm switch for ideal pwm converters operating in ccm was extended to pwm converters with lossy resistive elements, but the problem of finding a similar correction for pwm converters operating in dcm remains unsolved. However, for the ideal buck-boost converter in figure 6.6, the pwm switch in dcm as derived is appropriate.

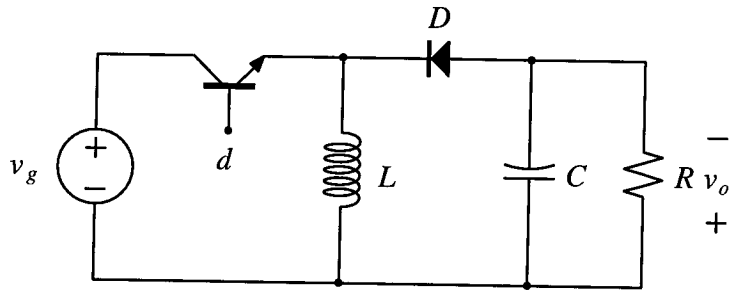


Figure 6.6: Ideal buck-boost converter.

The analysis begins by identifying equivalent inductance L_{on}. Since the buck-boost converter contains only one inductor, this step is trivial. Next, the dc circuit model of figure 6.5(a) is substituted into the circuit for the transistor and diode, and the capacitor is removed. These steps lead to the dc equivalent circuit in figure 6.7(a), from which the operating point is determined

$$\frac{D^2 T_s}{2L}\frac{V_g^2}{V_o} = \frac{V_o}{R} \quad \Rightarrow \quad M \equiv \frac{V_o}{V_g} = \frac{D}{\sqrt{K}} \tag{6.2.2}$$

where the "conduction parameter" K is defined

$$K \equiv \frac{2L_{on}}{RT_s} \tag{6.2.3}$$

For closed loop considerations, the operating point variables are solved in terms of the variables $\{M, K, V_o, R\}$, as shown in figures 6.7(b) and (c). The complete small-signal linear ac circuit model in figure 6.7(b) is exactly the same as the ac small-signal circuit model derived in [3], using the state-space averaging approach. Finally, from the reduced small-signal linear ac circuit model of figure 6.7(c), the desired control-to-output transfer function is given by

$$\frac{\hat{v}_o}{\hat{d}}(s) = \frac{V_o}{M\sqrt{K}} \; \frac{1}{1 + s/\omega_p} \quad ; \quad \omega_p = \frac{2}{RC} \tag{6.2.4}$$

which completes the example.

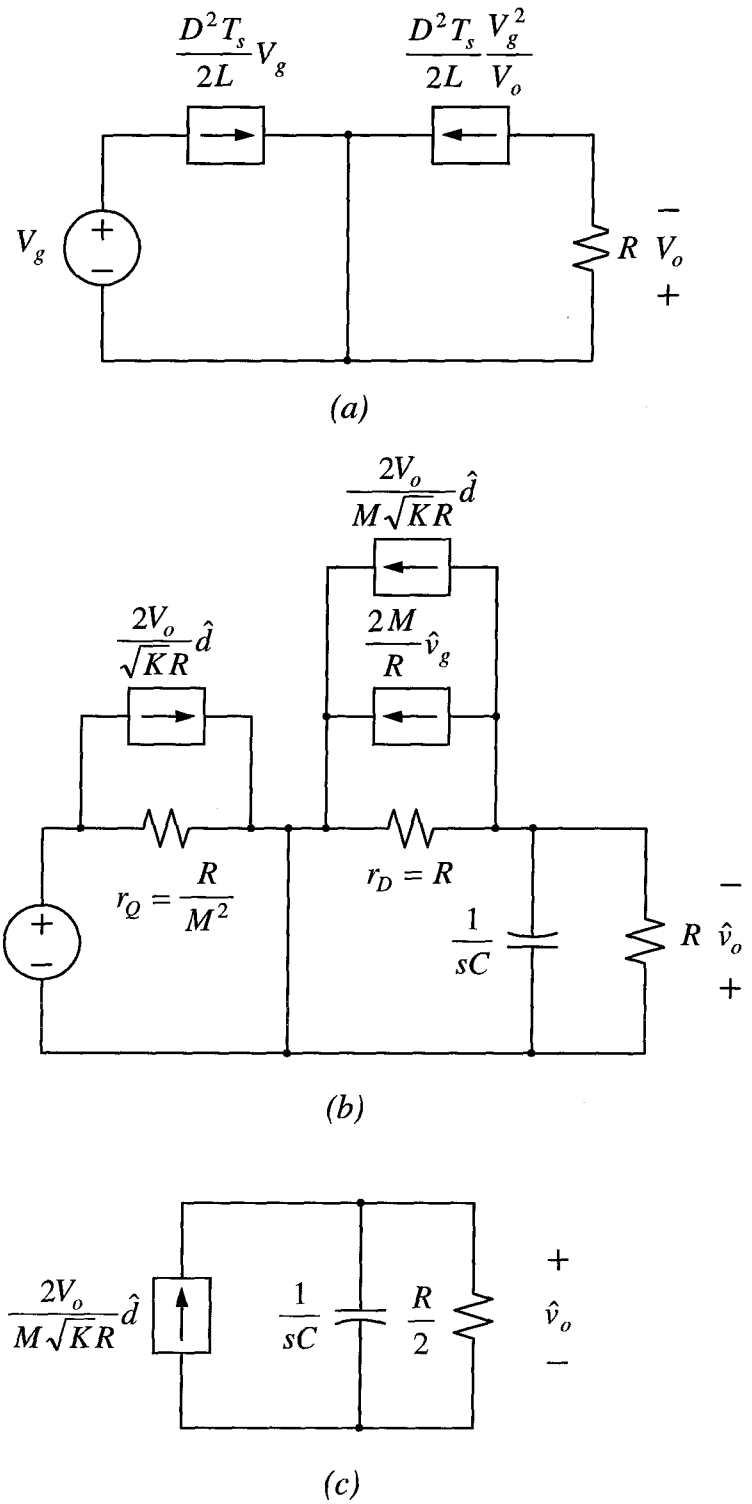


Figure 6.7: Circuit models for the buck-boost converter in dcm: (a) dc circuit model, (b) complete small-signal linear ac model, and (c) small-signal linear ac model for computation of the control-to-output transfer function.

6.3 Application of the Nonlinear Model in Ac/Dc Rectifier Circuits

The nonlinear model for pwm switches in dcm in figure 6.4 is useful in the analysis of ac/dc rectifier circuits because no small-signal assumption is made in its derivation. Hence, it can be used to accurately model the average switch behavior despite the large-signal variations encountered in ac/dc rectifier circuits. As an example, consider the buck-boost rectifier circuit with constant power load, shown below in figure 6.8. The low-pass filter is designed to attenuate ripple current generated by the converter at the switching frequency and its harmonics, and also to have little effect at the line frequency. The voltage at the converter input can therefore be approximated by a rectified sine wave with peak voltage equal to the peak of the line voltage. This results in the large-signal nonlinear circuit model shown in figure 6.9. From the model, the average current flowing into the converter input is

$$i_g(\theta) = \frac{d^2 T_s}{2L} v_g(\theta) \tag{6.3.1}$$

If the duty ratio is maintained constant, then the input current is proportional to the input voltage. As shown in chapter 2, proportional input current implies unity input power factor, regardless of the input voltage waveshape. In this case, because input current tracking occurs without exercising any control, the input current shaping is said

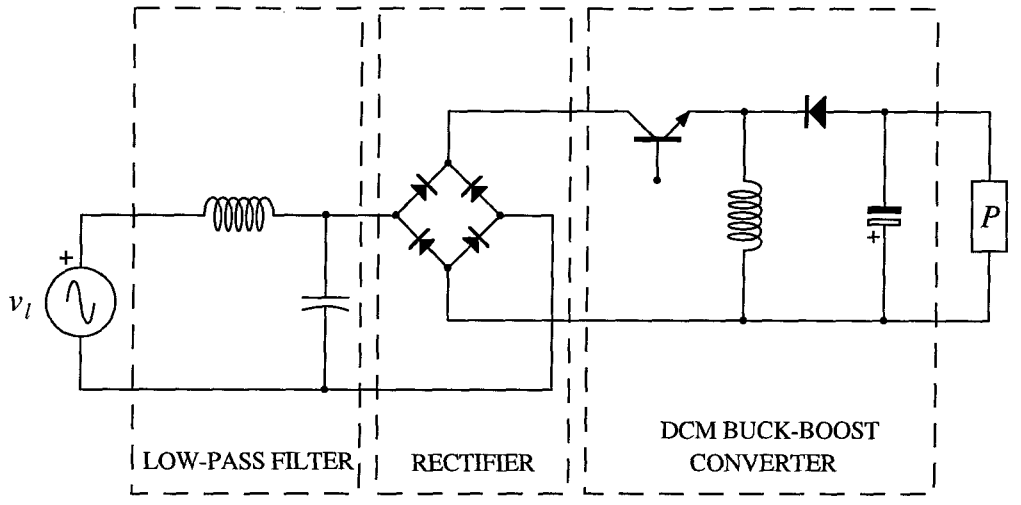


Figure 6.8: The buck-boost rectifier circuit

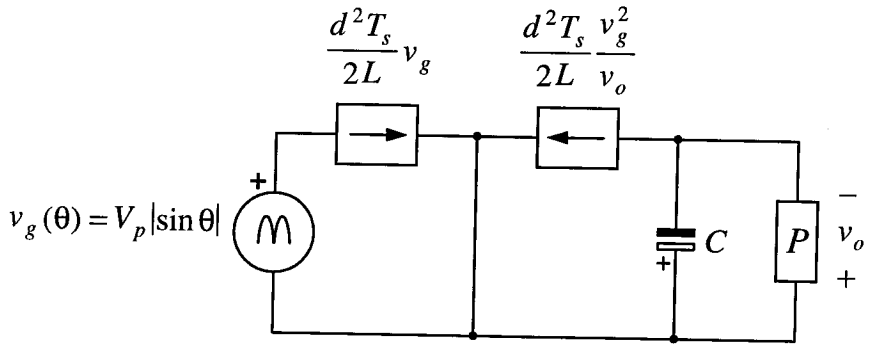


Figure 6.9: Continuous, nonlinear model of the dcm buck-boost rectifier.

to be "automatic." Also, because the input current is directly proportional to the input voltage, the input current shaping is said to be "ideal." Hence, the buck-boost converter in dcm is an example of an "ideal automatic input current shaper."

The model in figure 6.9 is nonlinear, but continuous. The continuity of the model makes it extremely efficient for the purpose of circuit simulation. In addition, the model is useful for both small-signal and large-signal simulations. However, this model is valid only when the converter operates in dcm, and we must assure ourselves that this is indeed the case when we use it. Rectifier circuits are normally designed to operate exclusively in one operating mode, and the analysis necessary to determine the converter operating mode is the subject of the next chapter.

Chapter 7

Operating Modes in Ac/Dc Rectifier Circuits

In the design of any basic electric power conversion system, the primary design requirements are the input voltage type (ac or dc) and voltage range, the number of outputs and type of each output, and the load power range for each output. With this information, the circuit designer chooses a converter topology or topologies which can best meet these design requirements while adhering to, minimizing, or maximizing some other secondary constraints (efficiency, cost, size, weight, etc.). In choosing a converter topology, the designer simultaneously decides, often not even consciously, on which mode or modes the converter or converters will operate in. Hence, the operating mode is a primary design consideration in the design of any power conversion system, perhaps second to only the converter topology itself.

The transition from operation in ccm to operation in dcm occurs when the ripple in the on-current i_{on} becomes large compared to the average on-current $\langle i_{on} \rangle$, causing the diode current to reach zero prior to the end of the switching cycle, thereby terminating diode conduction. Thus, in dcm, a third switching interval is created during which both the transistor and diode are off.

It is shown in this chapter that the determination of the boundary between operating modes in ac/dc rectifier circuits is very similar to that in dc/dc converter circuits. The key difference is in properly accounting for the variation of the operating point over the line period in the ac/dc rectifier circuit. With this in mind, rather than proceeding directly to the analysis of the discontinuous conduction mode in ac/dc rectifier circuits, we first consider dcm operation in dc/dc conversion circuits, and we will view the ac/dc case as an extension.

To be complete, we make use of ac and dc circuits [22,23], to generate a complete set of dc circuits for pwm converters (as defined in chapter 5) utilizing a single transistor and diode. The "dc circuit" of a pwm converter is a dc equivalent circuit representing the dc conversion properties only. The analysis shows that there are eight such dc circuits for pwm converters in this class, with eight corresponding unique dc conversion ratios. For each of these dc circuits, knowing the conversion ratio in ccm, the conversion ratio in dcm can be determined using the concept of equivalent duty ratio [1,5]. The implication of this analysis is that all pwm converters which share the same conversion ratio in ccm, also share the same conversion ratio in dcm.

7.1 Ac & Dc Circuits

The ac and dc circuits concept was introduced as a very general and powerful means of pwm converter analysis and synthesis [23]. For the present purpose, we consider only the special case of two-switch pwm converters derived from one particular ac circuit. Using this method, it is a simple matter to generate all possible dc circuits possessing the given ac circuit, thereby generating all possible dc conversion ratios for pwm converters employing one transistor and one diode. With this complete set of possible conversion ratios in ccm, we then derive the corresponding set in dcm.

Ac Circuits

The ac circuit illustrates the relationship between the switches in a pwm converter at high frequencies. The ac circuit of a pwm converter is formed by replacing each element in the converter by its high frequency equivalent; i.e., by shorting all capacitors, removing all inductors, and suppressing the input voltage source v_g. From the definition of a pwm converter given in chapter 5, the load appears in a loop of capacitors and possibly v_g. The load is therefore effectively shorted and does not appear in the ac circuit. Hence, the ac circuit contains only switches. It can be shown [22] that all pwm converters meeting the definition given in chapter 5 are in fact derivatives of the very same ac circuit, shown in figure 7.1.

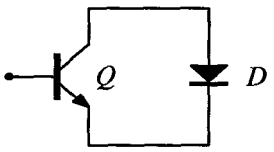


Figure 7.1: The ac circuit of all two-switch pwm converters meeting the definition in chapter 5.

Dc Circuits

The dc circuit illustrates the steady-state dc relationship between elements in a pwm converter. Since the average voltage across an inductor is zero in steady-state, as is the average current through a capacitor, the steady-state (or dc) behavior of these elements is that of a short circuit and an open circuit, respectively. Thus, the dc circuit of a pwm converter is formed by shorting all inductors and removing all capacitors. Hence, the dc circuit contains the source, the switches, and the load only. The generation of all possible dc circuits for two-switch pwm converters can be performed by inserting the switches in every position and orientation in the circuit consisting of the source and load, as shown in figure 7.2. Note, however, that all configurations are not dc circuits of valid pwm converters, and the validity of each configuration must be verified. To verify the validity of a particular dc circuit configuration, we assume, without loss of generality, that the dc circuit is the dc circuit of a pwm converter operating in ccm. Recall that in ccm, the average or dc component of the switch voltages and currents are related by the ideal transformer equations

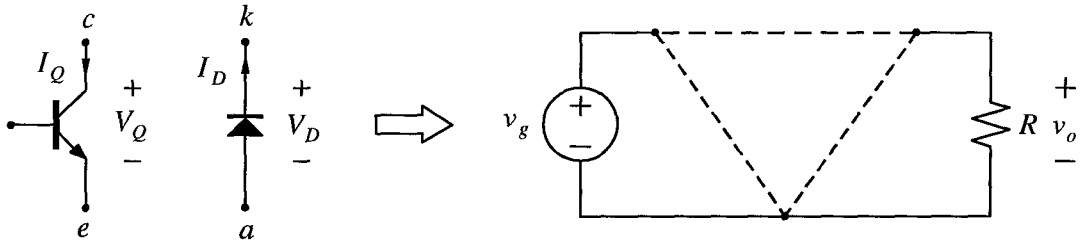


Figure 7.2: Dc circuit candidates for all two-switch pwm converters are generated by inserting the switches in both orientations in the three positions shown.

$$V_Q = \frac{D'}{D} V_D$$
$$I_Q = \frac{D}{D'} I_D \qquad (7.1.1)$$

In addition, the average voltages and currents for the switched are subject to the constraints

$$V_Q > 0$$
$$I_Q > 0$$
$$V_D > 0 \qquad (7.1.2)$$
$$I_D > 0$$

with reference directions as indicated in figure 7.2. If, after substituting either relation in (7.1.1) into the dc circuit, constraints (7.1.2) are satisfied, then that dc circuit is the dc circuit of a valid pwm converter. The astute reader will have noticed that in the general dc circuit of figure 7.2, it was assumed *a priori* that the dc circuit for a two switch pwm converter contains three nodes. In fact, it is shown in [22] that this is indeed the case. However, if possible dc circuits with two or four nodes are investigated by attempting to satisfy equations (7.1.1) and (7.1.2), it is found that none of these circuits satisfy these constraints.

After completing the process of substituting (7.1.1) and verifying (7.1.2), a total of eight dc circuits of valid pwm converters with one transistor and one diode are found, and these are shown in figure 7.3. It is interesting to note that only the buck-type converters (i.e., converters possessing the dc circuit in figure 7.3(a)) permit the entire duty ratio range $0 \le D \le 1$. In all other converters, the duty ratio is restricted in some way. Examples of pwm converter realizations corresponding to each of these dc circuits is shown in figure 7.4. Note that these pwm converter realizations are not unique, since many pwm converters may possess the same dc circuit.

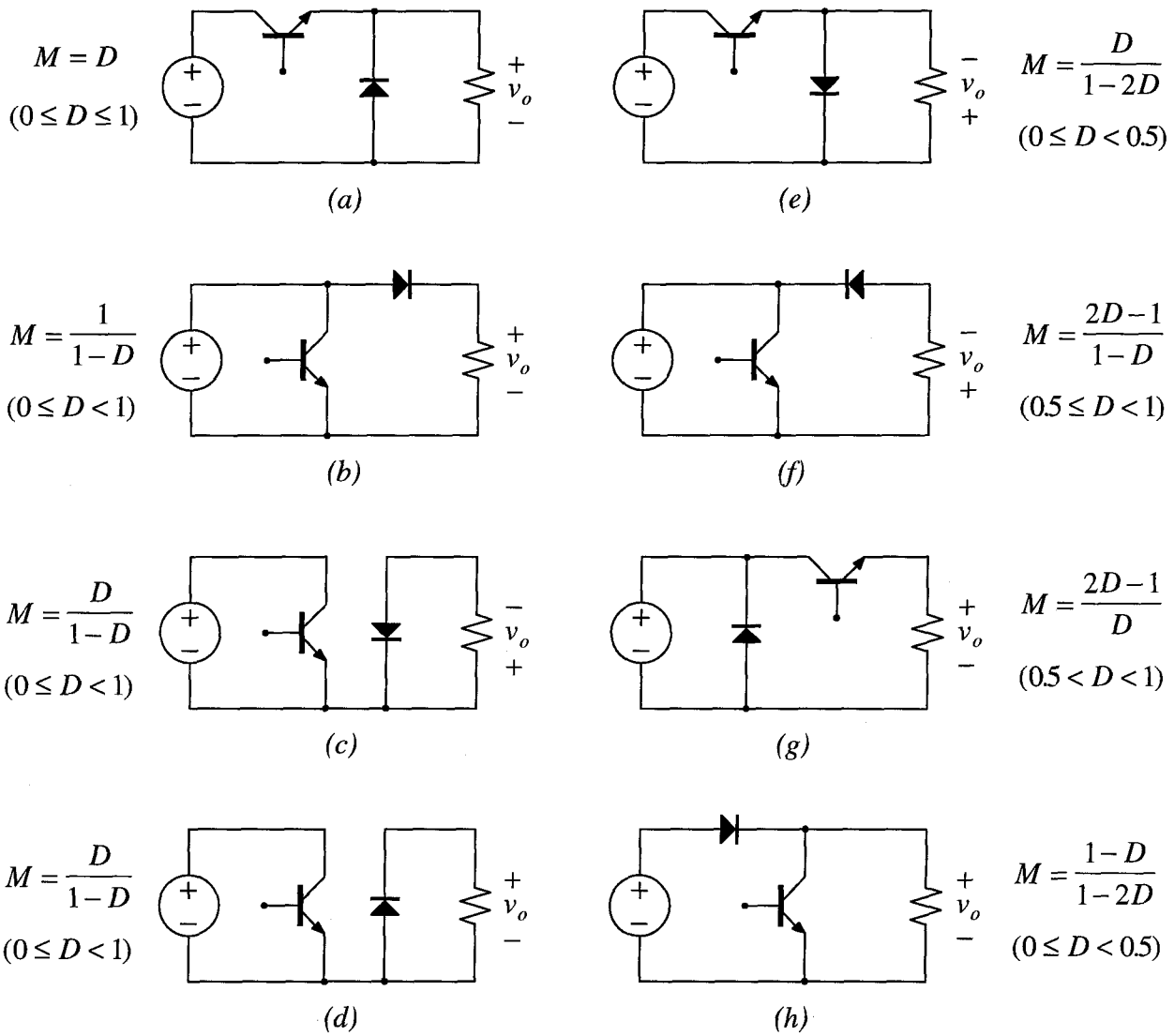


Figure 7.3: The complete set of eight valid dc circuits for two-switch pwm converters employing one transistor and one diode.

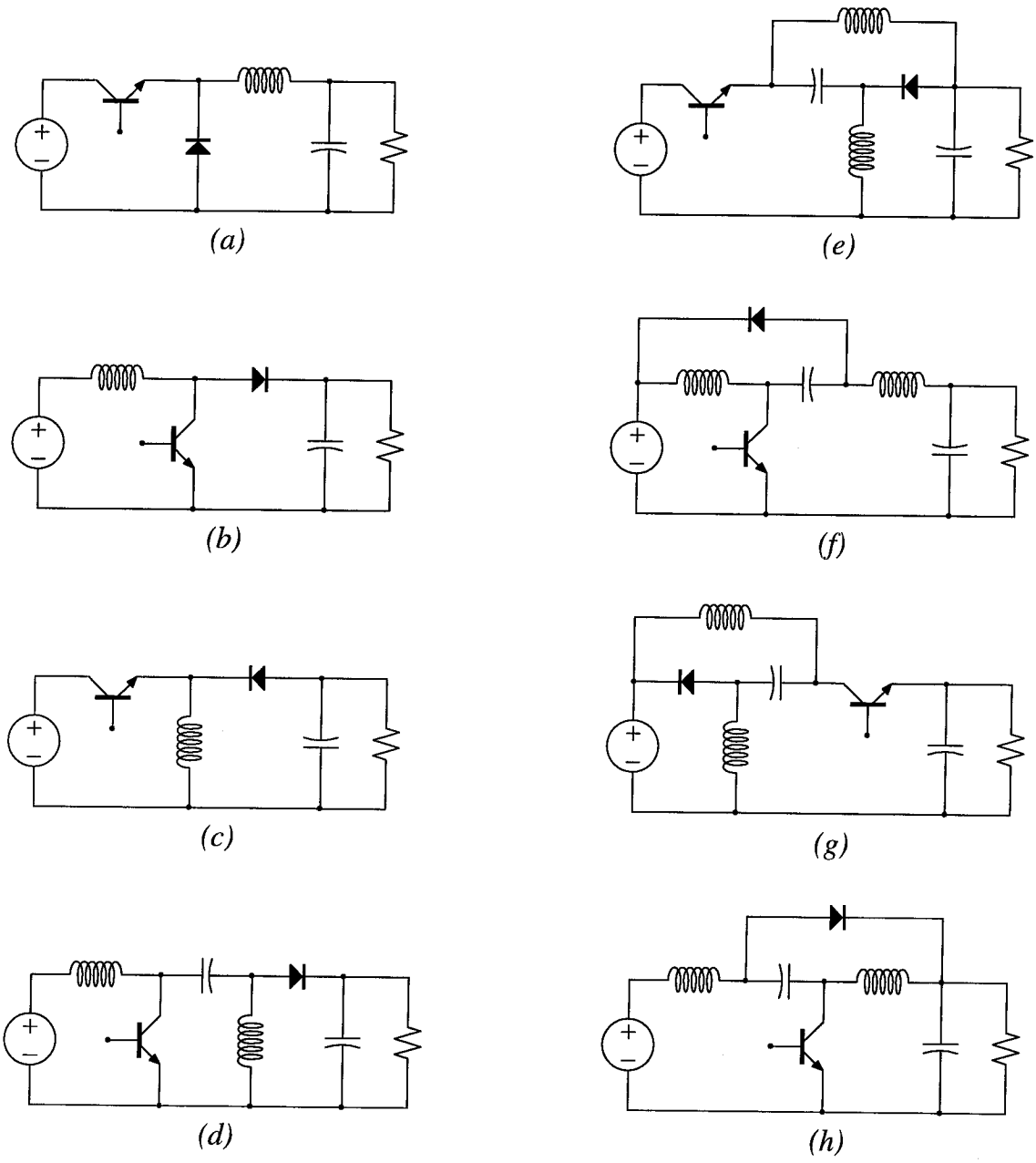


Figure 7.4: Pwm converter realizations corresponding to dc circuits (a)-(h) in figure 7.3: (a) buck, (b) boost, (c) buck-boost, (d) sepic, (e) inverting buck-boost-like, (f) inverting buck-boost-like, (g) buck-like, (h) boost-like.

7.2 Equivalent Duty Ratio

In this section, a unified method for finding the conversion ratio of dc/dc converters operating in dcm is derived, using the concept of equivalent duty ratio. The equivalent duty ratio concept was first used as a unified method of deriving the conversion ratio in quasi-resonant converters [1], and later was used in the analysis of pwm converters operating in dcm [5]. The equivalent duty ratio relates the converter conversion ratio in dcm to its conversion ccm. In the next section, these results are extended to apply to ac/dc rectifier circuits.

From figure 5.2, analysis of the switch waveforms for ideal pwm converters operating in ccm showed that the average or dc components of the transistor current and diode voltage are given by

$$\begin{aligned} I_Q &= DI_{on} \\ V_D &= DV_{off} \end{aligned} \tag{7.2.1}$$

Similarly, analysis of the dcm waveforms in figure 6.2 gives

$$\begin{aligned} I_Q &= \frac{D}{D+D_2} I_{on} \\ V_D &= \frac{D}{D+D_2} V_{off} \end{aligned} \tag{7.2.2}$$

The equivalent duty ratio is defined

$$\delta \equiv \frac{d}{d+d_2} \tag{7.2.3}$$

with its average or dc value given by

$$\Delta = \frac{D}{D+D_2} \tag{7.2.4}$$

Since the conversion ratio is derived from the dc circuit using only the average switch voltage and the average switch current, the conversion ratio in dcm is the same as the conversion ratio in ccm whenever these average quantities are equal. Comparison of the two sets of equations (7.2.1) and (7.2.2) reveals that this occurs whenever $\Delta = D$.

Hence, the conversion ratio in dcm can be derived by replacing the duty ratio D with the equivalent duty ratio Δ in the expression for the conversion ratio in ccm. That is

$$M_{\text{dcm}}(D, D_2) = M(D)\Big|_{D=\Delta} \tag{7.2.5}$$

where $M_{\text{dcm}}(D, D_2)$ denotes the conversion ratio in dcm, and $M(D)$ is the conversion ratio in ccm. This is not immediately useful, however, since the conversion ratio in dcm is a function of an unknown quantity D_2. To find an expression for D_2, take the ratio V_{off}/I_{on}, where, from the dcm waveforms in figure 6.2:

$$V_{off} = \frac{D+D_2}{D_2}V_Q \qquad I_{on} = \frac{T_s}{2L}D(D+D_2)V_Q \tag{7.2.6}$$

This gives

$$D_2 = \frac{2L}{DT_s}\frac{I_{on}}{V_{off}} \tag{7.2.7}$$

It can be shown [4] that for any pwm converter, regardless of the operating mode

$$\frac{V_{off}}{I_{on}} = \frac{R}{M} \tag{7.2.8}$$

which is an amazing result since it relates the converters internal quantities to its external quantities. Combining (7.2.7) and (7.2.8) gives the dc value of the decay interval in dcm

$$D_2 = \frac{KM_{\text{dcm}}}{D} \tag{7.2.9}$$

Substituting this result into the expression for the equivalent duty ratio (7.3.4) gives

$$\Delta = \frac{D^2}{D^2 + KM_{\text{dcm}}} \tag{7.2.10}$$

where conduction parameter K is given by the familiar definition

$$K \equiv \frac{2L_{on}}{RT_s} \tag{7.2.11}$$

The conversion ratio for any pwm converter operating in dcm can now be found as a function of the duty ratio D and conduction parameter K by solving

$$M_{\text{dcm}}(D,K) = M(\Delta) \tag{7.2.12}$$

with Δ as given by (7.2.10) and M is the conversion ratio in ccm.

Now consider the problem of the determination of the boundary between ccm and dcm for a dc/dc converter. The converter operates in dcm whenever

$$D+D_2 < 1 \tag{7.2.13}$$

and operates at the boundary between dcm and ccm when the inequality is replaced with equality in this expression. Substituting (7.2.9) into (7.2.13) gives the critical value of the conduction parameter K as a function of duty ratio D at the boundary between dcm and ccm

$$K_{\text{crit}}(D) = \frac{DD'}{M(D)} \tag{7.2.14}$$

Since the function $M(D)$ is one-to-one, the inverse function $D(M)$ exists, and the critical value of the conduction parameter can therefore be more conveniently expressed as a function of the conversion ratio as

$$K_{\text{crit}}(M) = \frac{D(M)D'(M)}{M} \tag{7.2.15}$$

Hence, the operating mode of the converter may be determined from

$$\begin{aligned} K < K_{\text{crit}} &\Rightarrow \text{dcm} \\ K = K_{\text{crit}} &\Rightarrow \text{boundary} \\ K > K_{\text{crit}} &\Rightarrow \text{ccm} \end{aligned} \tag{7.2.16}$$

The results for all eight dc circuits for pwm converters employing one transistor and one diode are tabulated in table 7.1. An important implication of this analysis is that any two converters possessing the same dc circuit exhibit not only the same conversion ratio in ccm, but the same conversion ratio in dcm as well.

dc circuit	$M(D)$	output polarity	domain of D	range of M	$D(M)$	$K_{crit}(D)$	$K_{crit}(M)$	$M_{dcm}(D,K)$
(a)	D	+	$0 \le D \le 1$	$0 \le M \le 1$	M	D'	$1-M$	$\frac{2}{1+\sqrt{1+4K/D^2}}$
(b)	$\frac{1}{1-D}$	+	$0 \le D < 1$	$1 \le M \le \infty$	$\frac{M-1}{M}$	$D(D')^2$	$\frac{M-1}{M^3}$	$\frac{1+\sqrt{1+4D^2/K}}{2}$
(c)	$\frac{D}{1-D}$	−	$0 \le D < 1$	$0 \le M < \infty$	$\frac{M}{1+M}$	$(D')^2$	$\frac{1}{(1+M)^2}$	$\frac{D}{\sqrt{K}}$
(d)	$\frac{D}{1-D}$	+	$0 \le D < 1$	$0 \le M < \infty$	$\frac{M}{1+M}$	$(D')^2$	$\frac{1}{(1+M)^2}$	$\frac{D}{\sqrt{K}}$
(e)	$\frac{D}{1-2D}$	−	$0 \le D < 0.5$	$0 \le M < \infty$	$\frac{M}{1+2M}$	$D'(1-2D)$	$\frac{1+M}{(1+2M)^2}$	$\frac{2}{-1+\sqrt{1+4K/D^2}}$
(f)	$\frac{2D-1}{1-D}$	−	$0.5 \le D < 1$	$0 \le M < \infty$	$\frac{1+M}{1+2M}$	$\frac{D(D')^2}{2D-1}$	$\frac{1+M}{M(2+M)^2}$	$\frac{-1+\sqrt{1+4D^2/K}}{2}$
(g)	$\frac{2D-1}{D}$	+	$0.5 \le D \le 1$	$0 \le M \le 1$	$\frac{1}{2-M}$	$\frac{D'D^2}{2D-1}$	$\frac{1-M}{M(2-M)^2}$	$\frac{D^2}{D^2+K}$
(h)	$\frac{1-D}{1-2D}$	+	$0 \le D < 0.5$	$1 \le M < \infty$	$\frac{M-1}{2M-1}$	$D(1-2D)$	$\frac{M-1}{(2M-1)^2}$	$1+\frac{D^2}{K}$

Table 7.1: Summary of the dc conversion properties of all eight dc circuits for pwm converters employing a single transistor and a single diode.

7.3 Pwm Converters in Ac/Dc Rectifier Circuits

When a pwm converter is used as a controllable interface between an ac power source and a dc load, the voltage and current "seen" by the converter at its input and output ports can vary over a wide range. These variations complicate the problem of the determination the converter operating mode as compared to the dc/dc case. However, a condition, similar to the one derived in the previous section for a dc/dc converter, can be derived for an ac/dc rectifier, once the voltage and current variations at the input and output ports are determined.

The general structure of a pwm converter based rectifier is shown below in figure 7.5. The converter output filter is considered separate from the converter, and it is assumed that energy storage for the purpose of load balancing occurs in the output filter only, with no significant low frequency energy storage within the converter itself. Under these conditions, the energy storage element or network is said to be "adjacent" to the load. The case of energy storage internal to the converter is not considered here, but is not of practical interest in two-switch converter-based rectifier circuits. In converters with three or more switches, energy storage within the rectifier can be advantageous [28,29]; the additional degree of freedom opening the possibility of simultaneously obtaining high input power factor, and fast regulation of the dc output voltage. However, many rectifier circuits of this type can be analyzed as the cascade connection of two two-switch converters, one which provides input current shaping as described here, and the other, acting as a regulator, provides fast regulation of the dc output voltage.

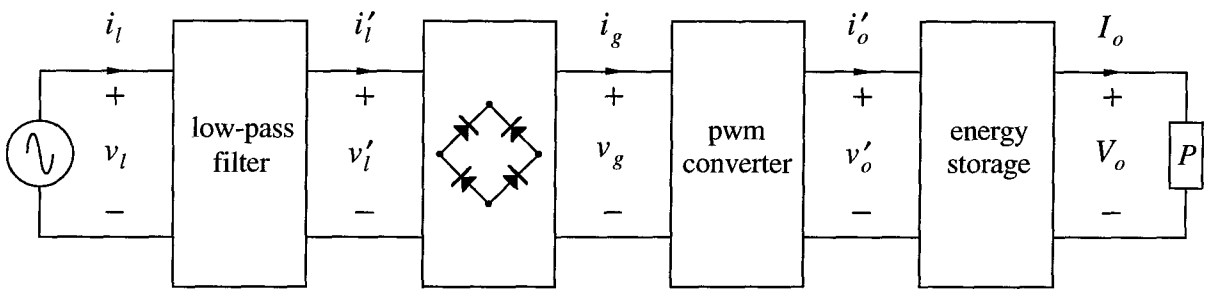


Figure 7.5: General structure of a complete ac/dc rectifier circuit, employing a two-switch pwm converter, shown with a constant power load.

The conduction mode of a pwm converter is determined by the average voltage and current appearing at its input and output ports. Since, in any switching period, the conduction mode is determined by whether or not the diode current reaches zero in that same period, we conclude that the conduction mode is a property of a switching period. Hence, the *average* voltage and current in this case refers to the switching frequency average, not the line frequency average. To simplify the expressions in the presentation that follows, we drop the switching frequency average notation $\langle\cdot\rangle$, and it is understood that we are talking about average quantities, the average taken over a switching period.

In the general rectifier configuration of figure 7.5, the low-pass filter is designed to attenuate switching frequency ripple current generated by the pwm converter, and to pass the line frequency component undisturbed. Therefore, the voltage at the input to the bridge rectifier v_l' may, for the present purpose, be considered the same as the line voltage v_l. Hence, voltage v_g, at the input of the pwm converter, is a rectified sinusoid with peak amplitude equal to the peak line voltage

$$v_g(\theta) = V_p|\sin\theta| \tag{7.3.1}$$

The voltage at the output of the pwm converter, v_o', depends on the type of energy storage utilized in the circuit. An energy storage element or network is usually one of two types; either the constant voltage (or low impedance) type, or the constant current (or high impedance) type. A large energy storage capacitor, for example, presents a stiff impedance to the converter output, and is therefore of the constant voltage type. A large energy storage inductor, being the dual of the large energy storage capacitor, provides nearly constant current at the converter output, and is therefore of the constant current type.

Consider the large energy storage capacitor connected across the converter output. If we assume that the rectifier circuit operates with unity input power factor and absorbs little low frequency energy, then the rectifier circuit approximates the ideal rectifier with a single load balancing element. In chapter 4, we showed that the current in the large energy storage capacitor is approximately given by

$$i_C(\theta) \cong -\frac{P}{V_C}\cos 2\theta \tag{7.3.2}$$

Since the capacitor voltage is nearly constant, the actual dc output current I_o, drawn by the constant power load, is nearly constant, and is approximately

$$I_o \cong \frac{P}{V_o} \tag{7.3.3}$$

KCL at the output node gives the current flowing from the converter output, i_o', given by

$$i_o' \cong 2I_o \sin^2\theta \tag{7.3.4}$$

The *apparent load* is defined in general as the ratio of the output voltage to the output current, measured at the converter output terminals

$$r'(\theta) \equiv \frac{v_o'(\theta)}{i_o'(\theta)} \tag{7.3.5}$$

For the present example of the large energy storage capacitor, the apparent load is given by

$$r'(\theta) = \frac{R}{2\sin^2\theta} \tag{7.3.6}$$

where R is the equivalent load resistance; i.e., the ratio of the dc output voltage to the dc output current

$$R \equiv \frac{V_o}{I_o} \tag{7.3.7}$$

The *apparent conversion ratio* is defined in general as the ratio of the output voltage to the input voltage, measured at the converter terminals

$$m'(\theta) \equiv \frac{v_o'(\theta)}{v_g(\theta)} \tag{7.3.8}$$

For the present example, the apparent conversion ratio is given by

$$m'(\theta) = \frac{M_p}{|\sin\theta|} \tag{7.3.9}$$

where M_p is the peak conversion ratio, $M_p \equiv V_o/V_p$. The *apparent conduction parameter* is defined in general as a function of the apparent load

$$k'(\theta) \equiv \frac{2L_{on}}{r'(\theta)T_s} \tag{7.3.10}$$

For the present example, the apparent conduction parameter is given by

$$k'(\theta) = 2K\sin^2\theta \tag{7.3.11}$$

where conduction parameter K is defined as usual

$$K \equiv \frac{2L_{on}}{RT_s} \tag{7.3.12}$$

The *apparent critical conduction parameter* is defined as a function of the apparent conversion ratio

$$k'_{\text{crit}}\left(m'(\theta)\right) = K_{\text{crit}}(M)\Big|_{M=m'(\theta)} \tag{7.3.13}$$

The operating mode for pwm converters in ac/dc rectifier circuits is determined in the same way as was done for dc/dc circuits, except the dc quantities are replaced by their apparent counterparts. Hence, the conditions for determining the operating mode in an ac/dc rectifier circuit are:

$$\begin{aligned} k'(\theta) < k'_{\text{crit}}\left(m'(\theta)\right) &\Rightarrow \text{dcm} \\ k'(\theta) = k'_{\text{crit}}\left(m'(\theta)\right) &\Rightarrow \text{boundary} \\ k'(\theta) > k'_{\text{crit}}\left(m'(\theta)\right) &\Rightarrow \text{ccm} \end{aligned} \tag{7.3.14}$$

The apparent circuit quantities, under the assumption of unity input power factor, are summarized in table 7.2, for the two common energy storage types. For rectifier circuits that operate with input power factor other than unity, the apparent load, apparent conversion ratio, and apparent conduction parameter can be computed from the definitions, once the average voltage and current at the converter input and output ports are determined.

energy storage	$v_o'(\theta)$	$i_o'(\theta)$	$r'(\theta)$	$m'(\theta)$	$k'(\theta)$
constant voltage	V_o	$2I_o \sin^2\theta$	$\frac{R}{2\sin^2\theta}$	$\frac{M_p}{\lvert\sin\theta\rvert}$	$2K\sin^2\theta$
constant current	$2V_o \sin^2\theta$	I_o	$2R\sin^2\theta$	$2M_p\lvert\sin\theta\rvert$	$\frac{K}{2\sin^2\theta}$

Table 7.2: Large-signal apparent quantities for pwm converters in ac/dc rectifier circuits, operating with unity input power factor, for the two common energy storage types.

Example: Boost Rectifier Operating Mode Boundary

Consider the standard boost rectifier circuit with a large energy storage output capacitor and a constant power load. Assume that the converter is controlled to achieve unity input power factor. Since the energy storage is of the constant voltage type, the apparent conversion ratio is, from table 7.2:

$$m'(\theta) = \frac{M_p}{\lvert\sin\theta\rvert} \tag{7.3.15}$$

Since the boost conversion ratio is restricted to the range $1 \le M < \infty$, achieving the required apparent conversion ratio is indeed possible, provided $M_p \ge 1$.

Suppose it is desired to operate exclusively in ccm. The inequality to satisfy is

$$k'(\theta) > k'_{\text{crit}}\left(m'(\theta)\right) \quad \Rightarrow \quad \text{ccm} \tag{7.3.16}$$

where the apparent conduction parameter $k'(\theta)$ can be read from table 7.2, and the apparent critical conduction parameter is determined by substituting the apparent conversion ratio $m'(\theta)$ into the expression for the critical conduction parameter, $K_{\text{crit}}(M)$, found in table 7.1. Doing so gives

$$K > \frac{M_p - \lvert\sin\theta\rvert}{2M_p^3} \tag{7.3.17}$$

The quantity on the right side of the inequality is largest when $|\sin\theta| = 0$, i.e., at the zero crossings of the line voltage, when the input voltage is minimum. Therefore, operation in ccm over the entire line period requires

$$K > \frac{1}{2M_p^2} \tag{7.3.18}$$

Now consider the opposite case, where it is desired to operate exclusively in dcm. Again, assume that the converter is controlled to obtain unity input power factor. For this case, the inequality to satisfy is

$$k'(\theta) < k'_{\text{crit}}\left(m'(\theta)\right) \quad \Rightarrow \quad \text{dcm} \tag{7.3.19}$$

which gives

$$K < \frac{M_p - |\sin\theta|}{2M_p^3} \tag{7.3.20}$$

The quantity on the right side of the inequality is minimum when $|\sin\theta| = 1$; i.e., at the peaks of the line voltage. Operation in dcm over the entire line period requires

$$K < \frac{M_p - 1}{2M_p^3} \tag{7.3.21}$$

It is important to reemphasize that the assumption of unity input power factor was made in this derivation, and the results are different when the power factor is other than unity. We return to this example in the next chapter, where the dcm boost rectifier is analyzed under various methods of control.

Chapter 8

The Dcm Boost Rectifier

In this chapter, the tools developed in the preceding chapters are applied to the analysis and design of the dcm boost rectifier circuit. The boost converter is in general an excellent choice for rectifier applications for two main reasons: First, it is capable of voltage step-up, and can therefore serve as the interface between the rectified line voltage and a constant voltage energy storage "network," namely an inexpensive bulk energy storage capacitor. Second, the boost converter is what is known as a "partial" power processing converter, which processes only part of the input power, making it extremely efficient as compared to total power processing converters, such as the buck-boost converter.

The boost rectifier operating in ccm is commonly used in rectifier applications at moderate power levels, but dcm operation offers several advantages which make it attractive in the low-to-medium power range. One advantage is the alleviation of switching loss in the power transistor resulting from the reverse-recovery of the rectifier diode. Another is the automatic current shaping property exhibited by the boost rectifier operating in dcm. Also, for higher power applications, it is possible to operate several smaller dcm boost power stages in parallel, phase-shifted with respect to one another, to obtain a high power rectifier circuit. The phase-shift is used as an input current ripple cancellation technique, the ripple of one converter acting to cancel, to some degree, the ripple of another.

In this chapter, three different control schemes for the dcm boost rectifier are examined, each offering some compromise between performance and complexity. First, the standard constant duty ratio scheme is analyzed. This scheme works well, but does induce some input current distortion, especially for low values of the ac/dc conversion

ratio. Acceptable performance is obtained at the expense of a high ac/dc conversion ratio. This high conversion ratio translates not only to high voltage stress in the rectifier circuit itself, but to high voltage stress in downstream converters and regulators as well. Hence, a tradeoff exists between the level of input current distortion and the high output voltage.

Next, a unity power factor control scheme [11] is analyzed which corrects the input current distortion problem, giving (ideally) unity input power factor regardless of the ac/dc conversion ratio. The main drawback of this approach is that it requires two analog multipliers in its circuit implementation, making it too complex for use in most low-cost systems, barring the production of a low-cost dedicated integrated circuit with the necessary analog multipliers built-in.

Finally, a third approach using optimal voltage feedback is analyzed, which provides near unity input power factor, without the added expense and complexity of the analog multiplier circuits. An additional benefit of the optimal voltage feedback approach is that it inherently provides excellent transient response at the rectifier output. This is not true of either of the previously mentioned approaches, where the response of the output voltage to changing line and load conditions needs to be considered separately. Experimental results for an optimal voltage feedback, universal input voltage range (85-265Vrms), 200W, dcm boost rectifier prototype are provided at the end of this chapter.

8.1 Dcm Circuit Model

The basic boost rectifier circuit is shown in figure 8.1(a). Just as in the buck-boost rectifier analysis in section 6.4, the low-pass filter is designed to attenuate current ripple at the switching frequency and its harmonics, and to have little effect at the line frequency. Thus, for low frequency considerations, the effect of the low-pass filter may be ignored, and the voltage at the converter input can be approximated by a rectified sinusoid with peak amplitude equal to the peak line voltage. The continuous nonlinear circuit model in figure 8.1(b) is formed by inserting the nonlinear dcm switch model from chapter 6, figure 6.4, and replacing the inductor with a short circuit.

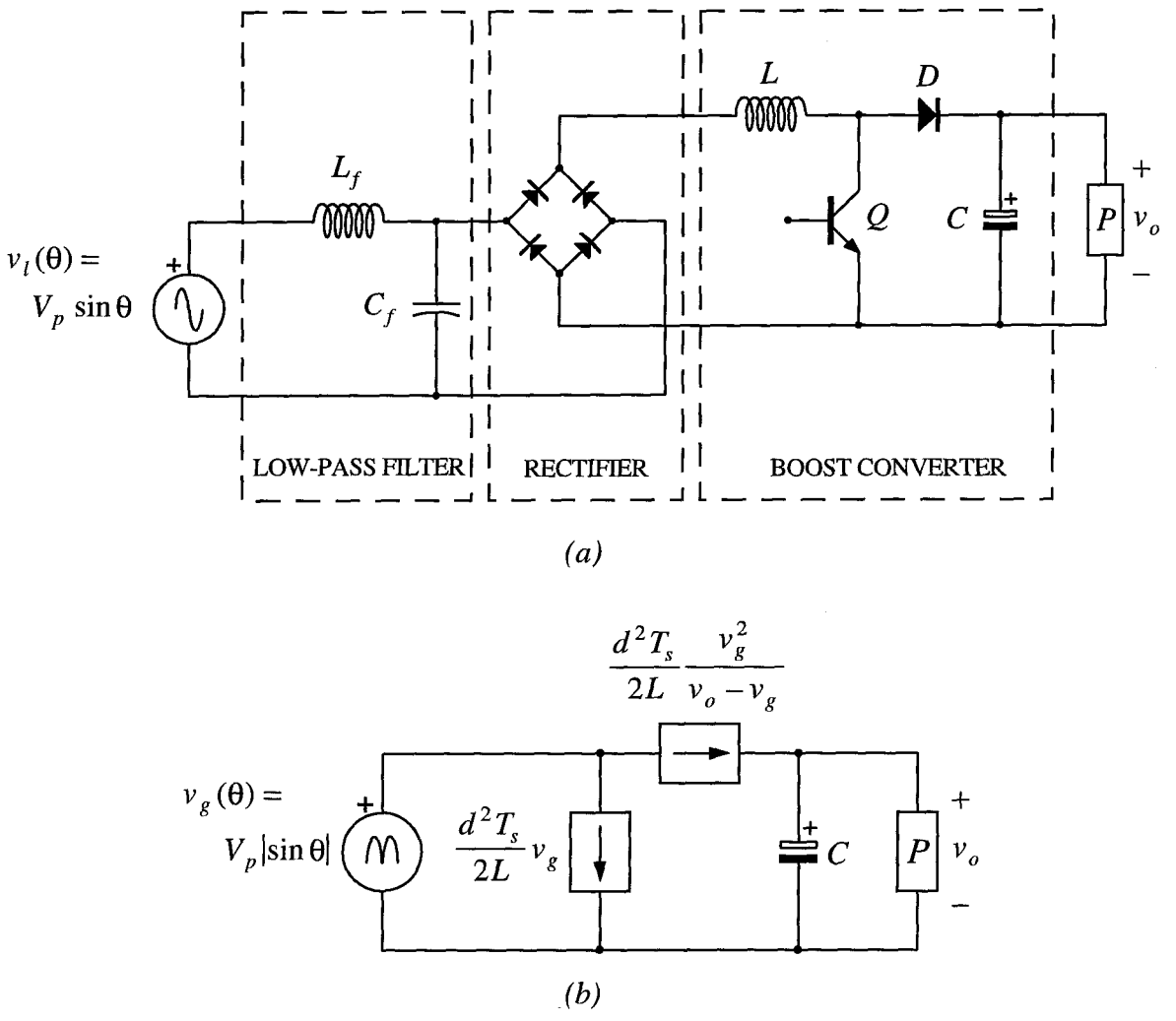


Figure 8.1: (a) The boost rectifier circuit, and (b) continuous, nonlinear dcm boost rectifier circuit model.

From the model, the converter input current, $i_g(\theta)$, is given by

$$i_g(\theta) = \frac{d^2(\theta) T_s}{2L} \frac{v_o(\theta) V_p |\sin\theta|}{v_o(\theta) - V_p |\sin\theta|} \tag{8.1.1}$$

where the dependence of the duty ratio, input voltage, and output voltage on angle θ is shown explicitly. In each of the control schemes in the following sections, this dependence is different. We begin with analysis of the constant duty ratio dcm boost rectifier in the next section.

8.2 Constant Duty Ratio Dcm Boost Rectifier

The boost rectifier, when operated in dcm with constant duty ratio, exhibits less than unity input power factor, owing to distortion of the input current waveform. However, this circuit can be designed so that the power factor and input current harmonics are maintained to levels which are acceptable for many applications. In this section, the performance characteristics of this rectifier circuit are analyzed and assessed with respect to the ideal rectifier of chapter 2.

8.2.1 Operating Point

The fundamental assumption in the analysis of this circuit is that the duty ratio is constant with respect to the line period. In this scheme, duty ratio variations *do* occur in response to input voltage and output load variations, but are assumed to occur slowly with respect to a line period. In addition, it is assumed that the energy storage capacitor is large enough so that the output voltage may be considered constant. With these assumptions, the converter input current in steady-state can be written

$$i_g(\theta) = \frac{D^2 T_s}{2L} \frac{V_p |\sin\theta|}{1 - \frac{1}{M_p}|\sin\theta|} \tag{8.2.1}$$

where the duty ratio D and peak conversion ratio M_p are assumed to be constant. For the constant power load, the equivalent large-signal load resistance can be expressed

$$R = \frac{V_o^2}{P} \tag{8.2.2}$$

The operating point is then found by equating the average input power over half of a line period with the output power

$$\frac{D^2 T_s}{2L} V_p^2 \bar{f}(M_p) = \frac{V_o^2}{R} \tag{8.2.3}$$

where the "bar" notation is used to denote the average over half the line period:

$$\bar{h} = \frac{1}{\pi}\int_0^{\pi} h(\theta)\, d\theta \tag{8.2.4}$$

and the function $f(M_p,\theta)$ is given by

$$f(M_p,\theta) = \frac{\sin^2\theta}{1-\frac{1}{M_p}|\sin\theta|} \tag{8.2.5}$$

The average of this function over half the line period can be written in closed form [14]:

$$\bar{f}(M_p) = \frac{M_p^3}{\sqrt{M_p^2-1}}\left[1+\frac{2}{\pi}\sin^{-1} M_p^{-1}\right] - M_p^2 - \frac{2}{\pi}M_p \tag{8.2.6}$$

Then, solving equation (8.2.3) for the steady-state duty ratio gives

$$D = M_p\sqrt{\frac{K}{\bar{f}(M_p)}} \tag{8.2.7}$$

where K is the familiar conduction parameter.

8.2.2 Power Factor and Harmonics

Substituting the steady-state value of the duty ratio (8.2.7) into equation (8.2.1) gives the switching frequency averaged converter input current as a function of the normalized time variable θ. This can then be written with respect to the ideal current as

$$i_g(\theta) = I_{ideal}\frac{1}{\sqrt{2}\bar{f}(M_p)}\frac{|\sin\theta|}{1-\frac{1}{M_p}|\sin\theta|} \tag{8.2.8}$$

The actual line current is the alternating periodic extension of this result. As shown in appendix A, the alternating periodic extension contains only odd harmonics. Also, because expression (8.2.8) is symmetric about $\pi/2$ on $[0,\pi]$, the alternating periodic extension is an odd function, and therefore contains only sine terms in its Fourier series expansion. Hence, the normalized current harmonics are obtained from

$$i_n \equiv \frac{I_n}{I_{ideal}} = \begin{cases} \dfrac{1}{\bar{f}(M_p)} \dfrac{1}{\pi} \displaystyle\int_0^{\pi} \dfrac{\sin\theta \sin n\theta}{1 - \dfrac{1}{M_p}\sin\theta} d\theta \text{ , } n \text{ odd} \\ 0 \text{ , } n \text{ even} \end{cases} \tag{8.2.9}$$

The fundamental component is easily seen to be

$$I_1 = I_{ideal} \tag{8.2.10}$$

and the rms value of the line current is

$$I_{rms} = I_{ideal} \frac{\sqrt{\bar{g}(M_p)}}{\sqrt{2}\bar{f}(M_p)} \tag{8.2.11}$$

where the function $g(M_p, \theta)$ is given by

$$g(M_p, \theta) = \frac{\sin^2\theta}{\left[1 - \dfrac{1}{M_p}|\sin\theta|\right]^2} \tag{8.2.12}$$

The average of this function over half the line period can also be written in closed form [14]:

$$\bar{g}(M_p) = M_p^2 + \frac{2}{\pi}\frac{M_p^3}{M_p^2 - 1} - \frac{M_p^5 - 2M_p^3}{(M_p^2 - 1)^{3/2}}\left[1 + \frac{2}{\pi}\sin^{-1} M_p^{-1}\right] \tag{8.2.13}$$

From chapter 2, the power factor, distortion factor, and displacement factor can be determined from

$$PF = \frac{I_{ideal}}{I_{rms}} \text{ ; } DF = \frac{I_1}{I_{rms}} \text{ ; } \cos\phi_1 = \frac{I_{ideal}}{I_1} \tag{8.2.14}$$

From equation (8.2.10), the displacement factor is obviously unity, making the power factor and distortion factor equal. From equation (8.2.11), the power factor may be written

$$PF = \frac{\sqrt{2}\bar{f}(M_p)}{\sqrt{\bar{g}(M_p)}} \tag{8.2.15}$$

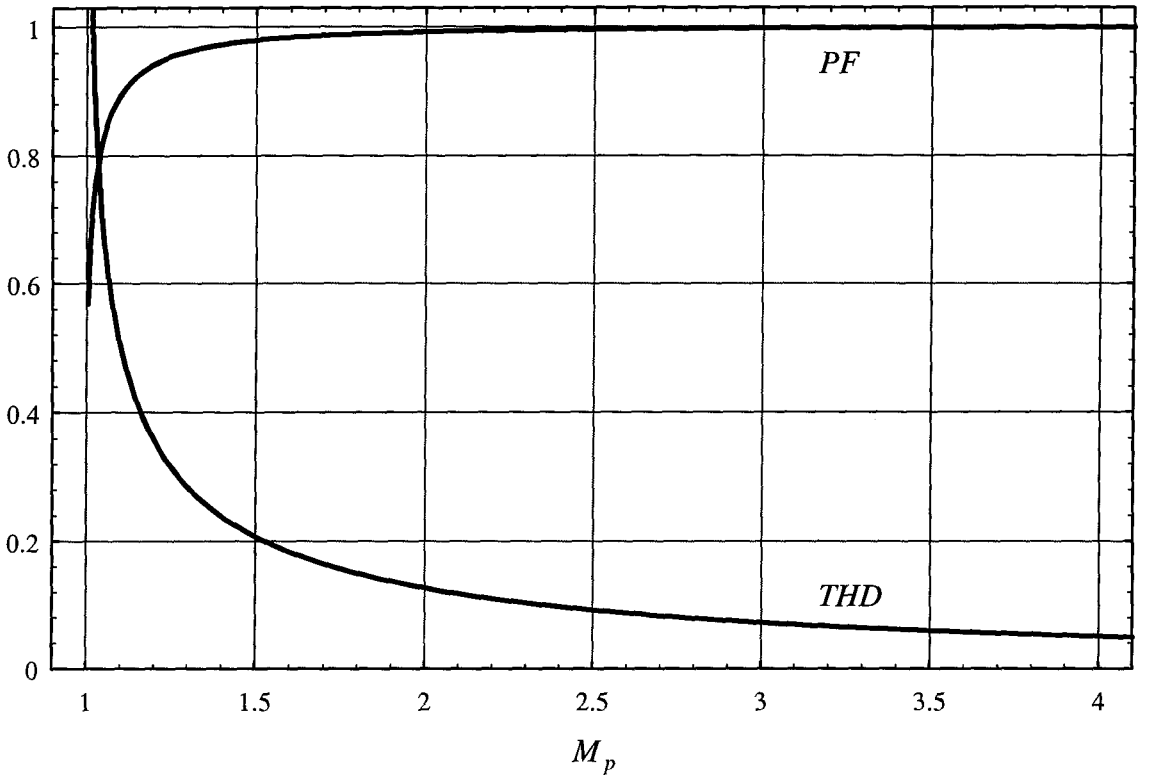


Figure 8.2: Power factor and total harmonic distortion as a function of the peak conversion ratio M_p for the dcm boost rectifier operated with constant duty ratio.

This expression is plotted above in figure 8.2 as a function of the peak conversion ratio M_p. Because the power factor and distortion factor are equal, the relationship between the power factor and the total harmonic distortion is one-to-one, and the total harmonic distortion may also be plotted as a function of M_p, as shown in figure 8.2.

Normalized input current harmonics 3-15 are determined by numerically evaluating equation (8.2.9), and their magnitudes are plotted in figure 8.3 as a function of peak conversion ratio . It is observed that harmonics of order $4n+1$ each vanish for some particular value of the conversion ratio M_p. The third harmonic is most prevalent being at least 20dB larger than all other harmonics over most of the range of conversion ratio shown. Harmonics of order 15 or higher become very small for conversion ratios exceeding 1.2, and are not included in the figure to preserve its clarity.

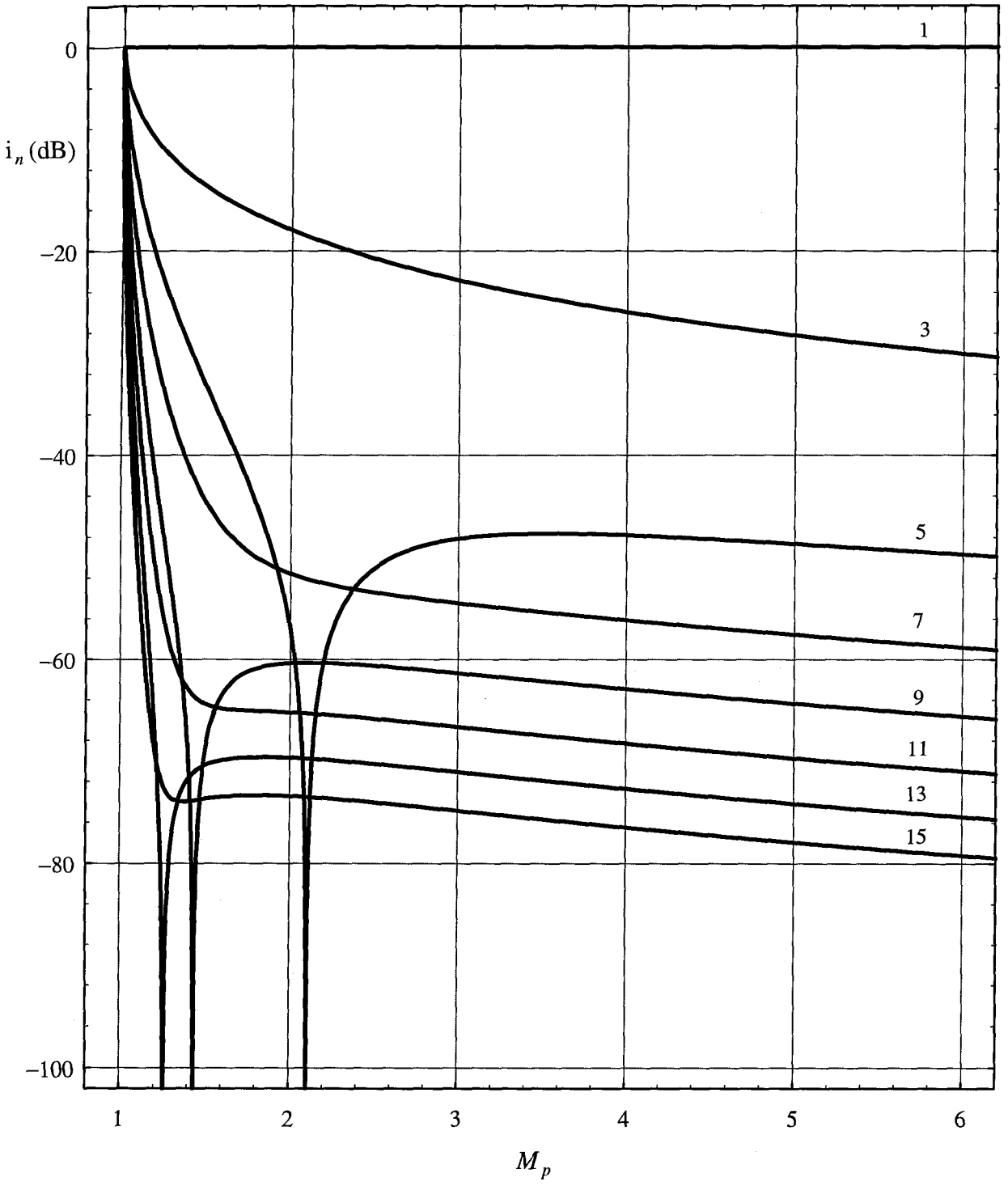


Figure 8.3: Normalized odd input current harmonics 1-15 vs. peak conversion ratio M_p for the dcm boost rectifier operated with constant duty ratio.

8.2.3 Conduction Mode Boundary

For the dcm boost rectifier operated with constant duty ratio, the critical boundary between dcm and ccm operation is found using the results of chapter 7. Since the dcm boost rectifier under this control does not operate with unity input power factor, the results in table 7.2 do not apply, and the critical boundary must instead be determined using the more general formulas for the apparent circuit quantities.

Since the output voltage is assumed to be constant, the apparent conversion ratio is unchanged from the unity input power factor case, and is given by

$$m'(\theta) = \frac{M_p}{|\sin\theta|} \tag{8.2.16}$$

The apparent load is, however, different from that in the unity power factor case. Using the notation from chapter 7, the nonlinear circuit model in figure 8.1(b) gives the current flowing from the converter output

$$i_o' = \frac{D^2 T_s}{2L} \frac{v_g^2}{V_o - v_g} \tag{8.2.17}$$

Substituting the steady-state duty ratio, equation (8.2.7), the apparent load $r'(\theta)$ can then be written

$$r'(\theta) = R \frac{\bar{f}(M_p)}{\sin^2\theta} \left[1 - \frac{1}{M_p} |\sin\theta| \right] \tag{8.2.18}$$

The apparent conduction parameter is then

$$k'(\theta) = K \frac{\sin^2\theta}{\bar{f}(M_p)\left[M_p - |\sin\theta| \right]} \tag{8.2.19}$$

From chapter 7, the condition for dcm operation is

$$k'(\theta) < k'_{\text{crit}}\left(m'(\theta)\right) \quad \Rightarrow \quad \text{dcm} \tag{8.2.20}$$

The apparent critical conduction parameter is found by substituting equation (8.2.16) into the expression for the critical conduction parameter for the boost converter in table 7.1. This gives

$$k'_{\text{crit}}\left(m'(\theta)\right) = \sin^2\theta \frac{M_p - |\sin\theta|}{M_p^3} \tag{8.2.21}$$

Hence, the rectifier circuit operates in dcm whenever

$$K < \bar{f}(M_p)\frac{(M_p - |\sin\theta|)^2}{M_p^4} \tag{8.2.22}$$

The quantity on the right-hand side of the inequality is smallest when $\sin\theta = \pm 1$; i.e., at the peaks of the rectified line cycle, when the voltage at the converter input is largest. Thus, to ensure dcm operation over the entire line period, the converter should be designed so that conduction parameter K satisfies

$$K < \bar{f}(M_p)\frac{(M_p - 1)^2}{M_p^4} \tag{8.2.23}$$

Recall, from section 7.3, the similar expression derived for the unity power factor dcm boost rectifier

$$K < \frac{M_p - 1}{2M_p^3} \tag{8.2.24}$$

We can define the critical conduction parameter for dcm operation in a rectifier circuit, $\tilde{K}_{\text{crit,dcm}}$, as the value of the conduction parameter which ensures dcm operation over the entire line period. Thus, for the constant duty ratio dcm boost rectifier, we get

$$\tilde{K}_{\text{crit,dcm}} = \bar{f}(M_p)\frac{(M_p - 1)^2}{M_p^4} \tag{8.2.25}$$

and for the unity power factor dcm boost rectifier

$$\tilde{K}_{\text{crit,dcm}} = \frac{M_p - 1}{2M_p^3} \tag{8.2.26}$$

These expressions are plotted for comparison in figure 8.4. The critical value of the conduction parameter in the unity power factor case is always larger than that in the constant duty ratio case. From a glance at these plots, it may appear that the difference is insignificant. However, for low values of the peak conversion ratio M_p, the difference can be quite significant. For example, suppose it is desired to derive a 400Vdc output from an input voltage range of 85-265Vrms. When the input voltage is maximum, the peak conversion ratio M_p attains the minimum value of 1.07. The magnified plot in figure 8.5 shows that when $M_p = 1.07$, the critical value of the conduction parameter is about twice as large in the unity power factor case. Thus, the inductor in the unity power factor rectifier circuit can be twice as large, resulting in lower peak inductor current, lower current stress in the devices, and increased efficiency as compared to a similar circuit operated with constant duty ratio.

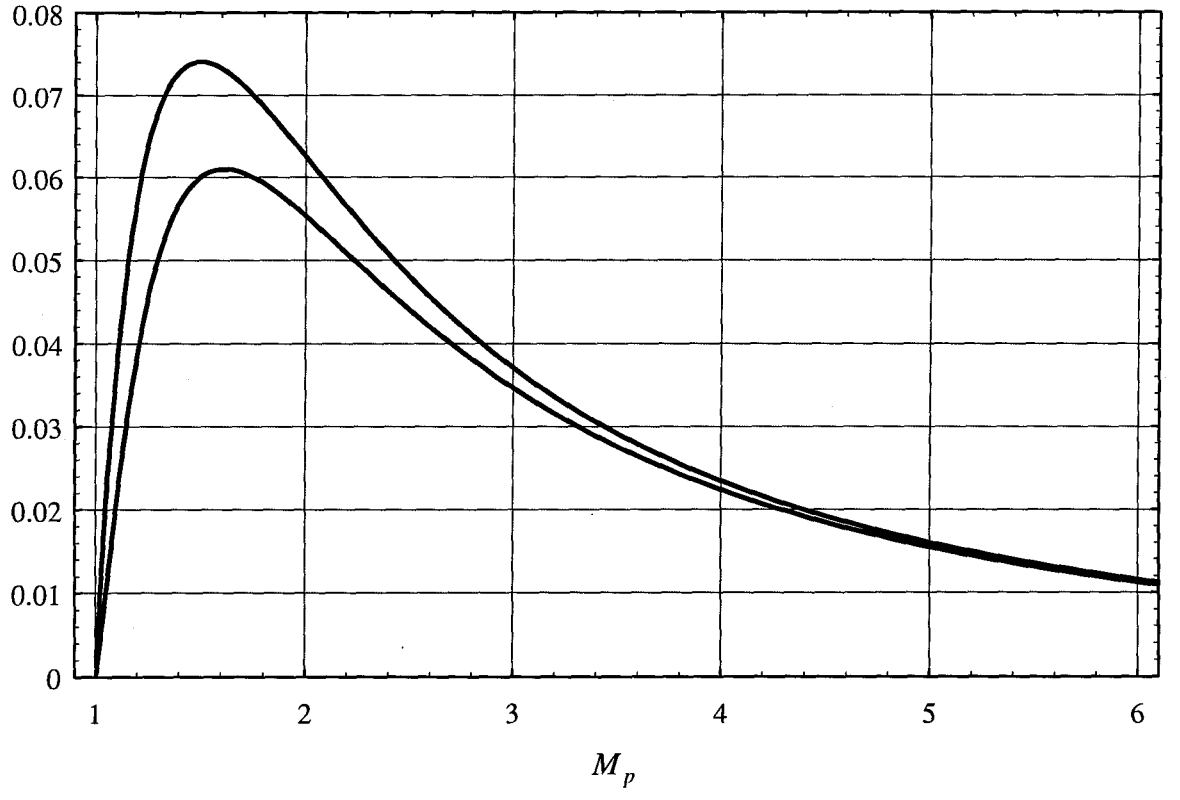


Figure 8.4: Critical conduction parameter $\tilde{K}_{\text{crit,dcm}}$ as a function of conversion ratio M_p for the unity power factor dcm boost rectifier (upper curve), and constant duty ratio dcm boost rectifier (lower curve).

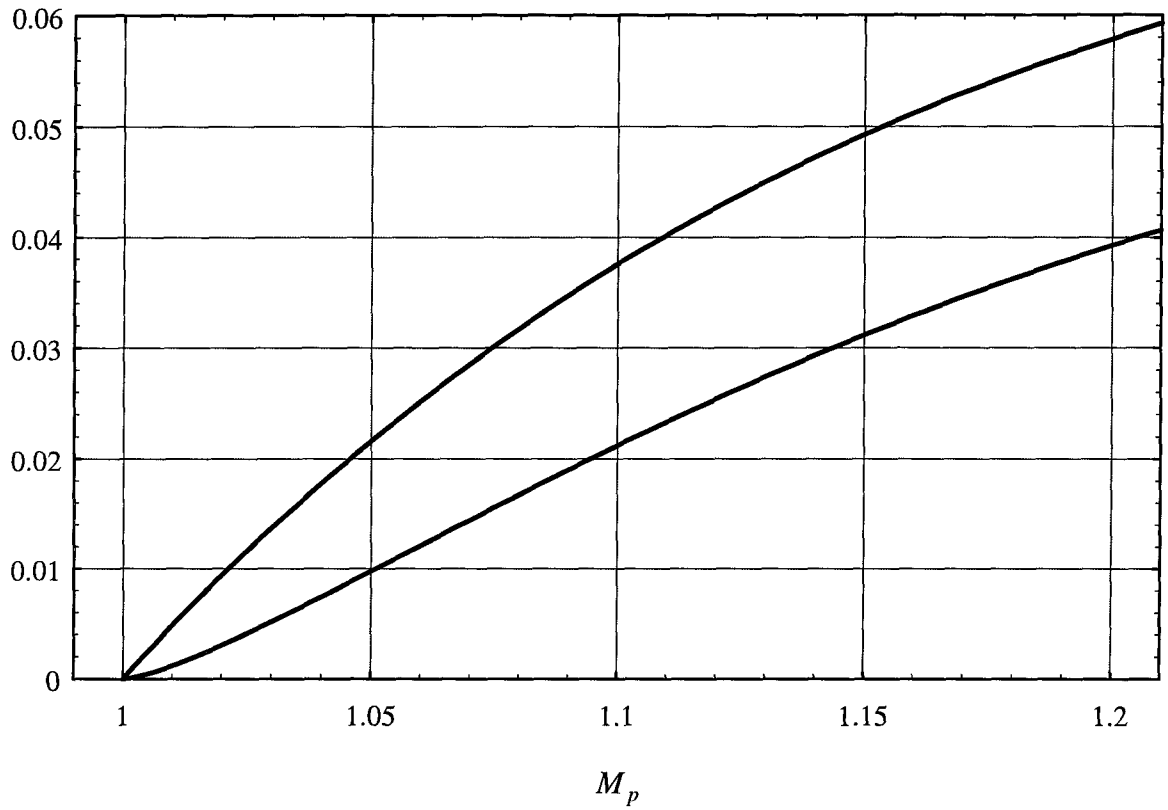


Figure 8.5: Magnified plot of critical conduction parameter $\tilde{K}_{\text{crit,dcm}}$ as a function of conversion ratio M_p for the unity power factor dcm boost rectifier (upper curve), and constant duty ratio dcm boost rectifier (lower curve).

8.3 Unity Power Factor Dcm Boost Rectifier

As demonstrated in the previous section, the benefits of operating the dcm boost rectifier with unity input power factor are realized not only by the utility, but by the rectifier circuit itself, with reduced component stress and increased efficiency. Control for unity power factor operation could be implemented in the usual manner, using a current control loop which causes the input current to track the input voltage, and a voltage control loop to regulate the output voltage. However, the current loop is neither desirable nor necessary, and it is shown in this section how unity power factor operation can be implemented using a combination of output voltage feedback and input voltage feedforward, without a current loop.

Again assuming that the output voltage is approximately constant, from the continuous nonlinear circuit model in figure 8.1(b), the switching frequency averaged current flowing into the converter input can be written

$$i_g(\theta) = \frac{d^2(\theta)T_s}{2L} \frac{V_p|\sin\theta|}{1-\frac{V_p|\sin\theta|}{V_o}} \tag{8.3.1}$$

For unity input power factor, it is necessary that the input current be proportional to the input voltage. This will be the case if

$$\frac{d^2(\theta)T_s}{2L} \frac{V_p}{1-\frac{V_p|\sin\theta|}{V_o}} = \sqrt{2}I_{ideal} \tag{8.3.2}$$

where $I_{ideal} = P/V_{ideal}$. Solving for the duty ratio, we find the necessary control

$$d(\theta) = \sqrt{2K}M_p\sqrt{1-\frac{1}{M_p}|\sin\theta|} \tag{8.3.3}$$

The duty ratio is maximum when $|\sin\theta| = 0$; i.e., at the "cusps" in the rectified input voltage waveform. The maximum duty ratio is therefore

$$D_{max} = \sqrt{2K}M_p \tag{8.3.4}$$

and the duty ratio can be written

$$d(\theta) = \frac{D_{\max}}{\sqrt{V_o}}\sqrt{V_o - V_p|\sin\theta|} \tag{8.3.5}$$

A simple control system for generating this control law is shown in figure 8.6. Since the (scaled) output voltage is nearly constant and is equal to the reference voltage in steady-state, the reference is used in the current correction circuit to represent the output voltage. If desired, the actual (scaled) output voltage signal could be used in the current correction circuit instead of the reference voltage, but doing so complicates the small-signal analysis somewhat [12].

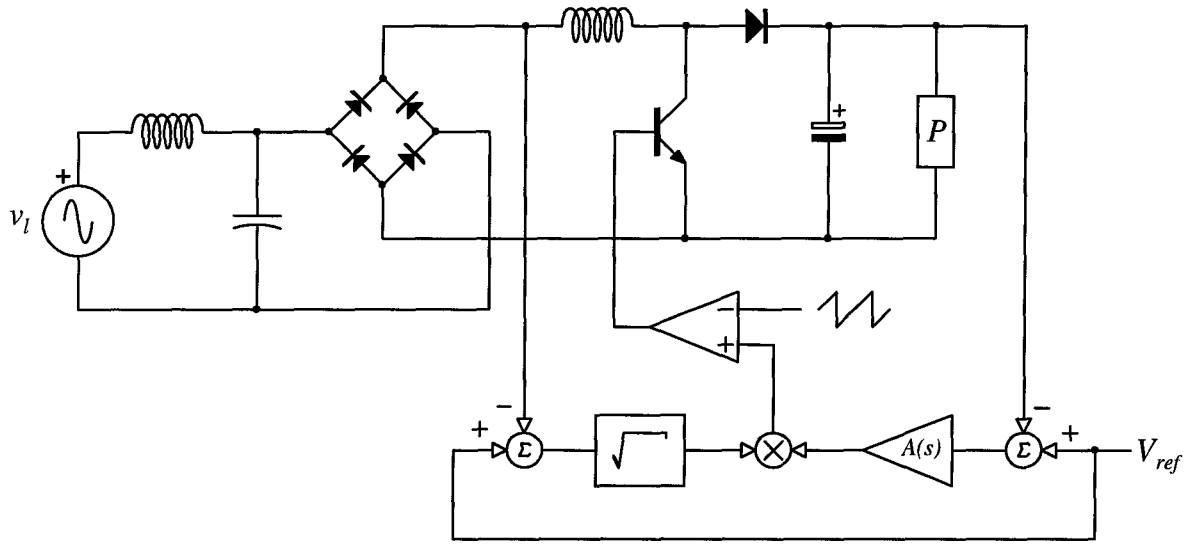


Figure 8.6: Unity power factor dcm boost rectifier. In this implementation, the reference voltage is used to represent the output voltage in the current correction circuit.

The voltage feedback amplifier should be designed to provide proportional-plus-integral feedback compensation. The integral component yields zero error in the steady-state value of the output voltage, and also to the proper correction in the input current correction circuit. The proportional component is added to provide adequate phase margin at crossover. In order to maintain the integrity of the input current waveform, the crossover frequency should be chosen well below twice the line frequency. If this requirement is violated, the control loop responds to ripple in the output voltage at twice the line frequency, which then acts to distort the input current. Thus, a tradeoff exists between the response of the output voltage control loop and the integrity of the input current waveform.

The main drawback of this approach is the need for two nonlinear operations in the feedback circuit, namely the square-root and the multiplication. The square-root is easily implemented with a standard analog multiplier, as is the multiplication. However, the cost and complexity of these additional circuits may be prohibitive for most low-cost designs. This problem could be solved with the manufacture of a

dedicated integrated circuit with the necessary control functions built-in, but at present, none are available.

8.4 Optimal Voltage Feedback Dcm Boost Rectifier

In this section, an alternative approach called optimal voltage feedback is analyzed which is, in some sense, a compromise between the previous two approaches. Optimal voltage feedback provides improved power factor over the constant duty ratio boost rectifier, without the added complexity and expense of the analog multiplier circuits required by the unity power factor boost rectifier. An additional benefit of the optimal voltage feedback approach is that it inherently provides excellent output voltage transient response as compared with the constant duty ratio and unity power factor approaches. The implementation requires the addition of a linear optimal feedback filter, which can be constructed using standard op-amps.

8.4.1 Optimal Duty Ratio Modulation

It is commonly understood that there exists a tradeoff between fast output voltage regulation and a high quality input current waveform in two-switch rectifier circuits with a single control. In these circuits, output voltage ripple at twice the line frequency, when fed back through the feedback amplifier, normally influences the duty ratio in a way that induces distortion of the input current waveform. The idea behind optimal voltage feedback is to adjust the amplitude and phase of this feedback signal in such a way that it acts to *improve*, rather than degrade, the input current waveshape.

Consider the dcm boost rectifier, with the duty ratio modulated according to

$$d(\theta) = D + \tilde{d}\cos 2\theta \tag{8.4.1}$$

where D and $\tilde{d}$ are constants to be determined. Again assuming that the output voltage is constant, equation (8.1.1) gives the switching frequency averaged input current to the converter under this modulation

$$i_g(\theta) = \frac{D^2 T_s}{2L} V_p \left[1 + \frac{\tilde{d}}{D}\cos 2\theta\right]^2 \frac{|\sin\theta|}{1 - \frac{1}{M_p}|\sin\theta|} \tag{8.4.2}$$

The optimal modulation amplitude, $\tilde{d}^*$, is defined as the modulation amplitude which, for a given operating condition, maximizes the input power factor. To find the value for the optimal modulation amplitude, we need to evaluate the power factor under this type of duty ratio modulation. Using the results of chapter 2 and appendix A, the power factor in this case can be written

$$PF = \sqrt{\frac{2}{\pi}} \frac{\int_0^\pi i_g(\theta)\sin\theta\, d\theta}{\sqrt{\int_0^\pi i_g^2(\theta)\, d\theta}} \tag{8.4.3}$$

Substituting equation (8.4.2) for the converter input current gives

$$PF = \sqrt{\frac{2}{\pi}} \frac{\int_0^\pi (1+\alpha\cos 2\theta)^2 \frac{\sin^2\theta}{M_p - \sin\theta}\, d\theta}{\sqrt{\int_0^\pi \left[(1+\alpha\cos 2\theta)^2 \frac{\sin\theta}{M_p - \sin\theta}\right]^2 d\theta}} \tag{8.4.5}$$

where the modulation index α is defined as the ratio of the modulation amplitude to the dc component of the duty ratio

$$\alpha \equiv \frac{\tilde{d}}{D} \tag{8.4.6}$$

For a given value of the peak conversion ratio M_p, the power factor can be plotted as a function of modulation index α, as shown in figure 8.7. Examination of this plot shows that for each value of the conversion ratio, the power factor can be made remarkably close to unity, by the proper choice of the modulation index. Hence, for each value of the conversion ratio M_p, there exists an optimum value of the modulation index for which the power factor is maximum.

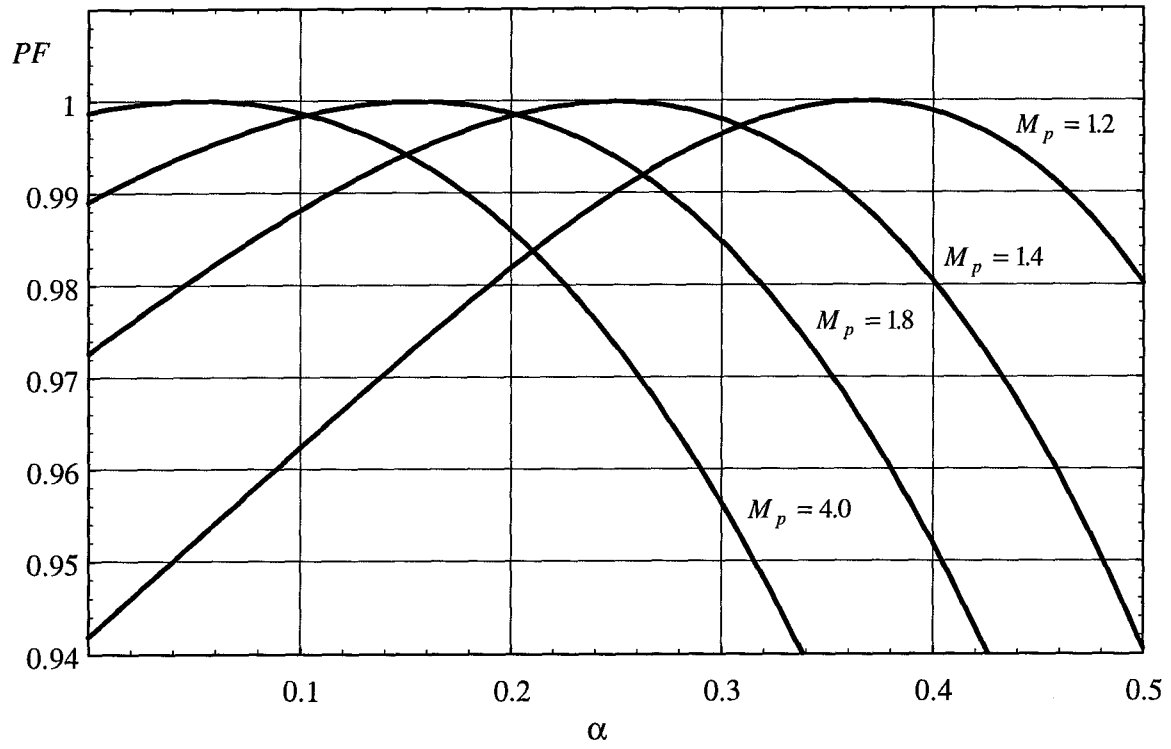


Figure 8.7: Input power factor for the dcm boost rectifier as a function of modulation index α *for several values of peak conversion ratio* M_p.

We can plot the optimum value of the modulation index, α^*, as a function of conversion ratio M_p by locating numerically the value of α for which the power factor is maximum for a specific value of M_p, and repeating this process for many values of M_p in the desired range. This procedure was used to generate the plot in figure 8.8. The information contained in the plot is not immediately useful however, because it gives the optimal value of the ratio $\tilde{d}/D$, but the dc component D is not known. To find this component, we equate the average input power with the output power, and solve for the duty ratio as a function of the conversion ratio M_p, conduction parameter K, and the modulation index α:

$$D(M_p, K, \alpha) = \sqrt{\frac{M_p K}{\frac{1}{\pi}\int_0^{\pi} (1+\alpha\cos 2\theta)^2 \frac{\sin^2\theta}{M_p - \sin\theta}\, d\theta}} \tag{8.4.7}$$

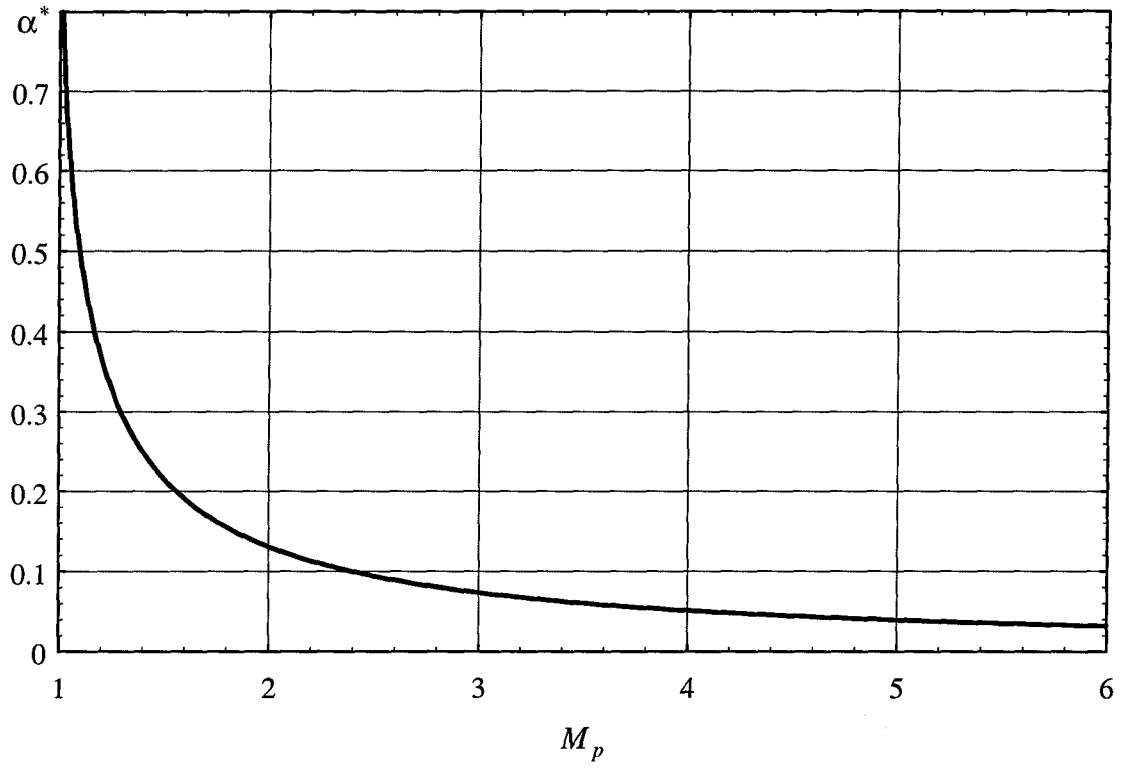


Figure 8.8: Optimum value of the modulation index, α^*, as a function of peak conversion ratio M_p.

If the duty ratio is modulated in an optimal manner, that is, if the value of the modulation index is that which maximizes the input power factor, then the modulation index α is equal to its optimum value α^*. We define the optimum value of the dc component of the duty ratio

$$D^*(M_p, K) \equiv D\left(M_p, K, \alpha^*(M_p)\right) \tag{8.4.8}$$

The optimum modulation amplitude, $\tilde{d}^*$, can then be written as a function of the conversion ratio M_p, and conduction parameter K:

$$\tilde{d}^*(M_p, K) = \alpha^*(M_p) D^*(M_p, K) \tag{8.4.9}$$

The dependence on conduction parameter K is easily extracted, to form a new ratio which is a function of the conversion ratio alone:

$$\frac{\tilde{d}^*}{\sqrt{K}}(M_p) = \alpha^*(M_p)\sqrt{\frac{M_p}{\frac{1}{\pi}\int_0^{\pi}\left(1+\alpha^*(M_p)\cos 2\theta\right)^2 \frac{\sin^2\theta}{M_p - \sin\theta}\, d\theta}} \tag{8.4.10}$$

This function is plotted below in figure 8.9, and is now in a useful form since, given the operating conditions of the rectifier circuit, the optimal value of the modulation amplitude, $\tilde{d}^*$, is easily determined. A magnified plot of this same function is given in figure 8.10, which is useful for determining the optimal modulation amplitude for low values of the peak conversion ratio.

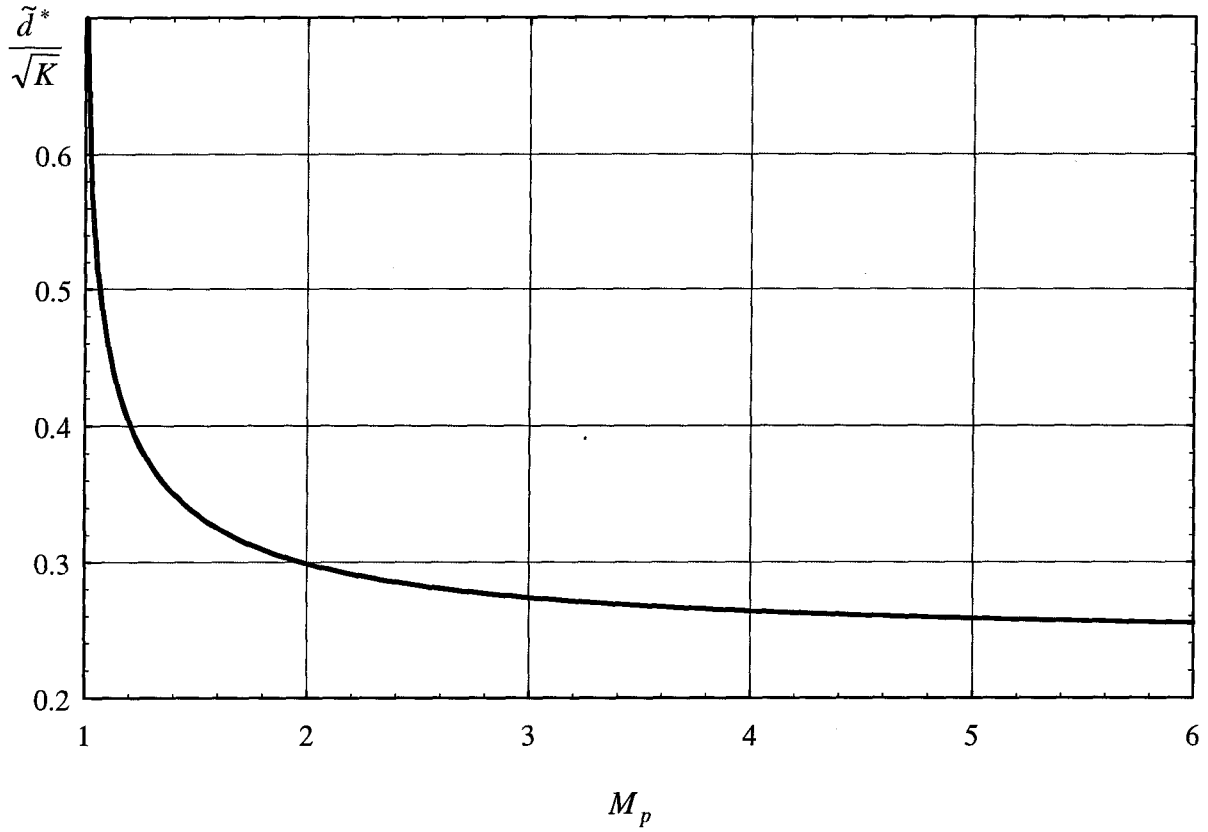


Figure 8.9: Optimal modulation ratio $\tilde{d}^*/\sqrt{K}$ for the dcm boost rectifier as a function of conversion ratio M_p.

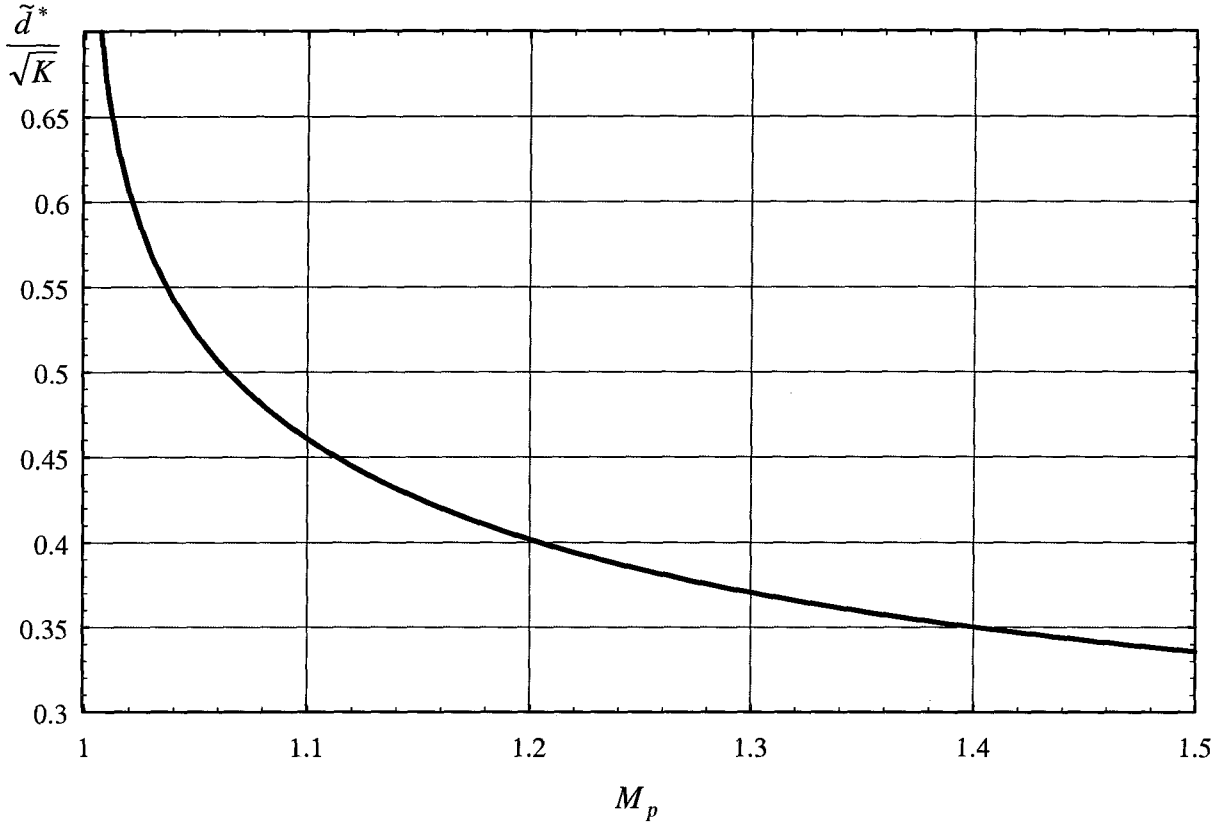


Figure 8.10: Optimal modulation ratio $\tilde{d}^*/\sqrt{K}$ for the dcm boost rectifier as a function of conversion ratio M_p, expanded for low values of the conversion ratio.

8.4.2 Optimal Voltage Feedback

The motivation for deriving the optimal duty ratio modulation amplitude is that a signal of the necessary frequency is available within the rectifier, and it is normally fed back anyway! This signal is of course the output voltage, and the idea behind optimal voltage feedback is to adjust the amplitude and phase of the output voltage signal, fed back through the feedback amplifier, so that it acts to improve, rather than degrade, the input power factor. Using simple linear feedback, it is not possible to optimize the duty ratio modulation amplitude for all operating conditions. However, this approach does provide substantial performance improvement over the standard constant duty ratio dcm boost rectifier, including improved power factor, improved transient response, and increased efficiency.

A block diagram of the optimal voltage feedback dcm boost rectifier is shown below in figure 8.11. The circuit is basically the same as the constant duty ratio dcm boost rectifier, except the ordinary feedback amplifier is replaced with the optimal voltage feedback amplifier, $A^*(s)$. This section is concerned with the determination of this optimal gain function.

If the modulation amplitude is optimal, then the rectifier operates with nearly unity input power factor, as demonstrated in the plots of figure 8.7. In chapter 4, under the assumption of unity input power factor and zero converter energy storage, we showed that the voltage across the energy storage capacitor is determined, and can be approximated by

$$v_C(\theta) \cong V_C + \tilde{v}_C \sin 2\theta \tag{8.4.11}$$

Further, the amplitude of the ac component can be approximated by

$$\tilde{v}_C \cong -\frac{P}{2\omega_l C V_C} \tag{8.4.12}$$

Now, the optimal duty ratio modulation function is given by

$$d^*(\theta) = D^* + \tilde{d}^* \cos 2\theta \tag{8.4.13}$$

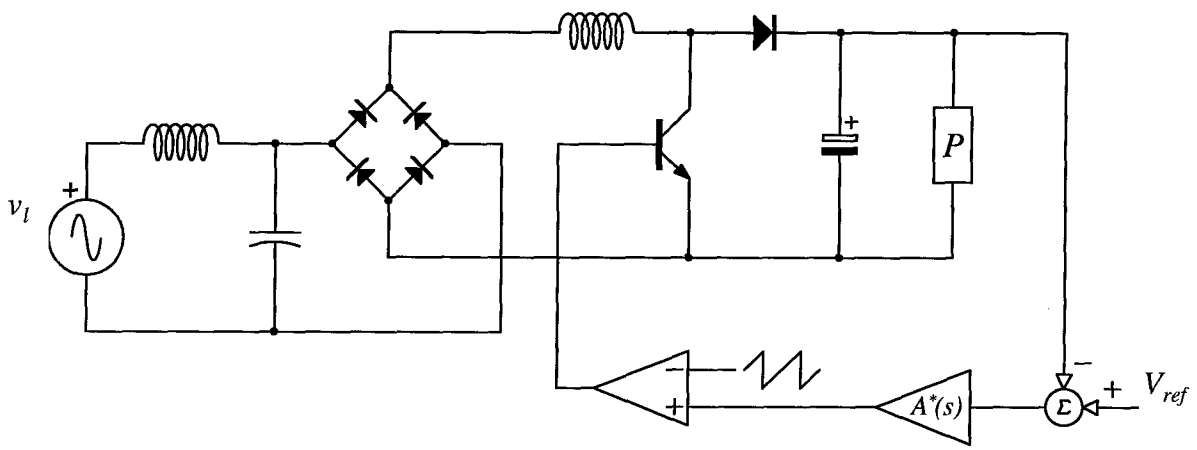


Figure 8.11: Optimal voltage feedback dcm boost rectifier.

The goal is to design the feedback amplifier so that the duty ratio is modulated in accordance with the optimal modulation function, in both amplitude and phase. The dc components are automatically taken care of by the integrator to be included in the optimal feedback amplifier, which nulls the steady-state dc error. To determine the magnitude and phase of the optimal feedback amplifier gain at twice the line frequency, we first need to know the modulator gain. For the standard linear ramp type modulator, the gain is simply

$$\tilde{d} = \frac{v_+}{V_{ramp}} \tag{8.4.14}$$

where v_+ is the voltage at the "+" terminal of the modulator comparator, and V_{ramp} is the peak-to-peak value of the ramp sawtooth. The feedback amplifier gain is defined by the ratio

$$A(s) \equiv -\frac{v_+}{v_C}(s) \tag{8.4.15}$$

The magnitude of the optimal feedback amplifier gain, evaluated at twice the line frequency, is therefore

$$\left|A^*(j2\omega_l)\right| = \frac{\tilde{d}^* V_{ramp}}{\left|\tilde{v}_C\right|} \tag{8.4.16}$$

Taking into account the phase inversion at the summing node, the proper phase of the fed-back signal is obtained by adding 90 degrees of phase-shift to the output voltage signal. Thus, at twice the line frequency, the optimal feedback amplifier should exhibit 90 degrees of phase lead, and have voltage gain magnitude as given by (8.4.16). As mentioned previously, the optimal feedback amplifier must also incorporate an integrator in order to null the steady-state dc error. Finally, while satisfying these requirements, the optimal feedback amplifier must also be designed so that the overall feedback loop is stable.

8.4.3 Optimal Feedback Amplifier Design

The optimal feedback amplifier is one which, for a given operating condition, amplifies the ripple in the output voltage at twice the line frequency with the proper

magnitude and phase so that the duty ratio is modulated in an optimal manner, thereby maximizing the input power factor. Because optimality of the feedback amplifier depends only on the magnitude and phase of the amplifier voltage gain characteristic at one particular frequency, neither the amplifier configuration nor its transfer function is unique. In addition, because the feedback amplifier gain is fixed, optimality cannot be achieved for all operating conditions.

It is difficult to demonstrate the stability of the feedback loop with a rectified ac input. The quasi-static approximation [9] is applicable when the operating point variations occur at frequencies which are low with respect to the bandwidth of the feedback loop. Conversely, line frequency averaging [12] is applicable when the bandwidth of the feedback loop is well below the frequencies at which the operating point is varying. In the present situation, the bandwidth of the control loop and the fundamental frequency of the operating point variations are of the same order, and thus neither approximation is justified.

To get past this problem, stability is verified considering only average dc conditions; i.e., under the assumption that the input voltage is a constant dc source, with value equal to the average value of the rectified ac input voltage. It is then assumed that the introduction of the rectified ac input does not cause this feedback loop to be unstable. For a dc input voltage source, the dcm pwm switch model of chapter 6 can be used to determine the dc and small-signal ac circuit models for the boost converter, as shown in figure 8.12. Note that the constant power load is modeled as a positive resistor in the dc model, emulating the large-signal dc characteristic of this type of load, and as a negative resistor in the ac model, emulating the small-signal ac characteristic in the dynamic model.

From the reduced ac model in figure 8.12(d), the control-to-output transfer function of the dcm boost converter with constant power load is given by

$$\frac{\hat{v}_o}{\hat{d}}(s) = 2V_o\sqrt{\frac{\overline{M}-1}{K\overline{M}}}\,\frac{1}{1+s/\omega_p} \quad ; \quad \omega_p = \frac{1}{(\overline{M}-1)RC} \tag{8.4.17}$$

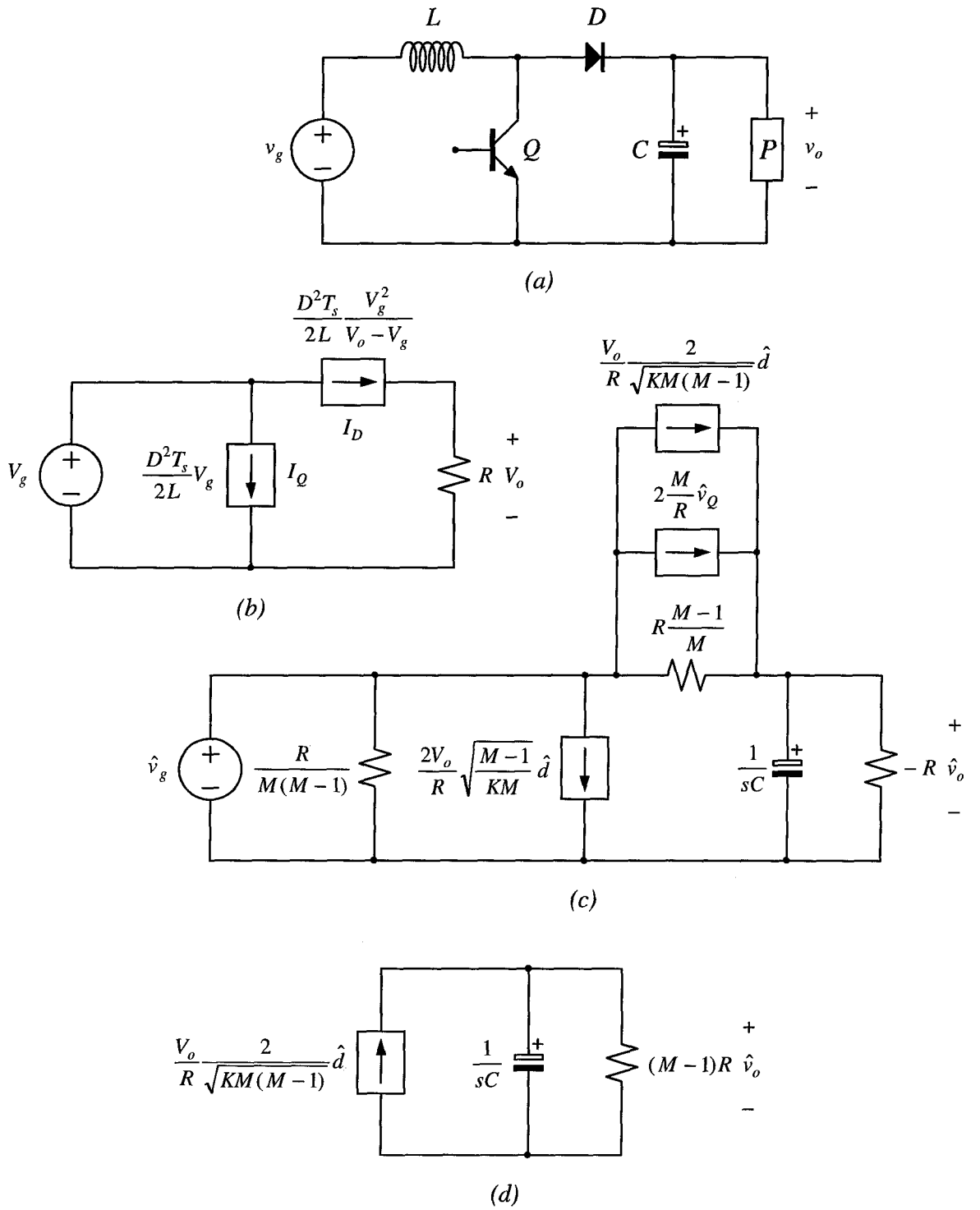


Figure 8.12: (a) Boost converter with constant power load, (b) dcm dc circuit model, (c) complete dcm ac circuit model, (d) reduced ac model for computation of the control-to-output transfer function.

where $\overline{M}$ is the average value of the conversion ratio, which is related to the peak conversion ratio by

$$\overline{M} = \frac{\pi}{2} M_p \tag{8.4.18}$$

The sketch of the transfer function magnitude $|A^*(s)|$ in figure 8.13 achieves optimality. The frequency of the complex pair of zeros, ω_{z2}, is chosen to coincide with twice the line frequency. Zero ω_{z1} is chosen to be well below twice the line frequency, so that the 90 degree phase lag introduced by the integrator pole at $s = 0$ will be nearly nullified at twice the line frequency. Then, at twice the line frequency, each zero of the complex zero pair acts to contribute 45 degrees of phase lead, totaling the desired 90 degrees of phase lead necessary for optimality. The complex pair of poles at ω_{p1} are then added to prevent the loop gain from becoming too large, and rolling off the loop gain at a reasonable fraction of the switching frequency. Finally, pole ω_{p2} is added at a high frequency to attenuate switching ripple in the feedback loop, and to predictably roll-off the gain of the feedback amplifier at high frequencies. The reader can easily verify that the overall loop gain function is stable.

The quality factor Q_z associated with the complex zero pair is chosen to be unity as a compromise between two conflicting design criteria. The first is for the circuit to be insensitive to an error in the frequency of the complex zero pair, since an error here causes the phase of the fed back signal at twice the line frequency to be other than 90 degrees. For $Q = 1$, the phase transition is not particularly rapid, as shown in figure 8.14. Thus, if component tolerances cause the zero frequency to shift with respect to twice the line frequency, the phase error measured at the modulator will not be large. This requirement is in conflict with the desirability for the overall loop gain $T(s)$ to be large over as broad a frequency range as is possible. Inspection of the loop gain magnitude function in figure 8.13 shows that, by design, the loop gain magnitude function has a local minimum at twice the line frequency. A larger value for Q_z, while maintaining the optimal feedback amplifier gain at twice the line frequency fixed, causes the overall loop gain $T(s)$ to rise by this same amount Q_z. However, the rapid phase transition renders high values for Q_z impractical.

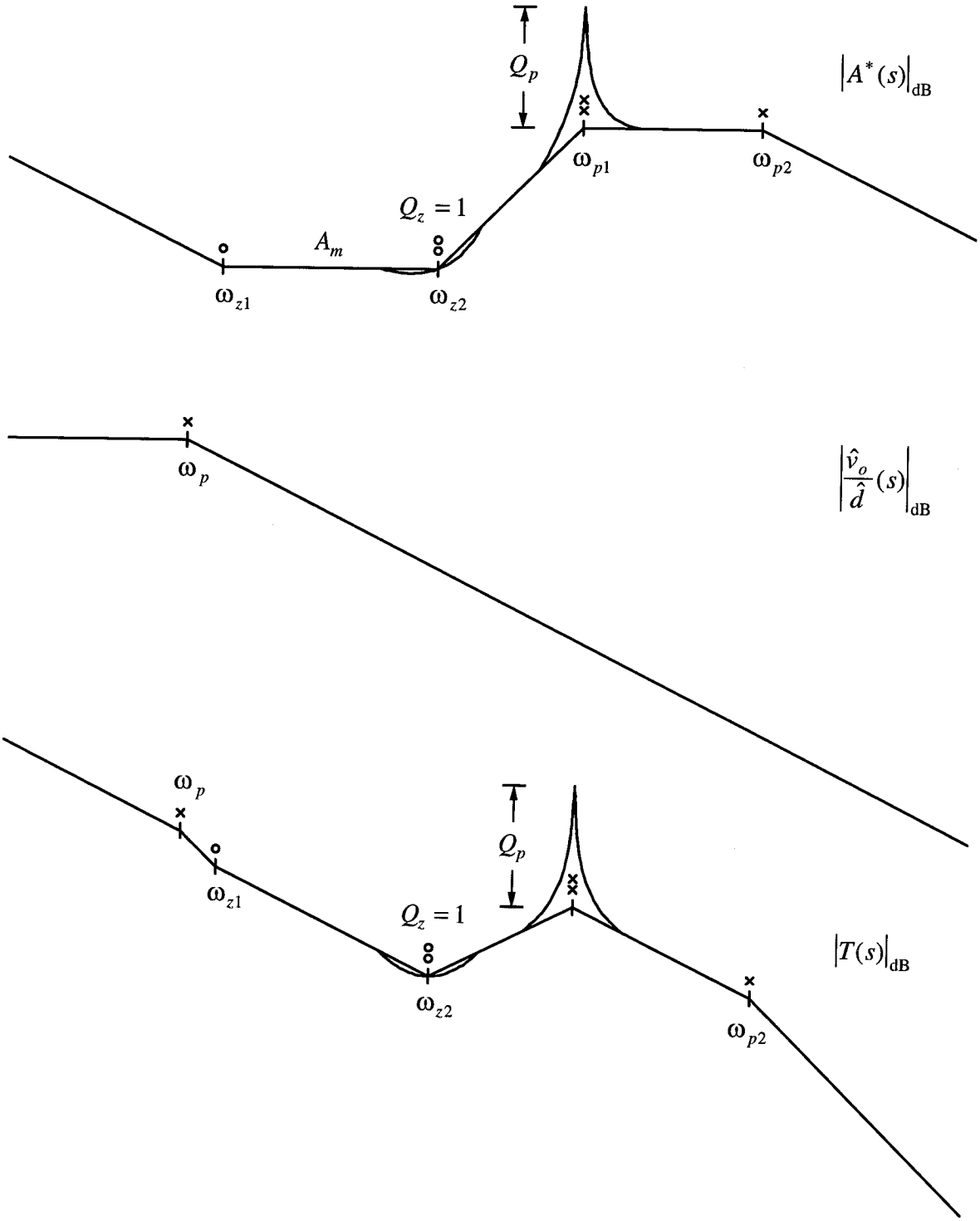


Figure 8.13: Magnitude sketches of: the optimal feedback amplifier voltage gain $A^*(s)$, the small-signal control-to-output transfer function $\hat{v}_o(s)/\hat{d}(s)$, and loop gain $T(s)$.

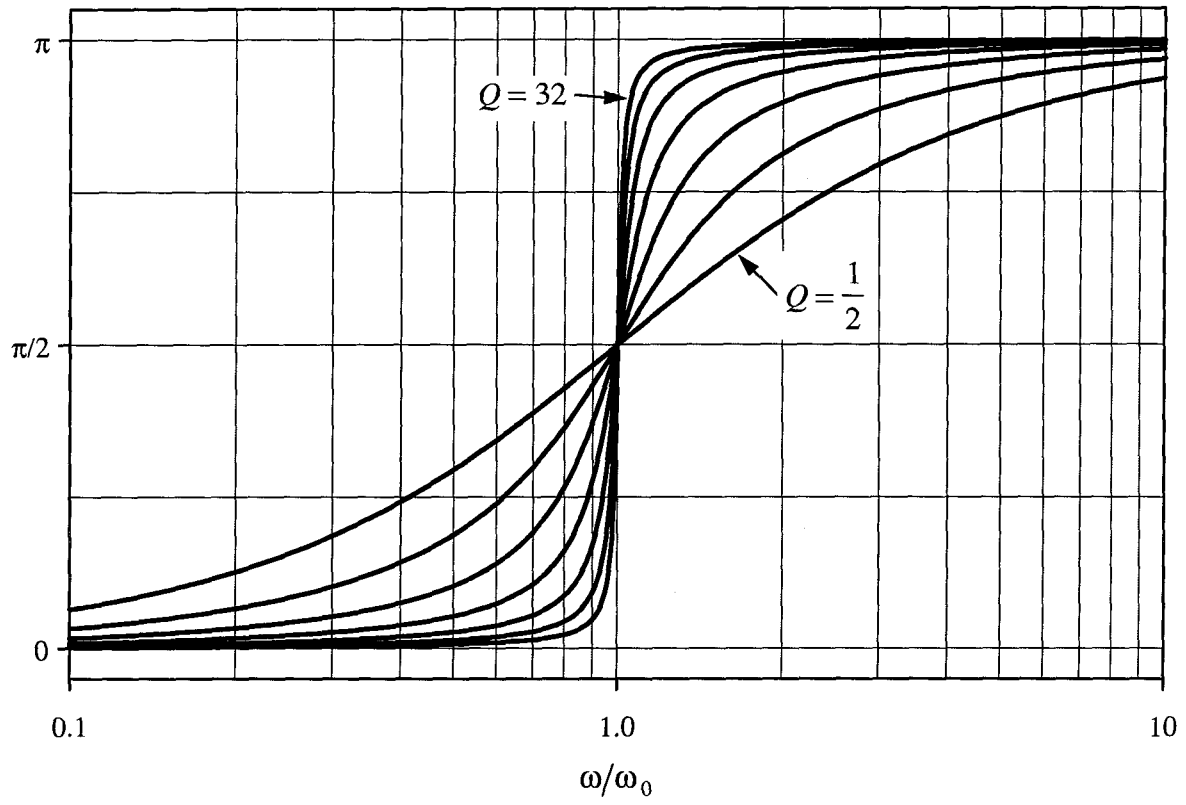


Figure 8.14: Phase angle of the quadratic expression $f(s) = 1 + \frac{1}{Q}(\frac{s}{\omega_0}) + (\frac{s}{\omega_0})^2$ *evaluated at* $s = j\omega$, *as a function of normalized frequency* ω/ω_0 *for* $Q = \frac{1}{2}$, 1, 2, 4, 8, 16, and 32.

The quality factor Q_p associated with the complex pole-pair should be chosen to be large enough that the phase lag introduced by these poles has little influence at twice the line frequency. Again referring to figure 8.14, this requirement implies that the value for Q_p must be chosen correspondingly large, if the complex pole-pair frequency is to be kept to a reasonable low value.

From the optimal voltage feedback amplifier magnitude sketch in figure 8.13, the required amplifier transfer function can be written by inspection:

$$A^*(s) = A_m \frac{1 + \frac{\omega_{z1}}{s}}{1 + \frac{s}{\omega_{p2}}} \frac{1 + \frac{1}{Q_z}(\frac{s}{\omega_{z2}}) + (\frac{s}{\omega_{z2}})^2}{1 + \frac{1}{Q_p}(\frac{s}{\omega_{p1}}) + (\frac{s}{\omega_{p1}})^2} \tag{8.4.19}$$

In the next section, the realization of a feedback amplifier with this characteristic is given for an actual design example, followed by experimental results demonstrating the performance characteristics of the optimal voltage feedback dcm boost rectifier.

8.5 Optimal Voltage Feedback Dcm Boost Rectifier Design Example

In this section, optimal voltage feedback is used in the design of a 200W dcm boost rectifier with a constant power load. The rectifier is designed to operate for input voltages from 85-265 Vrms, 60Hz, and to have a 400Vdc output. The peak-to-peak output voltage ripple at 120Hz (twice the line frequency) shall be less than 5% of the dc output voltage. The switching frequency is chosen to be 100KHz. Operation is to be from zero load to full load. The design strategy is to design the rectifier so that optimality is achieved under worst-case conditions: namely high line and maximum load. Under these conditions, with optimal voltage feedback, the power factor will be nearly unity. Under other conditions, the voltage feedback may be sub-optimal, but excellent performance is observed anyway.

8.5.1 Converter Design

The inductor is chosen to be as large as possible while maintaining discontinuous operation over the entire line period. A larger inductor leads to lower peak current in the converter for the same operating condition, thereby reducing component stress and increasing efficiency. At high line (265Vrms) the peak conversion ratio is only 1.07. Since the feedback is to be optimal at high line and full load, we may assume that the power factor is unity under this condition for the purpose of choosing the inductor. Referring to figure 8.5, for unity power factor operation, $M_p = 1.07$ corresponds to $\tilde{K}_{\text{crit,dcm}} = 0.028$. Therefore, for discontinuous operation, we require

$$K \equiv \frac{2L}{RT_s} < \tilde{K}_{\text{crit,dcm}} \tag{8.5.1}$$

Substituting the equivalent load resistance of 800Ω, the inductor is required to be less than $112\mu H$. To provide some margin, we choose $L = 100\mu H$.

From figure 8.4, this choice for the inductor also satisfies (8.5.1) under the low-line condition, $M_p = 3.33$, assuming either unity power factor or constant duty ratio control. In fact, for the present case, since the feedback is optimized at high line and full power, the modulation of the duty ratio at low line and full power is actually larger than optimal under low-line conditions, ensuring discontinuous operation over the entire line cycle.

The energy storage capacitor is chosen from the ripple requirement. Using equation (8.4.12), the output voltage ripple is approximately

$$\frac{|\tilde{v}_C|}{V_C} \cong \frac{1}{2\omega_l CR} \tag{8.5.2}$$

where $|\tilde{v}_C|$ is the peak value of the output voltage ripple at twice the line frequency. From this expression, the required capacitor value is 66μF. To provide some margin and also due to component availability, the chosen capacitor is an electrolytic type of value $C = 80\mu F$. It is important to verify that the equivalent series resistance (esr) of this capacitor is small with respect to its reactance at twice the line frequency. Finally, in addition to the large electrolytic capacitor, a relatively small (1.2μF) mylar capacitor is added in parallel to absorb the switching frequency ripple current, since the impedance of the electrolytic type capacitor is not particularly low at the switching frequency. This completes the selection of the converter component values.

8.5.2 Optimal Feedback Amplifier Realization

The required feedback amplifier transfer function can be realized using any one of a variety of circuits. In this example, the amplifier is realized from the cascade connection of a standard output voltage feedback amplifier, followed by a specially designed biquadratic filter, as shown in figure 8.15. The circuit shown is easily implemented with a standard quad op-amp. With the standard feedback amplifier section, we realize the transfer function

$$A_1(s) = A_m \frac{1+\frac{\omega_{z1}}{s}}{1+\frac{s}{\omega_{p2}}} \tag{8.5.3}$$

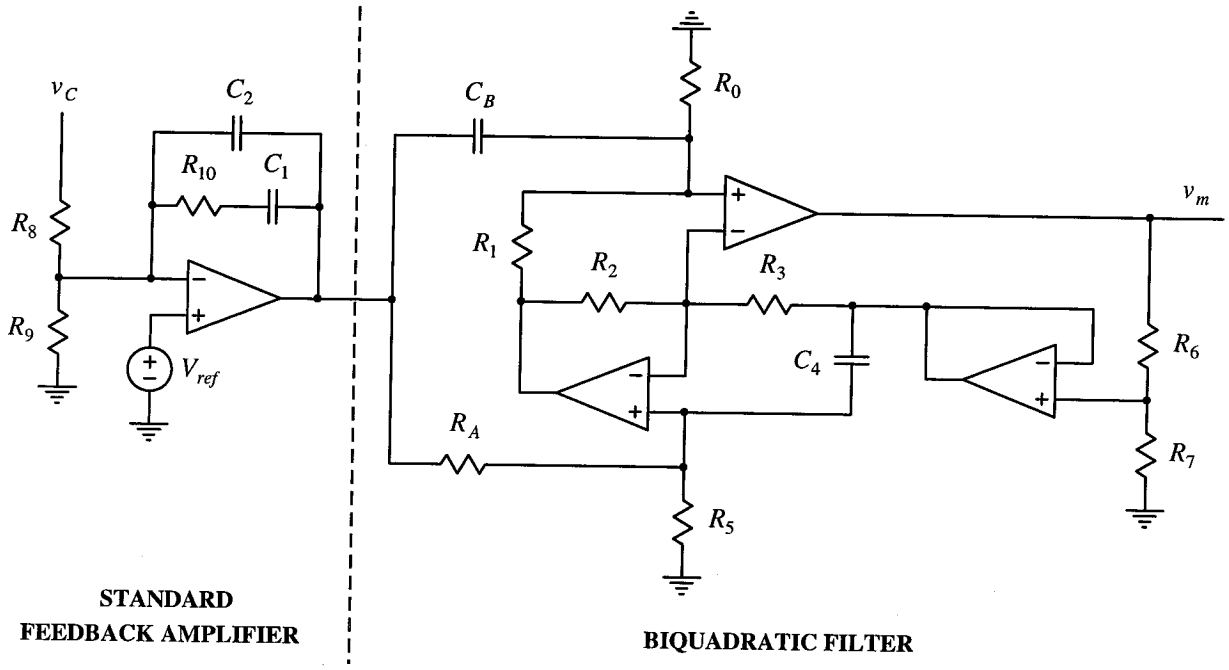


Figure 8.15: Optimal voltage feedback amplifier circuit realization.

and with the biquadratic filter section, we realize

$$A_2(s) = \frac{1 + \frac{1}{Q_z}\left(\frac{s}{\omega_{z2}}\right) + \left(\frac{s}{\omega_{z2}}\right)^2}{1 + \frac{1}{Q_p}\left(\frac{s}{\omega_{p1}}\right) + \left(\frac{s}{\omega_{p1}}\right)^2} \tag{8.5.4}$$

The overall voltage gain of the voltage feedback amplifier is then given by the product

$$A^*(s) = A_1(s)A_2(s) \tag{8.5.5}$$

The complex zero pair frequency is chosen to coincide with twice the line frequency. At this frequency, the magnitude of the amplifier gain is approximately

$$\left|A(j2\omega_l)\right| \cong \frac{A_m}{Q_z} \tag{8.5.6}$$

and since we've agreed to set $Q_z = 1$, the magnitude of the voltage gain at twice the line frequency is simply A_m. To optimize the gain for operation high line ($M_p = 1.07$) and

maximum load (200W), the optimum duty ratio modulation is found from the curve in figure 8.10:

$$\left.\frac{\tilde{d}^*}{\sqrt{K}}\right|_{M_p=1.07} = 0.49 \tag{8.5.7}$$

From equation (8.3.6), the optimal midband gain, A_m^*, is therefore

$$A_m^* = \frac{(0.49)\sqrt{K}V_{ramp}}{|\tilde{v}_C|} \tag{8.5.8}$$

From equation (8.3.4), the amplitude of the output voltage ripple at twice the line frequency $|\tilde{v}_C|$, at maximum load, is 8.3V. Looking ahead to the actual circuit prototype in figure 8.18, the sawtooth ramp voltage is 2Vp-p, but is preceded by a 3:1 voltage divider. This makes the effective ramp voltage 6Vp-p. Hence, the optimal midband gain is

$$A_m^* = 0.056 \tag{8.5.9}$$

The reference voltage is $V_{ref} = 5\text{V}$. The divider ratio set up by resistors R_8 and R_9 should therefore be 80:1 to derive the 400Vdc output. Thus, choosing $R_8 = 1\text{M}\Omega$ gives $R_9 = 12.7\text{K}$. The midband gain of the standard feedback amplifier section is given by the ratio R_{10}/R_8. Setting this equal to the optimal midband gain in equation (8.5.9) gives $R_{10} = 56\text{K}$. Zero ω_{z1} is placed a decade below twice the line frequency at 12Hz, for reasons explained earlier. In the circuit, the zero frequency determined by

$$\omega_{z1} = \frac{1}{R_{10}C_1} \tag{8.5.10}$$

which gives $C_1 = 0.24\mu\text{F}$. We use the nearest standard value, $C_1 = 0.22\mu\text{F}$. Pole ω_{p2} is given by

$$\omega_{p2} = \frac{1}{R_{10}C_2} \tag{8.5.11}$$

Placing this pole at 5KHz to attenuate switching frequency ripple and noise in the feedback loop, gives $C_2 = 570\text{pF}$. We use the nearest standard value $C_2 = 560\text{pF}$. This completes the design of the standard feedback amplifier section.

Biquadratic Filter Design

The biquadratic filter section is designed through the synthesis procedure described in this section. The biquadratic transfer function to be realized is given by equation (8.5.4). The complex zero-pair is placed at twice the line frequency with quality factor $Q_z = 1$. From figure 8.14, in order to avoid excessive phase shift at twice the line frequency, the complex pole-pair corner frequency is chosen to be 5 times the complex zero-pair frequency, $\omega_{p1} = 5\omega_{z2}$, with associated quality factor $Q_p = 5$. With these design requirements, we proceed with analysis of the general biquadratic filter section, from which the desired optimal transfer function is synthesized.

The general biquadratic filter section [32] is shown in figure 8.16, where circuit elements have been characterized by their admittance parameters. Admittance parameters are chosen because they make analysis of this circuit easy, and are useful in the synthesis procedure that follows. Assuming the op-amps are ideal, we begin by writing KCL equations at nodes *a*, *b*, and *c*:

$$\begin{aligned} (v_d - v_a)Y_1 + (v_1 - v_a)Y_B - v_a Y_0 &= 0 \\ (v_d - v_b)Y_2 + (v_2 - v_b)Y_3 &= 0 \\ (v_2 - v_c)Y_4 + (v_1 - v_c)Y_A - v_c Y_5 &= 0 \end{aligned} \tag{8.5.12}$$

Assuming that the circuit is stable, the voltage across the input terminals of each op-amp is zero. Thus, we have

$$v_a = v_b = v_c \tag{8.5.13}$$

Equations (8.5.12) and (8.5.13) can be solved for the voltage transfer function v_2/v_1. Doing so gives

$$\frac{v_2}{v_1} = \frac{Y_A(Y_1Y_3 - Y_0Y_2) + Y_2Y_B(Y_4 + Y_5)}{Y_1Y_3(Y_A + Y_5) + Y_2Y_4(Y_B + Y_5)} \tag{8.5.14}$$

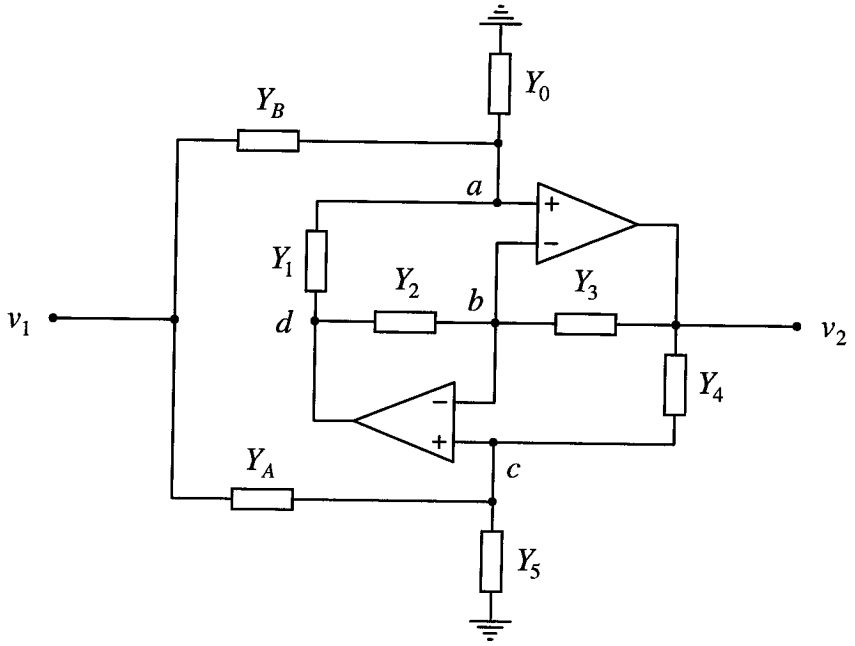


Figure 8.16: General biquadratic section.

The synthesis of a desired transfer function is performed by substituting element (or network) admittances into this expression. Since the desired transfer function is second order, the circuit will contain two capacitors (we restrict ourselves to the use of capacitors as reactive elements). The remaining circuit elements will be conductances. If we try substituting capacitors for admittances Y_4 and Y_B, and conductances for the remaining elements, we immediately arrive at the biquadratic transfer function

$$\frac{v_2}{v_1}(s) = \frac{G_A(G_1G_3 - G_0G_2) + sC_BG_2G_5 + s^2C_BC_4G_2}{G_1G_3(G_A + G_5) + sC_4G_0G_2 + s^2C_BC_4G_2} \tag{8.5.15}$$

Written in another form, this becomes

$$\frac{v_2}{v_1}(s) = \frac{G_AG_1G_3 - G_AG_0G_2}{G_AG_1G_3 + G_1G_3G_5} \frac{1 + s\dfrac{C_BG_2G_5}{G_AG_1G_3 - G_AG_0G_2} + s^2\dfrac{C_BC_4G_2}{G_AG_1G_3 - G_AG_0G_2}}{1 + s\dfrac{C_4G_0G_2}{G_AG_1G_3 + G_1G_3G_5} + s^2\dfrac{C_BC_4G_2}{G_AG_1G_3 + G_1G_3G_5}} \tag{8.5.16}$$

Aside from the fact that the dc gain is not unity, this expression reveals that this is indeed of the desired form, with the complex zero-pair frequency below the complex

pole-pair frequency. Inspection of equation (8.5.15) shows that it is the high frequency gain, rather than the dc gain, which is unity for this circuit. This minor problem will be resolved at the end of the synthesis process. Put in standard pole-zero form, the transfer function can be written

$$\frac{v_2}{v_1}(s) = A_0 \frac{1+\frac{1}{Q_z}(\frac{s}{\omega_z})+(\frac{s}{\omega_z})^2}{1+\frac{1}{Q_p}(\frac{s}{\omega_p})+(\frac{s}{\omega_p})^2} \tag{8.5.17}$$

where the dc gain, corner frequencies, and quality factors are given by

$$A_0 = \frac{G_A G_1 G_3 - G_A G_0 G_2}{G_A G_1 G_3 + G_1 G_3 G_5} = (\frac{\omega_z}{\omega_p})^2$$

$$\omega_z = \sqrt{\frac{G_A G_1 G_3 - G_A G_0 G_2}{C_B C_4 G_2}} \qquad Q_z = \frac{1}{G_5}\sqrt{\frac{G_A G_1 G_3 - G_A G_0 G_2}{G_2}}\sqrt{\frac{C_4}{C_B}} \tag{8.5.18}$$

$$\omega_p = \sqrt{\frac{G_A G_1 G_3 + G_1 G_3 G_5}{C_B C_4 G_2}} \qquad Q_p = \frac{1}{G_0}\sqrt{\frac{G_A G_1 G_3 + G_1 G_3 G_5}{G_2}}\sqrt{\frac{C_B}{C_4}}$$

Observe that these expressions do not depend on G_1, G_2, and G_3 independently, but rather on the ratio $G_1 G_3 / G_2$. Hence, they may be written

$$A_0 = \frac{1 - G_0 \frac{G_2}{G_1 G_3}}{1+\frac{G_5}{G_A}}$$

$$\omega_z = \sqrt{\frac{G_A}{C_B C_4}\left[\frac{G_1 G_3}{G_2} - G_0\right]} \qquad Q_z = \frac{1}{G_5}\sqrt{G_A\left[\frac{G_1 G_3}{G_2} - G_0\right]}\sqrt{\frac{C_4}{C_B}} \tag{8.5.19}$$

$$\omega_p = \sqrt{\frac{G_1 G_3}{G_2}\cdot\frac{G_A + G_5}{C_B C_4}} \qquad Q_p = \frac{1}{G_0}\sqrt{\frac{G_1 G_3}{G_2}(G_A + G_5)}\sqrt{\frac{C_B}{C_4}}$$

which leaves two degrees of freedom in choosing values for G_1, G_2, and G_3. Taking the ratio of the quality factors gives

$$\frac{Q_p}{Q_z} = \frac{C_B}{C_4}\frac{G_5}{G_0}\frac{\omega_p}{\omega_z} \tag{8.5.20}$$

From a practical standpoint, it is preferable for the capacitors to have the same value, so that identical capacitors can be used in the actual circuit. Thus, let $C_B = C_4$. Next, we normalize admittance parameters with respect to G_0, and frequency with respect to twice the line frequency $2\omega_l$:

$$y = g + jb = \frac{G + jB}{G_0} \quad ; \quad \Omega = \frac{\omega}{2\omega_l} \tag{8.5.21}$$

The normalized circuit parameters then become

$$g_k = \frac{G_k}{G_0} \qquad \Omega_m = \frac{\omega_m}{2\omega_l} \qquad c_n = \frac{2\omega_l C_n}{G_0} \tag{8.5.22}$$

Trivially, we have $g_0 = 1$. The normalized design objectives are

$$\begin{aligned} \Omega_z &= 1 \qquad & Q_z &= 1 \\ \Omega_p &= 5 \qquad & Q_p &= 5 \end{aligned} \tag{8.5.23}$$

From the ratio of the quality factors in equation (8.5.20):

$$\frac{Q_p}{Q_z} = 5 \quad \Rightarrow \quad g_5 = 1 \tag{8.5.24}$$

Squaring the expressions for Q_z and Q_p in (8.5.19):

$$Q_z^2 = g_A\left(\frac{g_1 g_3}{g_2} - 1\right) \qquad Q_p^2 = \frac{g_1 g_3}{g_2}(1 + g_A) \tag{8.5.25}$$

Solving each expression for the ratio $g_1 g_3 / g_2$, and equating gives

$$\frac{g_1 g_3}{g_2} = \frac{Q_z^2}{g_A} + 1 = \frac{Q_p^2}{1 + g_A} \tag{8.5.26}$$

which, when solved for g_A, gives the quadratic

$$g_A^2 + (1 + Q_z^2 - Q_p^2) g_A + Q_z^2 = 0 \tag{8.5.27}$$

The roots of this equation are real whenever $Q_p/Q_z \geq 2$, and are real and positive whenever $Q_p/Q_z > 2$. For the design goal $Q_p/Q_z = 5$, the roots are approximately given by $g_A \cong 22.96$ and $g_A \cong 0.04356$. If we were to choose the larger root, then from equation (8.5.26):

$$\frac{g_1 g_3}{g_2} = \frac{Q_z^2}{g_A} + 1 \cong 1.0435 \tag{8.5.28}$$

From the expressions in (8.5.19), we can show that with $g_0 = 1$, the values for A_0, ω_z, and Q_z are extremely sensitive to the value of the ratio $g_1 g_3/g_2$, when this ratio is close to one. However, choosing the smaller root for g_A alleviates this problem. For the smaller root, we have

$$\frac{g_1 g_3}{g_2} = \frac{Q_z^2}{g_A} + 1 \cong 23.96 \tag{8.5.29}$$

Since we have assumed that the capacitor values are equal, the normalized capacitor values are $c_B = c_4 = c$. From equation (8.5.19), the normalized complex zero-pair corner frequency can then be written

$$\Omega_z = \frac{1}{c}\sqrt{g_A\left(\frac{g_1 g_3}{g_2} - g_0\right)} \tag{8.5.30}$$

Substituting equation (8.5.29) for the ratio $g_1 g_3/g_2$, with $g_0 = 1$, gives simply

$$\Omega_z = \frac{Q_z}{c} \tag{8.5.31}$$

from which we conclude that $c = 1$. Summarizing the results, we found

$$\begin{aligned} g_0 &= 1 & g_5 &= 1 \\ \frac{g_1 g_3}{g_2} &= 23.96 & g_A &= 0.04356 \\ c_4 &= 1 & c_B &= 1 \end{aligned} \tag{8.5.32}$$

If we arbitrarily select $g_2 = 1$ and $g_1 = g_3$, the circuit element values can be found by de-normalizing and converting the admittance parameters to impedance parameters.

With the normalizing conductance G_0 chosen to be $G_0 = (10\text{K}\Omega)^{-1}$, the circuit element values are

$$\begin{aligned} R_0 &= R_2 = R_5 = 10\text{K} \quad (10\text{K}) \\ R_1 &= R_3 = 2.04\text{K} \quad (2\text{K}) \\ R_A &= 229\text{K} \quad (220\text{K}) \\ C_B &= C_4 = 133\text{nF} \quad (100\text{nF} \| 33\text{nF}) \end{aligned} \tag{8.5.33}$$

where the standard values used in the actual circuit prototype are shown in parentheses.

Finally, the dc gain of the biquadratic section can be made to be unity with a slight modification. For large signal considerations, it is necessary for the dc gain to be large enough that the output is able swing over the full range required by the modulator, and was chosen to be unity for simplicity. The dc gain of the biquadratic section in the present configuration can be expressed

$$A_0 = \left(\frac{\omega_z}{\omega_p}\right)^2 \tag{8.5.34}$$

The dc gain of the biquadratic section can be increased by a factor λ, simply by attenuating the feedback signal by this same amount, as depicted below in the block diagram in figure 8.17.

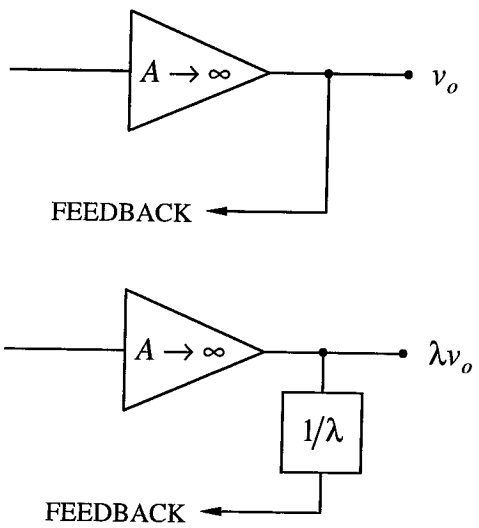


Figure 8.17: The gain of an ideal feedback amplifier is increased by a factor λ, simply by attenuating the feedback signal by this same factor.

The complete circuit diagram reflecting this modification is shown in figure 8.18. To make the dc gain of the biquadratic section unity, set

$$\frac{R_7}{R_6 + R_7} = (\frac{\omega_z}{\omega_p})^2 \tag{8.5.35}$$

For the present design, we can choose $R_7 = 1\text{K}$ and $R_6 = 24\text{K}$ to achieve the desired dc gain. As a final note, in order not to exceed the common-mode range of the op-amp inputs, the reference voltage is used as a floating ground point for the biquadratic section. This eliminates the need for either dual power supplies or op-amp sensing near ground, thereby allowing use of an ordinary inexpensive quad op-amp to implement the entire optimal voltage feedback amplifier.

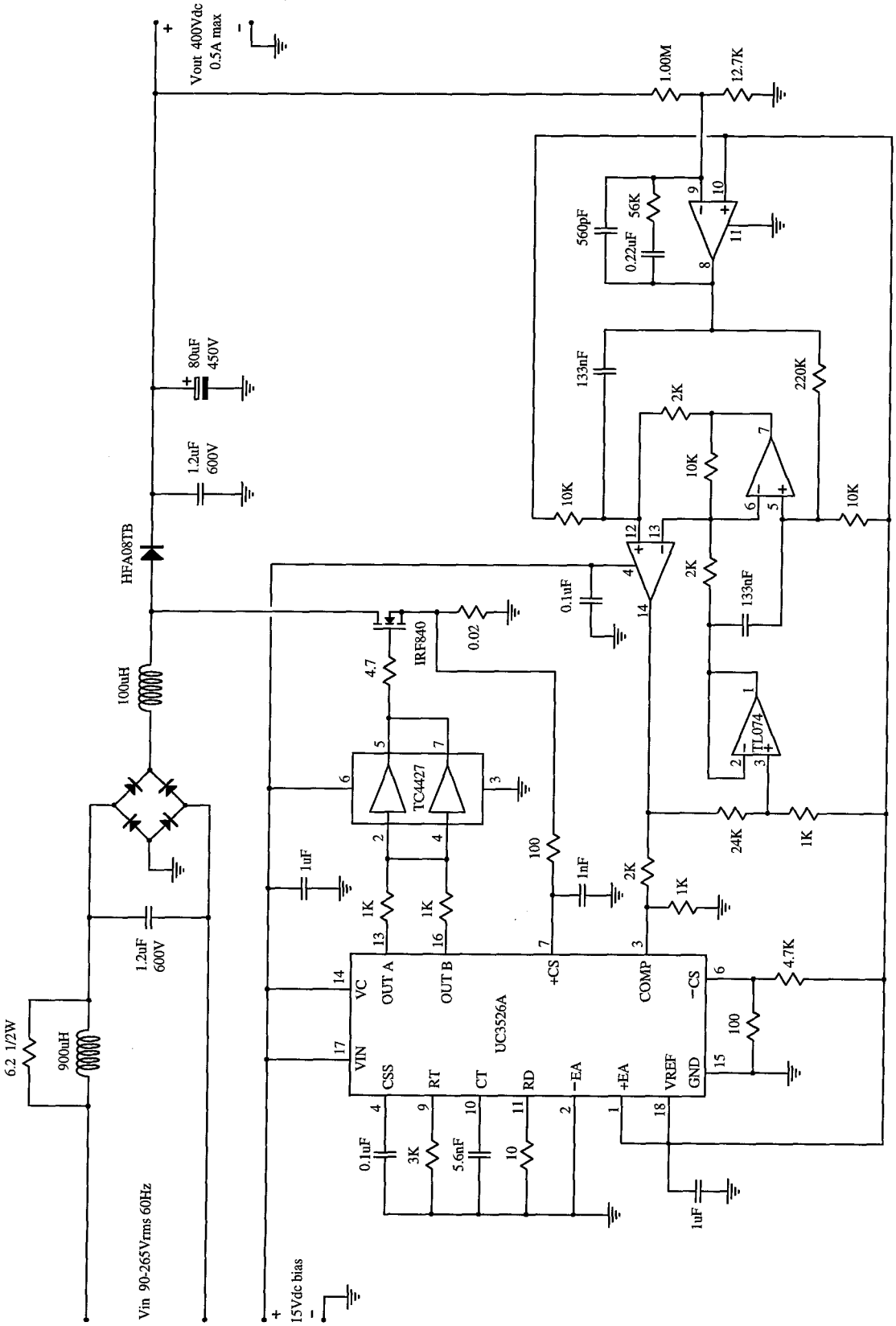


Figure 8.18: Complete schematic diagram of the 200W prototype optimal voltage feedback dcm boost rectifier.

8.5.3 Experimental Results

Experimental waveforms for the prototype rectifier are shown in figures 8.19 and 8.20. As demonstrated in figure 8.19, at full power, the observed current waveshape is excellent under both high line and low line conditions. At reduced power levels, the current waveshape degrades somewhat under high line conditions, but actually improves under low line conditions. This happens because the reduction in load causes the feedback to tend towards the optimal value under low line conditions, but away from the optimal value under high line conditions. Nevertheless, the waveshape is excellent under any combination of line and load.

Figure 8.20 shows the response to a step load change, switched from 10% to 100% of the maximum load power of 200W. The transient response is good inherently, owing to optimal voltage feedback. At high line, the output voltage overshoot is only about 10V, and the output recovers from this drastic load change in only a few line cycles. At low line, because the loop gain is lower, the output voltage overshoot is about 40V, or about 10% of the dc output voltage. If this is unacceptable, it is easily reduced by increasing the value of the output capacitor. The overshoot is approximately inversely proportional to the capacitor value, so doubling the size of the output capacitor cuts the overshoot approximately in half. Note, however, that changing this capacitor value requires redesign of the optimal voltage feedback amplifier, since the output voltage ripple amplitude is also approximately inversely proportional to the value of this capacitor.

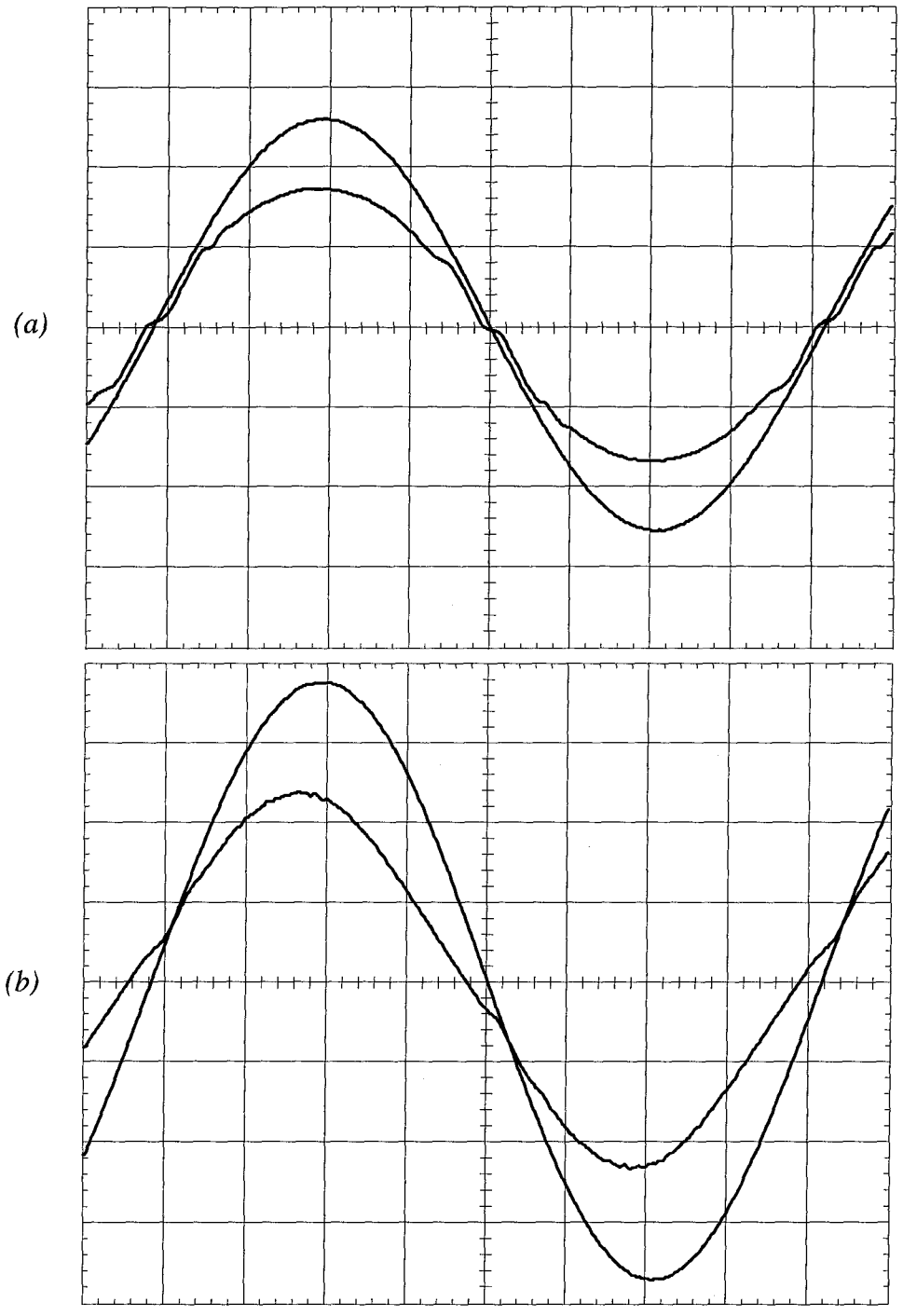


Figure 8.19: Measured input voltage and current waveforms at full power (200W) for the prototype optimal voltage feedback dcm boost rectifier. (a) 90Vrms input (larger waveform) @ 50V/div., input current (smaller waveform) @ 2A/div., (b) 265Vrms input (larger waveform) @ 100V/div., input current (smaller waveform) @ 0.5A/div.. Horizontal: 2ms/div..

(a)

(b)

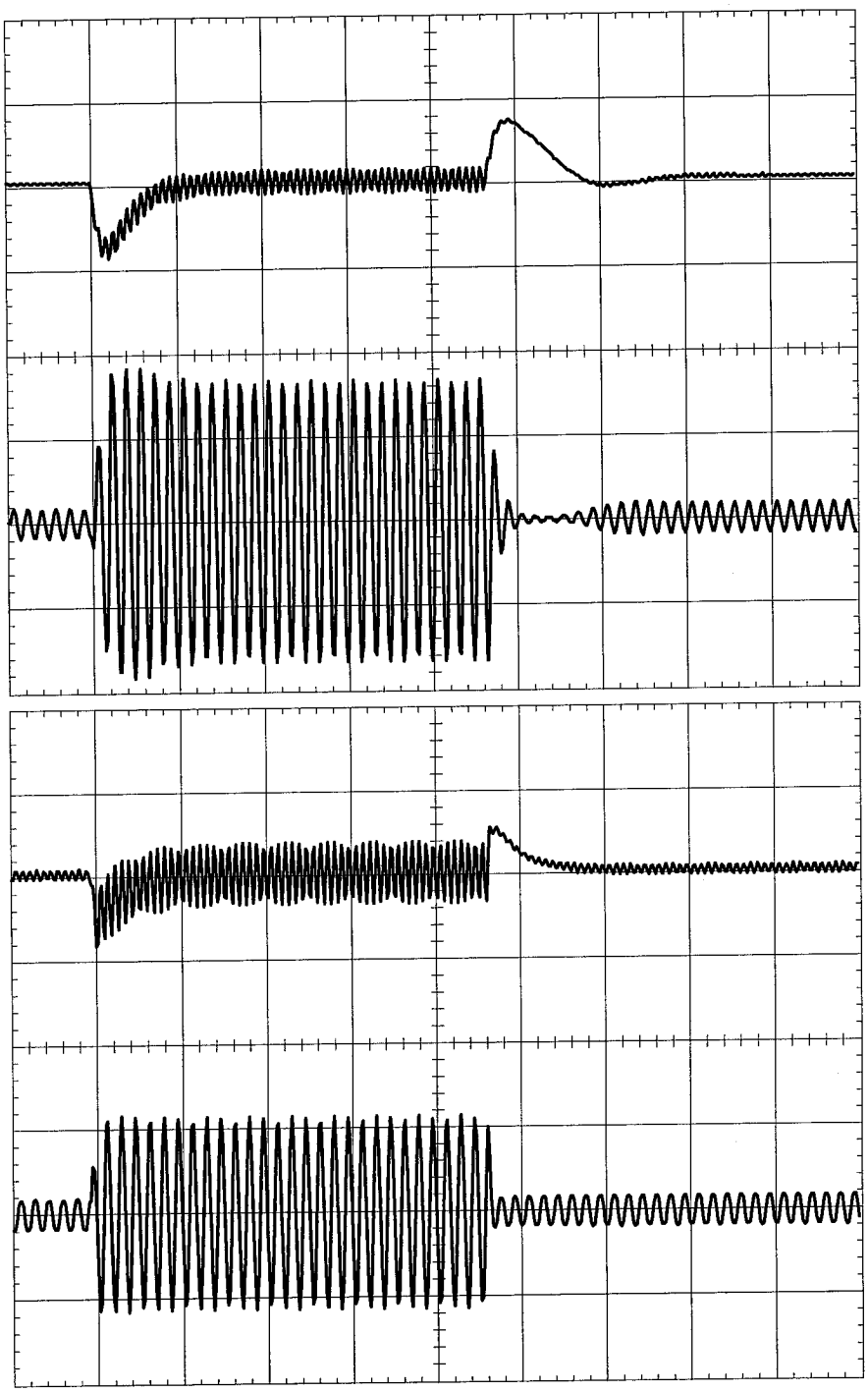


Figure 8.20: Step load response: 10%→100%→10%. (a) with 90Vrms input voltage; top trace: output voltage @ 50V/div.; bottom trace: input current @ 2A/div., (b) with 265Vrms input voltage; top trace: output voltage @ 20V/div.; bottom trace: input current @ 1A/div.. Horizontal: 100ms/div..

Chapter 9

Conclusion

The ac/dc rectification problem surrounds us. Virtually all of the electronic devices in any home or office operating from the ac utility line require a rectifier circuit to convert the ac utility line voltage to one or more usable dc voltages. In the rectification process, some level of input current distortion is inevitably generated. The primary objective of this thesis has been to provide a framework by which the performance of these ac/dc rectifier circuits can be analyzed and assessed. The secondary objective has been to provide useful results and examples, that may be used for the purpose of design.

The power factor is a figure of merit describing the effectiveness with which an ac power source transfers power to a load. For the specific case of sinusoidal ac source voltage, the power factor can be broken into the product of two components: the distortion factor, indicative of the current harmonics present in the input circuit, and the displacement factor, indicative of the phase displacement of the fundamental component of the input current relative to the input voltage. The ideal case occurs when both of these factors are unity, thereby making the input current the smallest current, in the rms sense, for a given load power.

The performance of a rectifier circuit can be assessed relative to a fictional device called the ideal rectifier. The ideal rectifier draws power from the sinusoidal input voltage source with unity input power factor, and is also lossless. The lossless property implies that the input and output power are, on average, equal. The rms input current to the ideal rectifier, called the "ideal current" is given by the ratio of the output power to the rms input voltage. The performance of rectifier circuits can, in general, be assessed relative to this idealization.

Passive rectifier circuits can provide high input power factor, even approaching unity as a limiting case for the resonant filter. In the analysis of the passive rectifier circuits in this thesis, it was assumed that the rectifier circuit was to be followed by a high performance switching post-regulator. The loading effect of this post-regulator can be modeled as a constant power load, and some limitations are brought out in the analysis under this assumption. For example, it was shown that both the capacitor filter and the line-side inductor filter are power limited, each having a boundary beyond which they can no longer operate properly.

The capacitor filter was shown to exhibit poor performance under any operating condition, and may be dismissed for use in high power factor applications. Acceptable performance for many applications can be achieved with either of the inductor filters described, and the analysis in this thesis provides a means for selecting an inductor given a required performance level. For operation in the discontinuous conduction mode, for a given inductor size, the performance of the inductor filters is nearly the same as that of the resonant filter, giving the advantage to the inductor filters which do not require the resonant capacitor. This renders the resonant filter little more than an analytical novelty, except perhaps when used in conjunction with a high-frequency ac buss, where operation in the continuous conduction mode is achieved with an inductor of reasonable size.

If the rectifier circuit must provide the load with constant power, then it must store energy internally. If, in addition, the rectifier circuit operates with unity input power factor, then the energy stored in the rectifier circuit is determined to within a constant. If all energy storage in the rectifier circuit occurs in a single linear reactive element, then the terminal voltage and current for that element are determined. This is often approximately true in the case in actual rectifier circuits.

For pwm converter analysis, the pwm switch method confines the nonlinear behavior inherent in pwm switching to the switches themselves. Several new pwm switch models were presented in this thesis, and each model was derived based on the averaging of the switch waveforms. For each switch, its average behavior is modeled by a dependent generator, which is easily inserted into the converter circuit in place of the actual

transistor and diode switches, terminal-by-terminal, to create a complete average circuit model. Separate models were derived for operation in either the continuous or discontinuous conduction modes. In the continuous conduction mode, the effect of parasitic resistive elements were accounted for by a simple adjustment of the switch model, easily derived by inspection.

A pwm converter in an ac/dc rectifier circuit can operate in ccm, dcm, or both, all in the same line cycle. It is usually desired to maintain only one operating mode, because the nature of the control characteristics of the switches change as the border between modes is crossed. Operation exclusive to one operating mode over the entire line period is indeed possible, and can be verified by compliance with an inequality.

The dcm boost converter has several advantages over other converters that make it useful in rectifier circuits operating in the low-to-medium power range. Its partial power processing property, combined with the alleviation of losses associated with the reverse-recovery of the rectifier diode make it extremely efficient. However, the dcm boost rectifier is not an ideal automatic current shaper, and thus distorts the input current waveform when operated with constant duty ratio. This distortion can be corrected in an open-loop manner, by appropriately adjusting the duty ratio over the line period, and a circuit to provide this correction was presented. Implementation requires two analog multipliers, which may be undesirable due to cost.

Another method of improving the input current waveshape of the dcm boost rectifier is using optimal voltage feedback. Optimal voltage feedback provides another desirable feature inherently, namely that of good output voltage transient response. It requires a specially designed filter, to feed back the output voltage ripple with the appropriate magnitude and phase to achieve optimality. Optimality is achieved when the input power factor is maximum. This method does not provide optimum performance under all operating conditions, so the feedback can be designed so that optimality is achieved under the worst-case condition—high line and maximum load. Acceptable performance over the entire operating range is then possible.

Conceptually, the ac/dc rectification problem is a simple one. However, its solution is complex, and no one solution is appropriate for all applications. Given a design

problem, the methods developed here will hopefully assist in the determination of the best solution, or even be used in the analysis and development of new rectifier circuits and topologies.

Appendix A

Periodic Extensions

A problem which frequently arises in the analysis of power factor and harmonics in single-phase rectifier circuits is that of finding the Fourier coefficients of the *alternating periodic extension* of a function. In these circuits, the "unfolding" of the current waveform through the bridge rectifier creates an alternating periodic waveform of this type. In this section, the computation of the Fourier coefficients for this type of waveform is discussed, as well as a review of the more familiar concepts of odd and even periodic extensions.

A.1 Even Periodic Extension

Consider a function $f(\theta)$ defined on the interval $0 \le \theta \le \pi$. The graph of the *even extension* is the reflection of the graph $y = f(\theta)$ about the y axis. The graph of the *even periodic extension* is constructed by repeating the graph of both the function f and its even extension every 2π units along the θ axis, as shown in figure A.1(a). Hence, the even periodic extension is defined by the equations

$$F_e(\theta) = f(\theta) \;\; ; \;\; 0 \le \theta \le \pi$$

and, (A.1.1)

$$\left.\begin{aligned} F_e(-\theta) &= F_e(\theta) \\ F_e(\theta + 2\pi) &= F_e(\theta) \end{aligned}\right\} \text{ for all } \theta$$

Using the results of section 2.1, the Fourier coefficients of the even periodic extension $F_e(\theta)$ can be computed using the general formulas (2.1.15), which give

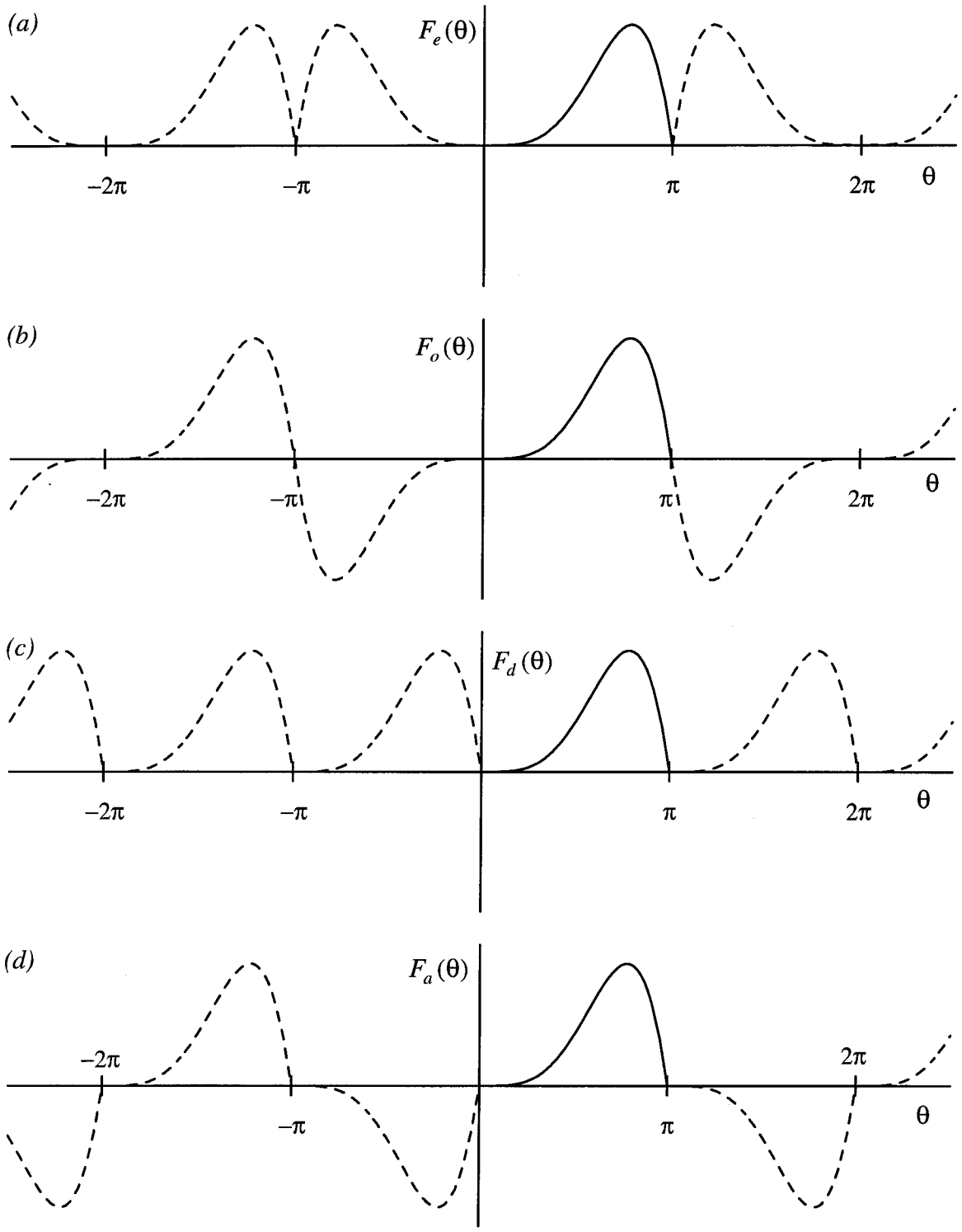


Figure A.1: The function $f(\theta)$ (solid), and the periodic extensions (dashed): (a) the even periodic extension $F_e(\theta)$, (b) the odd periodic extension $F_o(\theta)$, (c) the direct periodic extension $F_d(\theta)$, and (d) the alternating periodic extension $F_a(\theta)$.

$$F_{e0} = \frac{1}{2\pi}\int_{-\pi}^{\pi} F_e(\theta)\, d\theta$$

$$\left.\begin{aligned} a_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} F_e(\theta)\cos n\theta\, d\theta \\ b_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} F_e(\theta)\sin n\theta\, d\theta \end{aligned}\right\} \; n = 1,2,3,\ldots \qquad \text{(A.1.2)}$$

However, these computations may be simplified as follows: First, consider the dc term. The integrand is an even function, and the limits of integration are symmetric with respect to the origin. Interpreting the integral as an area, we can visualize that the area to either side of the vertical axis is the same. The integral can therefore be written as twice the original integral, but with the limits of integration taken from 0 to π. Next, consider the a_n coefficients. For any n, the integrand is the product of two even functions, and is therefore itself an even function. Again, using the area interpretation, this integral may also be written as twice the original integral, with the limits of integration taken from 0 to π. Finally, for the b_n coefficients, the integrand is the product of an even function and an odd function, and is therefore itself an odd function. In this case, the oddness makes the integral zero, and all of the b_n coefficients are therefore zero. Thus, for the even periodic extension $F_e(\theta)$, the Fourier coefficients can be written in terms of the function $f(\theta)$ as

$$F_{e0} = \frac{1}{\pi}\int_{0}^{\pi} f(\theta)\, d\theta$$

$$\left.\begin{aligned} a_n &= \frac{2}{\pi}\int_{0}^{\pi} f(\theta)\cos n\theta\, d\theta \\ b_n &= 0 \end{aligned}\right\} \; n = 1,2,3,\ldots \qquad \text{(A.1.3)}$$

Since the b_n coefficients are all zero, the Fourier series expansion of the even periodic extension is then simply

$$F_e(\theta) = F_{e0} + \sum_{n=1}^{\infty} a_n \cos n\theta \qquad \text{(A.1.4)}$$

sometimes called the Fourier cosine series expansion of the function $f(\theta)$. The Fourier series expansion of the even periodic extension thus contains a dc term and cosine terms only, and no sine terms. The harmonics, however, may be both odd and even.

A.2 Odd Periodic Extension

Consider the function $f(\theta)$ defined on the open interval $0 < \theta < \pi$. The graph of the *odd extension* is the reflection of the graph $y = f(\theta)$ across the diagonal $y = -\theta$. The graph of the *odd periodic extension* is constructed by repeating the graph of both the function f and its odd extension every 2π units along the θ axis, as shown in the example of figure A.1(b). The odd periodic extension is thus defined by the equations

$$\begin{aligned} &F_o(\theta) = f(\theta) \;\; ; \;\; 0 < \theta < \pi \\ &F_o(0) = F_o(\pi) = 0 \\ &\qquad \text{and,} \\ &\left.\begin{aligned} F_o(-\theta) &= -F_o(\theta) \\ F_o(\theta + 2\pi) &= F_o(\theta) \end{aligned}\right\} \text{ for all } \theta \end{aligned} \qquad \text{(A.2.1)}$$

At the points $\theta = 0$ and $\theta = \pi$, the odd periodic extension is assigned the value zero. As far as the computation of the Fourier coefficients is concerned, this choice is somewhat arbitrary, since the value of the function at any finite number of points cannot change the value of the integrals used to compute the coefficients. However, it can be shown that the Fourier series expansion of the odd periodic extension converges to zero at these points. Moreover, it can be shown that the Fourier series of a piecewise smooth function $f(\theta)$ of period 2π, converges to the value $f(\theta)$ at every point of continuity, and to the value

$$\frac{1}{2}\left[f(\theta_0^-) + f(\theta_0^+)\right] \qquad \text{(A.2.2)}$$

at every point of discontinuity $\theta = \theta_0$ [8]. Proof of this result is, however, beyond the scope of this presentation.

Using arguments similar to those for the even periodic extension, the Fourier coefficients of the odd periodic extension may be written

$$\left.\begin{aligned} F_{o0} &= 0 \\ a_n &= 0 \\ b_n &= \frac{2}{\pi}\int_0^{\pi} f(\theta)\sin n\theta \, d\theta \end{aligned}\right\} \; n = 1,2,3,\ldots \tag{A.2.3}$$

Since the dc term and the a_n coefficients are all zero, the Fourier series expansion of the odd periodic extension is then

$$F_o(\theta) = \sum_{n=1}^{\infty} b_n \sin n\theta \tag{A.2.4}$$

sometimes called the Fourier sine series expansion of the function $f(\theta)$. The odd periodic extension thus contains only sine terms, with no dc term nor cosine terms. The harmonics may be both odd and even.

A.3 Direct Periodic Extension

Again consider a function $f(\theta)$ defined on the open interval $0 < \theta < \pi$. The graph of the *direct extension* is formed by shifting the graph of the function $f(\theta)$ backward π units along the θ axis. The graph of the *direct periodic extension* is constructed by repeating the graph of the function $f(\theta)$ and the direct extension every 2π units along the entire θ axis, as shown in the example of figure A.1(c). The direct periodic extension is defined by the equations

$$\begin{aligned} &F_d(\theta) = f(\theta) \;\; ; \;\; 0 < \theta < \pi \\ &F_d(0) = F_d(\pi) = \frac{1}{2}\left[f(0^+) + f(\pi^-)\right] \\ &\qquad \text{and,} \\ &\left.\begin{aligned} F_d(\theta) &= F_d(\theta + \pi) \\ F_d(\theta) &= F_d(\theta + 2\pi) \end{aligned}\right\} \text{ for all } \theta \end{aligned} \tag{A.3.1}$$

In ac/dc rectifier applications, this type of waveform is often encountered on the dc (direct current) side of the bridge rectifier, and is therefore given the name "direct periodic extension." The Fourier coefficients of the direct periodic extension can then be expressed in terms of the function $f(\theta)$ as

$$F_{d0} = \frac{1}{\pi}\int_0^{\pi} f(\theta)\, d\theta$$

$$a_n = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_0^{\pi} f(\theta)\cos n\theta\, d\theta \;;\; n \text{ even} \\ 0 \;;\; n \text{ odd} \end{cases} \qquad \text{(A.3.2)}$$

$$b_n = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_0^{\pi} f(\theta)\sin n\theta\, d\theta \;;\; n \text{ even} \\ 0 \;;\; n \text{ odd} \end{cases}$$

The Fourier series expansion of the direct periodic extension can therefore be written

$$F_d(\theta) = F_{d0} + \sum_{n=2,4,6,..} a_n \cos n\theta + b_n \sin n\theta \qquad \text{(A.3.3)}$$

While it appears that the Fourier series expansion contains only even harmonics, this is somewhat artificial, because the expansion was based on a function of period 2π, rather than the actual period of this function which is only π. Nevertheless, it may be desirable to express the Fourier series expansion in this form, since the harmonics are referenced to the fundamental period of 2π, which, in the case of ac/dc rectifier circuits, is the normalized line period. Thus, in these circuits, the Fourier series expansion of the direct periodic extension of any waveform contains only even harmonics of the line frequency. This formulation provides an interesting comparison to the alternating periodic extension of the next section, which is shown to contain only odd harmonics of the line frequency.

A.4 Alternating Periodic Extension

Again consider the function $f(\theta)$ defined on the open interval $0<\theta<\pi$. The graph of the *alternate extension* is formed by sliding the graph of the function $f(\theta)$ backward π units, and then reflecting the graph about the θ axis. The graph of the alternating periodic extension is constructed by repeating the graph of both the function $f(\theta)$ and the alternate extension every 2π units along the θ axis, as shown in figure A.1(d). The alternating periodic extension is thus defined by the equations

$$\begin{aligned} &F_a(\theta) = f(\theta) \;\; ; \;\; 0<\theta<\pi \\ &F_a(0) = -F_a(\pi) = \frac{1}{2}\left[f(0^+) - f(\pi^-)\right] \\ &\qquad \text{and,} \\ &\left.\begin{aligned} F_a(\theta) &= -F_a(\theta+\pi) \\ F_a(\theta) &= F_a(\theta+2\pi) \end{aligned}\right\} \text{ for all } \theta \end{aligned} \tag{A.4.1}$$

The Fourier coefficients of the alternating periodic extension can then be written in terms of the function $f(\theta)$ as

$$\begin{aligned} &F_{a0} = 0 \\ &a_n = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_0^{\pi} f(\theta)\cos n\theta \, d\theta \;\; ; \;\; n \text{ odd} \\ 0 \;\; ; \;\; n \text{ even} \end{cases} \\ &b_n = \begin{cases} \dfrac{2}{\pi}\displaystyle\int_0^{\pi} f(\theta)\sin n\theta \, d\theta \;\; ; \;\; n \text{ odd} \\ 0 \;\; ; \;\; n \text{ even} \end{cases} \end{aligned} \tag{A.4.2}$$

The Fourier series expansion of the alternating periodic extension thus contains only odd harmonics, with both sine and cosine terms, and no dc term. The expansion can therefore be written as the sum of odd harmonics only

$$F_a(\theta) = \sum_{n=1,3,5...} a_n \cos n\theta + b_n \sin n\theta \qquad \text{(A.4.3)}$$

where the Fourier coefficients are given by the formulas (A.4.2).

A.5 Phase-Shifted Alternating Periodic Extension

Suppose that the function $f(\theta)$ is again defined on an open interval of length π, but in this case the interval begins at some angle θ_1, and ends at another angle $\pi + \theta_1$. The graph of the *alternate extension* is again formed by sliding the graph of $f(\theta)$ backward by π units, and then reflecting the graph about the θ axis. The graph of the *alternating periodic extension* is then constructed by repeating the graphs of the function $f(\theta)$ and the alternate extension every 2π units along the θ axis, as shown in the example of figure A.2. For the phase-shifted (general) case, the alternating periodic extension is defined by the equations

$$\begin{aligned} &F_a(\theta) = f(\theta) \;\; ; \;\; \theta_1 < \theta < \pi + \theta_1 \\ &F_a(\theta_1) = -F_a(\pi + \theta_1) = \frac{1}{2}\left[f(\theta_1^+) - f(\pi + \theta_1^-)\right] \\ &\qquad \text{and,} \\ &\left.\begin{aligned} F_a(\theta) &= -F_a(\theta + \pi) \\ F_a(\theta + 2\pi) &= F_a(\theta) \end{aligned}\right\} \text{ for all } \theta \end{aligned} \qquad \text{(A.5.1)}$$

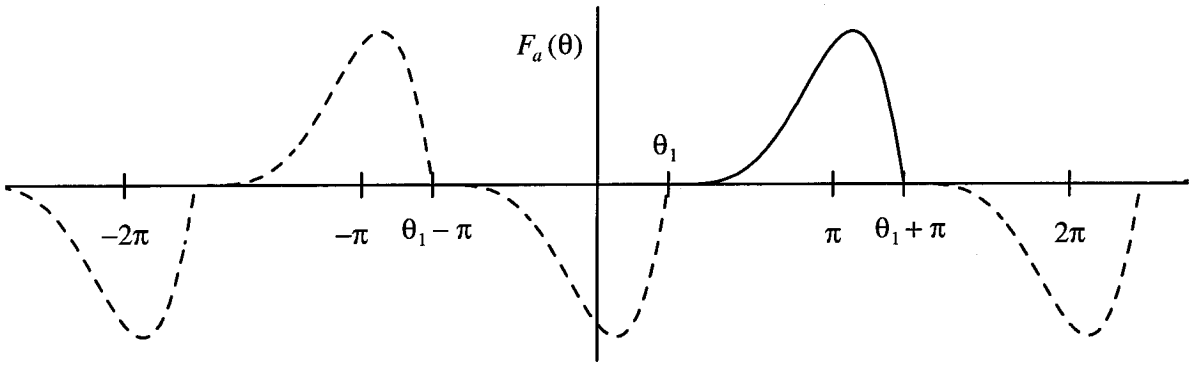


Figure A.2: The function $f(\theta)$, defined on the interval $\theta_1 < \theta < \theta_1 + \pi$ (solid), and its alternating periodic extension (dashed).

For the purpose of illustrating the alternating periodic extension, the waveform of figure 2.4 was conveniently chosen so that there is no jump discontinuity when forming the extension. In general, this is not always the case, yet it makes no difference insofar as computing the Fourier coefficients is concerned, since the value of the function at any finite number of points cannot change the value of its integral. To compute the Fourier coefficients, we start with the general formulas derived in section 2.1. These give

$$\left.\begin{aligned} F_{a0} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} F_a(\theta)\,d\theta \\ a_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} F_a(\theta)\cos n\theta\,d\theta \\ b_n &= \frac{1}{\pi}\int_{-\pi}^{\pi} F_a(\theta)\sin n\theta\,d\theta \end{aligned}\right\} \; n = 1,2,3,\ldots \qquad \text{(A.5.2)}$$

But in each of these expressions, the integrand is periodic with period 2π. Therefore, the interval over which integration takes place may be replaced by any other interval of length 2π. In terms of the original function $f(\theta)$, these integrals can then be written

$$\left.\begin{aligned} F_{a0} &= \frac{1}{2\pi}\int_{\theta_1-\pi}^{\theta_1}\left[-f(\theta+\pi)\right]d\theta + \frac{1}{2\pi}\int_{\theta_1}^{\theta_1+\pi} f(\theta)\,d\theta \\ a_n &= \frac{1}{\pi}\int_{\theta_1-\pi}^{\theta_1}\left[-f(\theta+\pi)\right]\cos n\theta\,d\theta + \frac{1}{\pi}\int_{\theta_1}^{\theta_1+\pi} f(\theta)\cos n\theta\,d\theta \\ b_n &= \frac{1}{\pi}\int_{\theta_1-\pi}^{\theta_1}\left[-f(\theta+\pi)\right]\sin n\theta\,d\theta + \frac{1}{\pi}\int_{\theta_1}^{\theta_1+\pi} f(\theta)\sin n\theta\,d\theta \end{aligned}\right\} \; n = 1,2,3,\ldots \qquad \text{(A.5.3)}$$

Substituting the variable $\theta' = \theta + \pi$ into the leftmost integral in each equation, we find that the Fourier coefficients of the phase-shifted alternating periodic extension may be written simply as

$$F_{a0} = 0$$

$$a_n = \begin{cases} \dfrac{2}{\pi} \displaystyle\int_{\theta_1}^{\theta_1+\pi} f(\theta) \cos n\theta \, d\theta \ ; \ n \text{ odd} \\ 0 \ ; \ n \text{ even} \end{cases} \tag{A.5.4}$$

$$b_n = \begin{cases} \dfrac{2}{\pi} \displaystyle\int_{\theta_1}^{\theta_1+\pi} f(\theta) \sin n\theta \, d\theta \ ; \ n \text{ odd} \\ 0 \ ; \ n \text{ even} \end{cases}$$

which are the same as the formulas found for the Fourier coefficients of the alternating periodic extension without phase-shift, except the limits of integration are changed. As one might expect, the alternating periodic extension contains only odd harmonics, regardless of the phase-shift, and no dc component.

Summarizing the results of this appendix, we found the following: (1) The Fourier series expansion of the even periodic extension contains a dc term and cosine terms only, (2) the Fourier series expansion of the odd periodic extension contains sine terms only, (3) the Fourier series expansion of the direct periodic extension contains a dc term and even harmonics only, and (4) the Fourier series expansion of the alternating periodic extension contains odd harmonics only.

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