

Towards Sustainable, Scalable, Low-Cost Indium Phosphide Space-Based Solar Power

Thesis by
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ABSTRACT

The world needs clean, sustainable, and consistent sources of power. Solar energy is an attractive source of renewable power, but energy storage is a challenge for intermittent sources like solar and wind. The massive reduction in space launch costs now makes the prospect of space solar power as a 24/7, consistent baseline source of clean power more of a viable possibility than before. Solar cells designed to provide power for Earth while in space must not only be low cost and efficient but also light and maintain their performance in harsh space environments, especially in extreme temperature conditions while being subject to damaging space radiation.

This thesis explores two different approaches to achieving radiation hardness: using nanowire solar cells instead of planar cells and using thin-film diffusion-doped cells. It does so with cells made of indium phosphide (InP), which is inherently more resilient to damage from space radiation than materials like silicon (Si) and gallium arsenide (GaAs). The performance of diffusion-doped planar cells is compared to epitaxially-grown solar cells as a baseline.

Nanowire cells were simulated in Lumerical to understand the light-trapping properties compared to planar cells with and without surface texturing that also enhances light absorption. The nanowires were simulated with and without hemispherical nanoparticles to enhance light absorption while maintaining a transparent conducting top layer to adequately transport the generated electricity. Nanowire and planar cells were further simulated in Sentaurus to predict their electrical performance. Nanowire fabrication was attempted as well, but reliable, consistent fabrication was challenging. Given the cost and scalability challenges of this approach, the rest of the work pivots to planar cells.

Epitaxially-grown InP cells optimized using Sentaurus were fabricated as a baseline and to work out fabrication challenges adjacent to the p-n junction formation itself. Then, diffusion-doped InP cells were fabricated using Cd_3P_2 and Zn_3P_2 as p-type dopants on undoped InP substrates. Preliminary cell performance optimization was conducted by adjusting diffusion temperatures and times as well as thinning the emitter layer. Efficiencies of up to 4.94% were achieved in Cd-doped cells and up to 3.85% were achieved in Zn-doped cells without anti-reflection coatings, with a maximum J_{SC} of 11.33 mA/cm^2 and a maximum V_{OC} of 778.1 mV in 100 nm thinned Zn-doped cells.

PUBLISHED CONTENT AND CONTRIBUTIONS

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S.A. simulated the nanowire, planar, and pyramidally-structured cells, presented the results in the plots and graphs, and wrote the manuscript.
- [2] Sara Anjum, Philip R. Jahelka, and Harry A. Atwater. Diffusion-Doped InP Solar Cells for Ultralight Space Power Applications. In *2024 IEEE 52nd Photovoltaic Specialist Conference (PVSC)*, pages 1713–1715, 2024. doi: 10.1109/PVSC57443.2024.10749655.
S.A. fabricated the cadmium diffusion-doped cells reported in this paper, measured the current-voltage and quantum efficiency characteristics of the cells, graphed the data, and wrote the manuscript.
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Chapter 1

LOW-COST SPACE-BASED SOLAR POWER (SBSP)

1.1 Principles of SBSP

The world's ever-increasing energy demands require clean, sustainable, and consistent sources of power to maintain and promote the development and well-being of societies around the globe. As of 2023, the world consumed over 27,000 TWh of electricity [130], while the world's renewable energy capacity as of 2023 is over 3.8 TW [58]. This represents only 43% of global installed power capacity, and falls far short of the 11 TW goal set at the COP28 to keep the world from warming more than 1.5°C [58].

Solar energy is an attractive renewable power source — with around 1.367 kW/m² reaching Earth outside of its atmosphere [62] and 1 kW/m² reaching Earth's surface [114], the world's energy demand in 2023 could be powered by solar panels covering around 3.73% of the US land mass [1] [130]. However, solar power struggles with intermittency because it only shines for part of the day, prohibiting round-the-clock energy generation on Earth. Worse, energy demand tends to peak in the late afternoon or early evening, so energy generation and energy usage do not align sufficiently [46]. Addressing this challenge necessitates either a way to generate solar power around the clock or adequate energy storage for nighttime use. Different forms of energy storage come with a variety of challenges to address, however. For instance, the most widely-used grid storage, pumped-storage hydropower, can only be done in certain locations [53]. Grid-scale battery storage has location flexibility, but is still costly due to lithium prices, while technologies such as compressed air and gravity storage play a smaller role, and hydrogen is still an emerging technology [53]. Bypassing the need for storage altogether by relying on 24/7 solar energy generation is an attractive prospect in light of these challenges.

SBSP, which involves launching an array of solar cells into orbit around the Sun and wirelessly transmitting that power down to Earth, would have several benefits. It would allow the solar panels to directly face the Sun and generate power at potentially any hour of the day as if it were noon. As an added bonus, it would also allow solar cells to harness energy from the Sun's AM0 spectrum, which reflects the spectrum outside of Earth's surface unattenuated by absorption from Earth's atmosphere. This

means the solar cells will receive a higher power density of 1.37 kW/m^2 in space compared to 1 kW/m^2 on Earth, meaning that all else equal, solar cells can generate more power in space than on Earth [25]. Below is a figure illustrating the difference between the AM0 and the AM1.5 Global spectrum, which accounts for all direct light hitting the solar cell as well as the diffuse light shining on and scattering from the atmosphere [104].

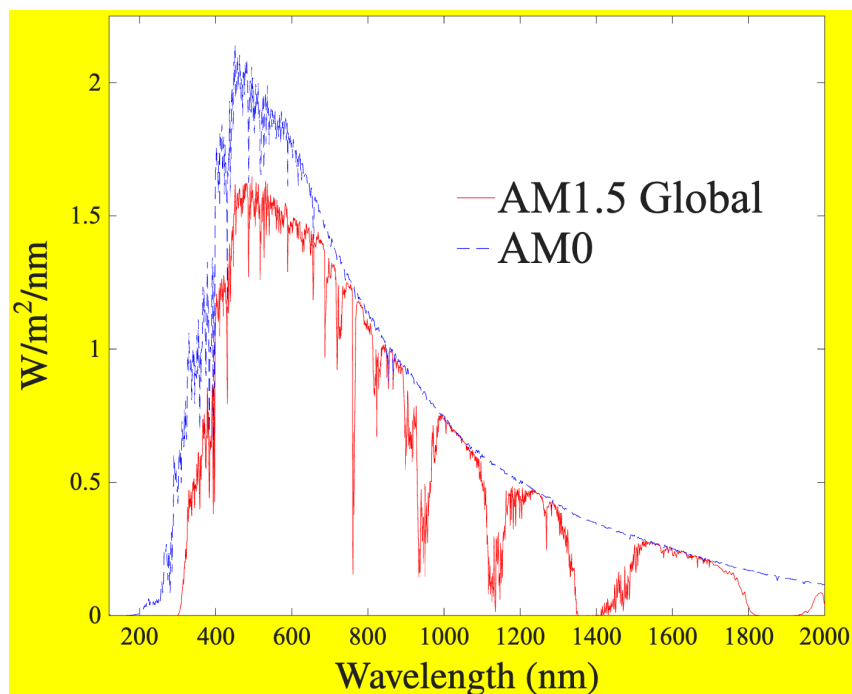


Figure 1.1: AM0 spectrum vs. AM1.5 Global spectrum.

The bumpiness of the AM1.5 Global spectrum is due to the atmospheric absorption, particularly at wavelengths longer than 900 nm. Wavelengths shorter than $1 \mu\text{m}$ are the most relevant to the solar cells investigated in this work. The spectrum illustrates that a noticeable bit more of light at wavelengths between 300 nm and 800 nm should be captured in space compared to on Earth.

1.2 Lightweight Solar Panels for SBSP

Since the launch cost is one of the most important levers controlling the levelized cost of electricity, and the launch cost depends heavily on weight — the lowest launch costs today are $\$1500 / \text{kg}$ — the weight of the solar panels being launched into space greatly affects the cost per W [111]. Worse, solar cells for space require heavy radiation shielding in order for them to even last 10-15 years, in contrast with terrestrial solar cells that do not require such radiation shielding because of

the protection from the atmosphere and last 20-30 years. For all of these reasons, designs for solar cells for space need to address a metric called **specific power**, which is the power per unit mass. Currently, solar cells in space have a specific power of 200 W/kg, weigh 2.1 kg / m², and cost \$10,000 / m² to manufacture, yielding a manufacturing cost of \$36 million and a launch cost of over \$11 million for a 60m x 60m solar panel [137] [111]. For space solar cells, only 15% of the areal density comes from the energy-generating layers of the panel [76]. If the need for radiation shielding can be reduced or eliminated, this would reduce the areal density to ~ 0.32 kg/m², which yields a specific power of ~ 1300 W/kg [137]. This means it is possible to generate over 6x the amount of solar power for a given launch weight allowance.

Increasing Specific Power of Solar Cells

There are several ways to increase the specific power of solar cells. These include [76]:

- **Relying on intrinsically radiation-hard materials;**
- **Using structures like nanowires (NWs) with greater radiation tolerance;**
- Reducing the absorber thickness and potentially compensating with nanophotonic absorbers.
- Using concentrator photovoltaics

This thesis will investigate InP as a choice of a radiation-hard material and using NWs for radiation-hard solar cells.

Here's an endnote.¹

Indium Phosphide (InP) for SBSP

Indium phosphide exhibits superior radiation hardness compared to counterparts such as Si and GaAs [162]. This is in part because hole traps such as H4 have lower energies in *p*-InP ($E_V = +0.37$ eV) than *p*-GaAs ($E_V = +0.79$ eV)[161] [131]. Since these traps are shallower in InP than in GaAs, these defects undergo room-temperature annealing easier in the former than the latter. However, defects such as the HD1 defect, which exhibits deep donor level behavior, are needed to fully explain the performance degradation and annealing behavior observed in InP after electron irradiation at high fluences of $10^{15} - 10^{16}$ cm⁻² [138]. The method of

growing the semiconductor can also make a difference — the work that described the HD1 defect mentioned earlier also found that MOCVD-grown InP exhibits greater resistance to electron radiation than LEC-grown InP because of lower formation of the HD1 defects [138]. This illustrates that the method of semiconductor formation can make the material more or less prone to radiation damage while also illustrating mechanisms, such as thermal annealing, that can mitigate and remove performance-degrading defects. A patented record InP planar solar cell, as of the writing of this thesis, achieved a record efficiency of 24.17% under the AM1.5G spectrum and 21.05% under the AM0 spectrum [153].

The work in this thesis was done on (100) InP. (110) InP wafers also exist, but are rarer. This is particularly relevant for any readers looking to do spalling work, since spalling (100) wafers yields corrugated surfaces while spalling (110) wafers yields flat surfaces [72], which would in turn affect the thickness and morphology of the fabricated solar cells, and even the ability to achieve the desired thinness for the final devices.

Nanowires for Improved Radiation Tolerance

The mechanisms giving rise to greater radiation hardness in NWs compared to planar cells will be described in greater detail in Section 2.1. In short, the more confined dimensions of the NW, particularly in the radial direction, limit the extent to which proton radiation in particular can displace InP atoms from their native crystal structure [27]. This in turn limits radiation-induced performance degradation.

InP NW solar cells have managed to achieve over 16% efficiency but remain under 20% efficiency [108], compared to the record 24.2% efficiency for planar single-junction InP cells [42]. Specific figures of merit will be discussed in greater technical detail later, but at a high level, the performance shortcomings in NW solar cells come largely from losses due to surface quality. Since NWs have a greater surface-area-to-volume ratio than planar surfaces, poor surface quality can degrade device performance significantly. Improving their surfaces is crucial to enhance NW photovoltaic performance to match, and maybe even exceed, the performance of their planar counterparts while benefiting from its radiation hardness properties in space.

Opting for NWs instead of planar structures may not result in less material consumption per se in the fabrication process — fabrication still requires starting with the wafer and the etching process reacts with the material to produce volatile com-

pounds that are difficult and cost-ineffective to recover. However, the presence of less active material in the device further elucidates why NW cells can exhibit greater radiation hardness while maintaining performance. There's less material to damage compared to a planar counterpart of equivalent height.

Thin-Film Solar Cells for Improved Radiation Tolerance

Thin film planar solar cells can also exhibit radiation hardness for similar reasons related to device dimensions restricting the extent of damage possible. Previous work on 10- μm thin film epitaxial solar cells made of GaInP, GaAs, and GaInAs demonstrated an end-of-life (EOL) efficiency that was 88% of its beginning-of-life (BOL) efficiency after an electron fluence of 10^{15} cm^{-2} .

Beyond the expense and scaling difficulty of epitaxial cells, epitaxial lift-off (ELO), which relies on a chemical to dissolve a sacrificial layer grown before the active solar cell layers, is particularly challenging for InP compared to GaAs. This is because it is difficult to find a chemical etchant that will attack a material that lattice-matches well to InP without also attacking the InP itself. One such lattice-matched material is $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ [5]. Etchants such as $\text{FeCl}_3\text{:H}_2\text{O}$ exist, which can selectively etch lattice-matched InAlAs while avoiding InP with a selectivity of over 500:1 for etching InAlAs versus InP. However, the etch rates at close to room temperature are less than $3.5 \mu\text{m} / \text{min}$. This pales in comparison to the etch rates for GaAs liftoff, which involve etching AlAs with HF and has etch rates over $14 \mu\text{m} / \text{min}$ as reported in the literature and industrial etch rates being even higher [158]. This is in part because reacting AlAs and HF yield AsH_3 , which is a gas that can act as an agitator to remove buildup of precipitated ions and circulate fresh etchant to the exposed sacrificial layer surface in order to facilitate rapid etching. FeCl_3 , on the other hand, just forms Fe^{2+} and Cl^- ions upon reacting with the InAlAs due to the redox potentials of the components involved, which means there is no agitator gas formed and the resulting aqueous ions can precipitate in the etched cracks. As a result, etching can slow down or become uneven.

In this thesis, ELO was attempted using FeCl_3 on MOCVD-grown wafers with an InAlAs layer under the active stack. Since the idea for ELO came after the wafers were ordered, the focus was on FeCl_3 as an etchant, which previous research has demonstrated to work on lattice-matched InAlAs with lifted-off samples up to $500 \mu\text{m}$ wide. However, given the desire for simple scalability, the process was tried on solar cells that measured 3 mm on each side, and abandoned when it did not work for

those samples. This is why spalling will be particularly important for future work on InP thin films — the prospects for ELO for InP are much more challenging because of inherent material characteristics such as lattice constants and redox potentials of the relevant sacrificial layers and etchants, and there is only so much that can be done to overcome those. Spalling, a mechanical process, can be somewhat more material-agnostic, although care will be needed in handling brittle InP samples.

1.3 Solar Cell Fabrication Methods

This section details solar cell fabrication processes for different cell types as well as various methods available to fabricate these devices such as MOCVD growth and diffusion doping.

Commercial Solar Cell Fabrication

In discussing commercial fabrication processes and techniques, which often differ from those used in the lab, it should be remembered that vacuum-free processing is preferable when possible without sacrificing too much material quality because vacuum-free systems are *generally* less expensive, both in upfront and maintenance costs, and more scalable. Thus, though some of these materials can, and often are, deposited in vacuum systems in labs, commercially they are deposited using vacuum-free methods that might be unfamiliar to laboratory researchers unfamiliar with commercial environments.

Crystalline Silicon Solar Cells

Commercial solar cells primarily consist of crystalline Si (c-Si) PVs, which make up 95% of the market, and thin-film PVs, which make up 3-5% of the market [124] [125]. Studying the status quo with commercial PV manufacturing can provide a roadmap from which to build for scaling III-V commercialization, particularly InP for the purposes of this thesis. The silicon solar cell manufacturing process is an extensive one that starts at silicon purification and ends with sealing [109]. The p-n junction, the basic unit of a solar cell consisting of a region with positively-charged impurities (p-type) adjacent to a region with negatively-charged impurities (n-type), is formed in silicon solar cells via a process called **diffusion doping** [109]. In this process, wafers are heated to high temperatures along with gaseous doping agents, which deliberately introduce impurities into the surface of the wafer to create the p-n junction [109]. Manufacturers often start with pre-doped Si, usually p-type, that is doped during the melting and ingot-forming process [151]. Then, the wafer is

doped with the opposite doping type to make the p-n junction [91].

CdTe Solar Cell Fabrication

For thin-film cells, CdTe, which is the most common thin-film PV material and makes up around 50% of the market share of thin-film solar cells [41], is typically deposited via a process called **close-space sublimation**, which involves heating the material and the glass substrate to different temperatures so that the material can condense onto the glass [126] [75]. However, First Solar, one of the largest solar manufacturers, uses **vapor transport deposition** instead, which relies on an inert gas to transport the heated material to the substrate [60] [122]. This method can be used to create thin films of materials like CdTe because such materials can sublimate at temperatures below their melting points, as low as $T = 450^{\circ}\text{C}$, which means they can transition from the solid phase directly to the gas phase [96]. In CdTe cells, the p-n junction is formed by a p-type CdTe layer paired with an n-type CdS [110]. CdS is often deposited via **evaporation, sputtering, electrodeposition, or spraying** [86]. Since CdTe and CdS naturally tend towards being p-type and n-type, respectively, it is easier to make the p-n junction just through material deposition than with Si cells, which require diffusion doping.

Thin-Film Si Solar Cell Fabrication

Thin-film Si solar cells make up 20% of the thin-film market [127]. Si's evaporation temperatures are much higher — over $T = 1300^{\circ}\text{C}$ — so methods such as **CVD** or **PECVD** are preferable, in which a compound like SiH_4 is heated to form polycrystalline or amorphous silicon on a substrate [98]. Commercial thin-film Si solar cells are largely amorphous. Polycrystalline Si solar cells require higher-temperature processing [43], and it is more challenging to make Si thin films with high-quality polycrystallinity [84] compared to CIGS or CdTe [163] [20]. Thin-film (amorphous) Si solar cells are deposited via **PECVD** because the plasma enhancement allows for films to be deposited at lower temperatures, which means reduced energy consumption and cost, and the system is not particularly sensitive to the use of plasma. Both forms of CVD involve breaking gaseous SiH_4 into Si and H atoms, after which the Si atoms deposit onto a substrate such as glass, plastic, or metal [164]. Amorphous silicon cells actually have a p-i-n structure because the structure and defects in the material would result in deteriorated performance in a p-n amorphous Si cell [128]. The p- and n-doped layers are formed by introducing

the gases diborane and phosphine, respectively, during the PECVD process [117].

Amorphous thin-film Si cells only have an efficiency of $\sim 12\%$, compared to the over 20-25% efficiency of commercial c-Si solar cells and the 19% efficiency of CdTe and CIGS thin-film solar cells [23]. The higher efficiencies of CdTe and CIGS cells are in part because CdTe and CIGS are direct-bandgap semiconductors [143] [103], which in short leads to more efficient conversion of incoming solar radiation into electricity. It is also because CdTe and CIGS are polycrystalline [81], which means they have lower defect densities, and the defects can be benign or even beneficial [163].

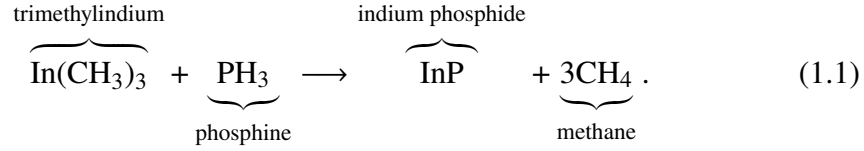
CIGS Solar Cell Fabrication

CIGS solar cells make up 20% of the thin-film market [127]. They are multilayered devices, in which the different layers are deposited via different techniques. First, a conductive sheet is placed on the substrate, and then a layer of molybdenum is deposited via **DC sputtering**, a low-cost metal deposition method [127] [79]. On top of that, p-type CIGS is deposited via **co-evaporation** due to the multiple components in the material. n-type CdS is deposited by **chemical bath deposition (CBD)**, a simple, vacuum-free, cost-effective, and scalable growth method in which a substrate is dipped into a solution and chemical reactions occur on its surface in response [127] [88]. Finally, a protective transparent conducting oxide (TCO) layer, often some form of zinc oxide, is deposited via **sputtering** or **CVD**, depending on a company's particular process optimizations, equipment choice, etc [127].

MOCVD Growth

Metal-organic chemical vapor deposition (MOCVD) involves materials in a gaseous phase chemically reacting at the substrate surface [61]. Metal-organic vapor phase epitaxy (MOVPE) is a subset of MOCVD that focuses on more precise epitaxial growth for highly-ordered crystalline structures [65]. The flowing gases contain the desired atoms needed for the growth layers. For instance, to grow gallium nitride (GaN), the gases trimethyl gallium and ammonia (NH_3) are flown through the system [3]. MOCVD is better than molecular beam epitaxy (MBE) for InP growth because phosphorous deposits on the inside of the MBE chamber, which necessitates time-consuming clean-up, while MOCVD introduces phosphorous via carrier gases like phosphine and the reactions happen at the substrate surface [116]. InP is grown using trimethylindium and phosphine precursors [142]. The chemical

reaction looks like the following:



Trimethylindium and phosphine react to form InP and methane [2]. Though MOCVD does not require the ultra-high vacuum that MBE does (pressures of 10^{-10} - 10^{-12} torr), the system does require pumping out air such that the chamber pressure is in the 10^{-2} — 10^2 torr range [64]. This means that MOCVD-based growth still requires expensive equipment, high-maintenance systems, high energy costs [24], and is limited in scalability due to wafer sizes and quantity capacity. Though 6" InP wafers exist [132], and there exist MOCVD systems that can process up to 24 6" wafers [149], this pales in comparison to the ~ 300 wafers that can be processed at once in a single diffusion doping run for Si [152] or the 0.6m x 1.2m sizes possible for thin-film cells like CdTe cells [17]. Thus, MOCVD growth is currently not suitable for the scalability desired for this endeavor.

Diffusion Doping

Diffusion doping is the most commonly-used commercial method for creating p-n junctions in solar cells. For crystalline silicon cells, industrial production uses the phosphorous source POCl_3 , in conjunction with carrier gases like N_2 and even O_2 , to react with the Si to form phosphor silicate glass (PSG) via intermediary interactions [67] [159]. It is often then followed by a drive-in step, in which the temperature is raised to drive the dopants from this surface PSG layer into the Si itself. During this stage, POCl_3 is eliminated or reduced [159] [106]. This multi-step process allows for better control of the doping profile and achieve a desirable combination of properties. Simply doping at high temperatures can result in an excessively high surface concentration or excessive surface roughness [139].

1.4 Technoeconomic Analysis of SBSP

The cost drivers for SBSP are quite different from those of terrestrial power. Light weight cells are essential for space solar cells in a way that they are not for terrestrial cells. This is not only because of the technical needs in space, where solar cells are floating and orbiting suspended without ground support, but also because launch costs, both for the original power system and the launches needed for its maintenance, dominate the total system cost over its lifetime [111] [83]. For terrestrial cells, on the other hand, the module assembly is the most significant component of the PV

module cost, but module assembly costs only make up $\sim 40\%$ of the total cost, while launch costs can be up to 70% of the total system lifetime costs [97] [83].

Since terrestrial PV does not require ANY launch costs, SBSP must rely on other advantages to compete with terrestrial PV and be cost-competitive. These include the following:

- **Solar irradiance:** 1367 W/m^2 for SBSP, 1000 W/m^2 for terrestrial PV;
- **Hours of solar power generation per day:** 24 hrs for SBSP, 4-7 hrs for terrestrial PV [123];
- **Atmospheric transmission:** 98.8% for SBSP, $< 73\%$ for terrestrial PV [83].

Current technoeconomic analyses (TEA) of space-based solar power conducted by organizations such as NASA paint a grim picture of the affordability of SBSP. NASA's cheapest baseline LCOE for SBSP is 61¢/ kWh as of 2024, compared to $3\text{--}12\text{¢/ kWh}$ for terrestrial renewables in 2023 [111] [57]. NASA does predict, however, that reducing launch costs by 50% and using electric propulsion instead of fuel to transfer the system from LEO to GEO could lower the LCOE to as low as 20¢/ kWh . Varying several other assumptions at once, such as improving solar cell efficiency from 35% to 50% and reducing servicer and debris costs, could reduce the LCOE even further to as low as 3¢/ kWh for a 2 GW system [111]. Meanwhile, Mizrahi et. al., who conducted a TEA for SSP that investigated an ultralight, flexible PV system that could potentially reduce SSP costs without PV efficiency improvements or switching to electric propulsion, predicts a $\sim 110 \text{ MW}$ system with an LCOE of 9.4¢/ kWh [83]. Notably, intermittent renewables like solar require energy storage, which raises their LCOEs. As of 2022, the LCOE of solar power with energy storage was 7.5¢/ kWh [54]. This makes SSPP even more economically compelling as an alternative, especially for niche applications in which access to extensive terrestrial renewable energy with storage is difficult, such as for remote communities and industrial operations, disaster relief and humanitarian aid, and military bases.

The Space Solar Power Project (SSPP) takes the latter approach, focusing on developing flexible, lightweight, deployable structures [83]. The aim is to manufacture cheaper modules, which include the spacecraft, PVs, and wireless power transfer (WPT) units, while also ensuring they remain lightweight. These modules make up the orbiting power station that will be launched into space [83]. SSPP aims to replace

commercially-available III-V triple-junction solar cells, which are fabricated using vacuum-based techniques like MOVPE [167], with InP solar cells made cheaply, scalably, and ultra-light through a combination of diffusion doping and spalling [83]. Spalling, as described before, can produce films that are around $\sim 2\ \mu\text{m}$ thick, potentially yielding radiation-hard cells that can last longer than current cells, while allowing for wafer reuse. These two advantages of spalling, combined with the lower cost and greater scalability of diffusion doping as well as the reduction of other vacuum-processing steps, pave the way for a potentially 17x reduction in PV costs [83].

Moreover, the spalled cells are expected to be 13x lighter than current commercially-available triple-junction cells, which will help increase the number of modules that can be launched in one go by 26x [83]. Since PVs make up 78% of the module's weight, fabricating micron-thick cells is crucial in reducing overall system costs. The weight and structural flexibility limit the number of modules that can fit in a given launch and dictate the launch vehicle needed. When paired with a 14x decrease in per-launch costs by switching from Falcon 9H to Starship as the launch vehicle of choice, launch costs can be reduced from $\sim \$27$ billion to $\$82$ million, a 330x decrease [83]! Additionally, more radiation-hard cells can reduce annualized module replacement costs [83].

For all of these reasons, making cells both lightweight and radiation hard in an affordable, scalable manner are key steps in reducing power station costs and bringing the LCOE of space solar power down to levels that are competitive with terrestrial alternatives.

Beyond cost alone, SBSP provides several other tactical advantages over terrestrial PV that make it attractive for research and development (R&D). These include:

- **Lack of long-term storage need:** While terrestrial PV has an LCOE of $\sim 7.5\text{¢/ kWh}$ with short-duration storage, medium and long-duration storage are not well-developed technologies, but are crucial to providing the grid with consistent baseload power. Without consistent clean baseload power, grids will continue to rely on fossil fuels or nuclear power. SBSP bypasses the energy storage need entirely while still serving as a source of clean baseload power.
- **Potentially greater flexibility for land use:** Because rectennas are 80% transparent meshes, they are potentially well-suited for dual land and water

use with, say, oceans or farms, unlike terrestrial PV which requires large areas of land dedicated specifically to the solar panels. This can reduce the effective terrestrial land footprint of solar power, freeing it up for other uses such as agriculture or housing development.

- **Reduced infrastructure needs for remote regions:** Currently, remote regions rely on diesel generators, natural gas pipelines, or grid extensions, which require extensive transportation and infrastructure. Alternatives such as microgrids also require land-based infrastructure and are susceptible to local energy resource quality. SBSP can help ensure a quality baseload source of power for microgrids.
- **Security and independence:** SBSP can reduce a country's reliance on foreign fossil fuels as its baseload power; improve grid stability against threats from weather, natural disasters, cyberattacks; and provide reliable, independent power to remote military bases.

In short, initial TEAs suggest that, with sufficient technological development, SBSP holds promise in providing a clean source of baseload power that is cost-competitive with terrestrial energy sources, particularly in regions that cannot use sources like geothermal, nuclear, or extensive grid storage. It has even more advantages when non-economic benefits are taken into account.

1.5 Thesis Outline

In Chapter 2, I will discuss the simulation of NW InP solar cells and compare them to planar and pyramidally-textured cells. I will also report on fabrication and characterization attempts. In Chapter 3, I will report on epitaxially-grown InP cells and their characteristics as a baseline for comparison to diffusion-doped cells. Finally, I will report on diffusion-doped InP cells made with two different dopant types.

Chapter 2

NANOWIRES FOR SPACE-BASED SOLAR POWER

2.1 The Advantages of Nanowires in SBSP

Two primary advantages of using NWs for space-based solar cells in particular include greater radiation hardness in space and enhanced light absorption. NW solar cells were found to exhibit less decay in performance efficiency after exposure to space radiation than planar solar cells. On the flip side, the NW structure enhances light absorption within it compared to the planar structure, which can compensate for the fact that there is less of the absorber material present. The following sections will discuss these advantages in greater detail.

Radiation Hardness of Nanowire Solar Cells

Previous studies have shown that NW solar cells have greater radiation hardness than their planar counterparts [28]. This behavior can be explained by the defect formation mechanisms and dynamics that occur when a material structure is exposed to different types of space radiation. High-energy radiation, whether in the form of electromagnetic radiation [63] or particle radiation such as proton and electron radiation [27], can displace atoms from their natural location within the material. This changes the properties of the material and makes it more challenging for it to convert light into electricity. Radiation that makes it all the way through the material produces uniform damage throughout the material, which actually results in a lower performance degradation compared to radiation that does NOT make it all the way through the material, which produces inhomogeneous damage within the material and results in worse performance degradation [27]. Counterintuitively, while electrons cause less damage the further into the material they go, protons cause more damage the further into the material they go [27]. This means that, up to a certain point, lower-energy proton radiation can cause more damage than higher-energy proton radiation [27].

Previous work comparing thin-film planar with NW GaAs solar cells found that the latter could withstand $\sim 40\times$ more radiation than the former [27]. Preliminary work on InP NWs has shown mixed results compared to GaAs NWs — the former hold up much better at particle energies on both the lower end (100 keV protons) and higher end (1 MeV electrons), but do slightly worse than the latter in the middle energy

ranges (350 keV protons) [27]. However, based on previous studies done on planar InP solar cells irradiated with 200 keV proton irradiation, InP NWs hold promise in withstanding radiation damage better than their planar counterparts [112]. Further studies must be done to confirm this, though, for two main reasons:

- **Apples-to-apples comparison:** InP planar and NW solar cells must be measured at the same proton energies and fluences for a true comparison of their degradation under irradiation, and they should be as close to the same height as possible.
- **Need for higher-performance cells:** Interestingly, higher-performance cells undergo greater proportional degradation of their initial performance than lower-performance cells. This is because lower-performance cells already have defects limiting their performance, so the extent to which radiation can further harm device performance is more limited than in higher-performance cells that are freer of defects. The InP NW cells measured earlier had much lower performance than both its InP planar and its GaAs NW counterparts, so InP NW device fabrication must be improved in order to provide a truer degradation comparison with high-performance cells.

The GaAs NW cells measured exhibited much better radiation hardness than the InP planar cells, despite InP being a more radiation-hard material [27] [112]. This hints at the immense potential that the NW geometry has in improving the radiation hardness of solar cells — this geometry has already shown potential in overcoming inherent material limitations with the illustration of GaAs NW solar cells withstanding greater fluences than their InP planar counterparts. However, it is important to note that the InP planar solar cells received a lower proton energy dose than the GaAs NW cells, and as mentioned before, lower proton energy can actually cause more damage [27]. Thus, a comparison between NW GaAs and planar InP cells must occur at the same energies to adequately assess the extent to which the NW geometry can overcome material limitations.

Light Absorption Enhancement in Solar Cells

NWs also enhance light absorption for a given amount of absorber material used. Previous work has shown that tapered NWs can achieve up to 90% broadband absorption across the visible spectrum [37]. NWs that were 1.6 μm tall and contained 108 nm planar equivalence of InP achieved at least 33% absorption improvement

over planar solar cells, if not more, at the wavelengths measured [37]. This is in large part due to the robust coupling into the optical waveguide modes that exist in individual NWs, which have widths in the ~ 100 nm or less range, smaller than the wavelengths of light which are of concern [37]. This results in an optical response that is polarization-independent and angle-insensitive [37].

2.2 Optical Design and Simulation of Nanowire Structures

Ansys Lumerical FDTD and Sentaurus Device were used to design the NW solar cell structures presented in this thesis.

Lumerical Introduction

Lumerical FDTD is a state-of-the-art finite difference time domain (FDTD) software to simulate light interactions with nanostructures. It uses polynomial fitting of experimentally-measured complex refractive indices for each material to interpolate the indices of refraction at intermediate wavelengths and accordingly model light absorption. Meanwhile, Sentaurus Device has sophisticated meshing, comprehensive recombination models, and advanced mobility models. It is also designed for the detailed analysis of defects, traps, and their impact on carrier transport and recombination. This section will focus on the optical design of the NWs, while future sections will introduce the electrical simulations performed in Sentaurus.

NW Optimization Basics in Lumerical

When optimizing the NW structure in Lumerical FDTD, the aim is to optimize light absorption within the InP material, since that is what has the potential to be converted into useful charge carriers for power generation. The figure of merit in question is the maximum short-circuit current (J_{SC}), which accounts for several factors:

- The amount of incoming light available to be absorbed at different wavelengths based on the solar spectrum.
- The fraction of incoming light that is not reflected from or transmitted through the device.
- InP's ability to absorb said incoming light based on its own material properties.

Differences in the second and third points arise from the other materials in the structure, such as metal contacts and anti-reflection coatings (ARCs), that also

absorb and reflect light, as well as any nanophotonic effects from the size and shape of the structures that could impact light absorption, such as the optical waveguide modes mentioned earlier.

The baseline NW structure used was the ITO-enhanced tapered InP structure reported in [145]. Below is a schematic of this cell:

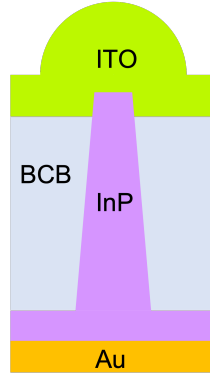


Figure 2.1: Schematic of the ITO-enhanced NW solar cell structure.

ITO is often used as a transparent top contact to improve lateral charge carrier transport at the top of the device without completely blocking sunlight the way metal contacts do. This is particularly important in NW solar cells because the wires are physically disjoint from each other, so charge carriers cannot travel from nanowire to nanowire except through the bottom of the device. However, ITO exhibits a reflectance of $> 10\%$, which reduces the theoretical maximum sunlight that these cells can absorb [145]. The authors of this paper found that they could reduce these losses by forming hemispherical ITO nanoparticles on top of the NW structure, which enhances light absorption due to Mie scattering effects [145]. They do this by etching back the benzocyclobutene (BCB) infill used to fill the NW array by $\sim 100\text{nm}$ and then depositing the ITO layer on top of that.

NW Parameters to Optimize in Lumerical

When optimizing the nanowire array, there are numerous parameters that can be optimized. The most important ones include:

- Top radius (r_t)
- Bottom radius (r_b)
- Height (h)

- Distance between adjacent wires (d).

There are other parameters that can also be tweaked for simulation purposes, such as InP base thickness beneath the NW, metal contact thickness, ITO thickness, and ITO hemisphere radius. In practice, however, fabrication realities limit the ability to tweak these parameters in real-world experimental devices. The nanowire arrays will likely need at least a few microns of substrate material beneath them, or they will remain on the 350- μm thick wafer. The ITO hemispheres form because ITO sticks to InP better than BCB [145], but this process is not conducive to fine-tuning the size of the ITO hemisphere, and even the exact thickness of the planar ITO layer would vary based on the exact shape of the nanowire tip exposed after the BCB etching. Thus, the simulation results will focus on the parameters listed in the bullet point list above. However, an additional challenge is that once one parameter, such as r_t , is optimized for with other parameters held constant, and another parameter, such as r_b , is then optimized, then the nanowire array geometry has now changed, and re-optimizing the previously-optimized parameters may become necessary. This can lead to never-ending optimization loops. Thus, I constrained some of my parameter sweeps based on currently-reported experimental results and fabrication realities.

Finally, a major simulation characteristic to optimize is the mesh size. There is a balance to be struck between mesh size and simulation time. The default mesh size that Lumerical sets is often a good starting point and yields *relatively* quick simulation run times. However, adjusting the defaults can be helpful for more accurate calculations. More details are provided in Appendix B.1.

Lumerical Calculations: Meshing and Predicted J_{SC}

Additionally, meshing in Lumerical can greatly influence the calculated carrier generation from the illumination source in the simulation. Particularly in the NW cells, the optical effects, which enhance light absorption particularly close to the top of the wire, require refined meshing for at least half the length of the wire. This means that the default mesh settings that Lumerical chooses may not suffice for the entire geometry of the simulation. In addition to refining the meshing on the solar cell structure, the meshing can also be refined on the monitors and illumination source. However, refined meshing makes the simulations run longer and consume more memory, so a balance must be struck between refined meshing for accurate calculations and resource capacity.

The carrier photo generation analysis calculates an absorption spectrum and a pre-

dicted J_{SC} with the assumption that each absorbed photon leads to one collected charge carrier, i.e., unity internal quantum efficiency. A single period of each structure was simulated, as illustrated in the schematics above, with appropriate symmetric and anti-symmetric periodic boundary conditions used to simulate an entire cell. 100 nm of Au was used as the back contact to the substrate, as illustrated in Figure 2.1. The simulations employ the AM0 spectrum provided in [95]. Due to the polynomial fitting of the material data, care must be taken with the solar spectrum range so as not to simulate unphysical sub-bandgap absorption. This is why the wavelength range is limited to 300-1000 nm. Given the experimental validation of the NW arrays in [37] and the cells in [145], this thesis will fix the NW height at $h = 1.6\mu\text{m}$, the height chosen in both papers, and fix the inter-wire distance as $d = 500$ nm, the approximate inter-wire distance. Such a wire has an equivalent planar thickness of $t_{eq} \approx 330$ nm, calculated as:

$$t_{eq} = \frac{V}{d^2} = \frac{\pi h(r_t^2 + r_t r_{bot} + r_{bot}^2)}{3d^2}. \quad (2.1)$$

Space Solar Spectrum

It is important to use the AM0 space solar spectrum to accurately simulate the optical performance for these cells in space. Details about doing this in Lumerical and Sentaurus are provided in Appendix B.2.

Top and Bottom Radius Sweep

Starting with $r_b = 175\text{nm}$ as reported in [145], I swept r_t from 35 to 175 nm. Then, fixing $r_t = 75\text{nm}$, I swept r_b from 75 to 175 nm. The parameter sweeps were run without any ITO layers on top or the BCB infill for simplicity's sake, since the focus is the NW geometry that best enhances light absorption. Additionally, though the refractive index properties of the BCB infill may impact light coupling and resulting resonances, its optical properties highly depend on how it is made and processed, which varies wildly, so simulating the NWs without it made the most sense for a parameter sweep focusing on NW geometry. Figure 2.2 plots the predicted current density (J_{SC}) of the NW arrays with the r_t and r_b sweeps described above.

Electric Field Plots

While the rise in predicted current density (J_{SC}) from 35-65 nm makes sense because the amount of InP material is increasing, the decrease in predicted J_{SC} for $r_t > 65\text{nm}$ is counterintuitive. This likely has to do with the optical modes and

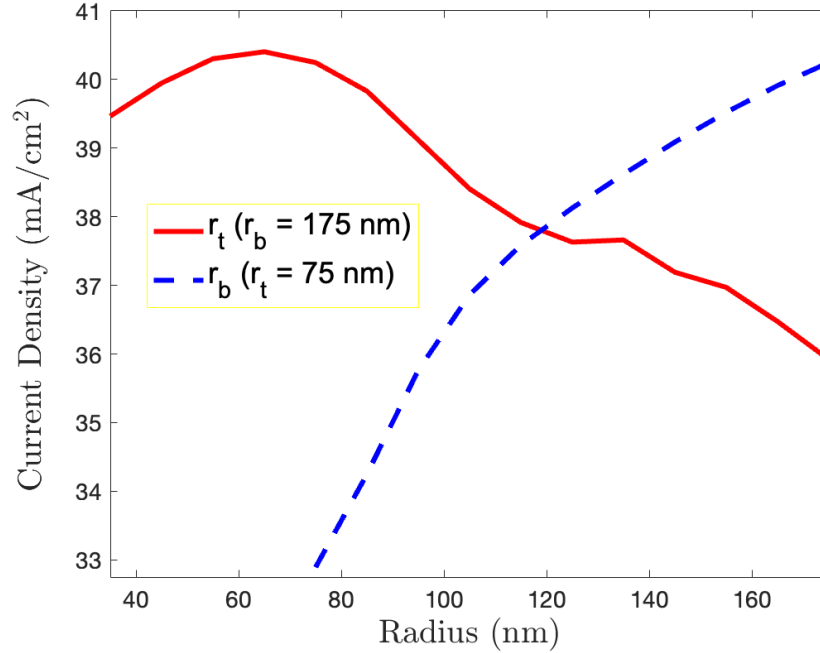


Figure 2.2: Lumerical parameter sweeps of r_t and r_b for tapered NWs. The r_t sweep was run with $r_b = 175$ nm while the r_b sweep was run with $r_t = 75$ nm.

resonances that can be supported at different radii as well as the intensity of the solar spectrum at the wavelength associated with the relevant modes. This can be investigated by comparing heat maps of the electric fields (E), given in V/m, within NWs with $r_t = 65$ nm and $r_t = 175$ nm, both with $r_b = 175$ nm. E is plotted at a wavelength of $\lambda = 550$ nm, which is approximately where the intensity of the solar spectrum achieves a maximum in the visible spectrum. The color bars have been scaled identically for all plots to make visual comparisons easier. Cross-sections are taken at heights of $z = 1.60\mu\text{m}$ and $z = 1.50\mu\text{m}$.

E is higher in the wires with $r_t = 65$ nm than in $r_t = 175$ nm. In the cylindrical NW, with $r_t = 175$ nm, the intensity of E decreases with distance from the surface within the top 100 nm of the wire. However, the intensity of E actually increases with distance from the surface within the first 100 nm from the wire. This illustrates the enhancement of E -field absorption in the tapered NW. The monotonic increase of the current density with increasing r_b is more intuitive.

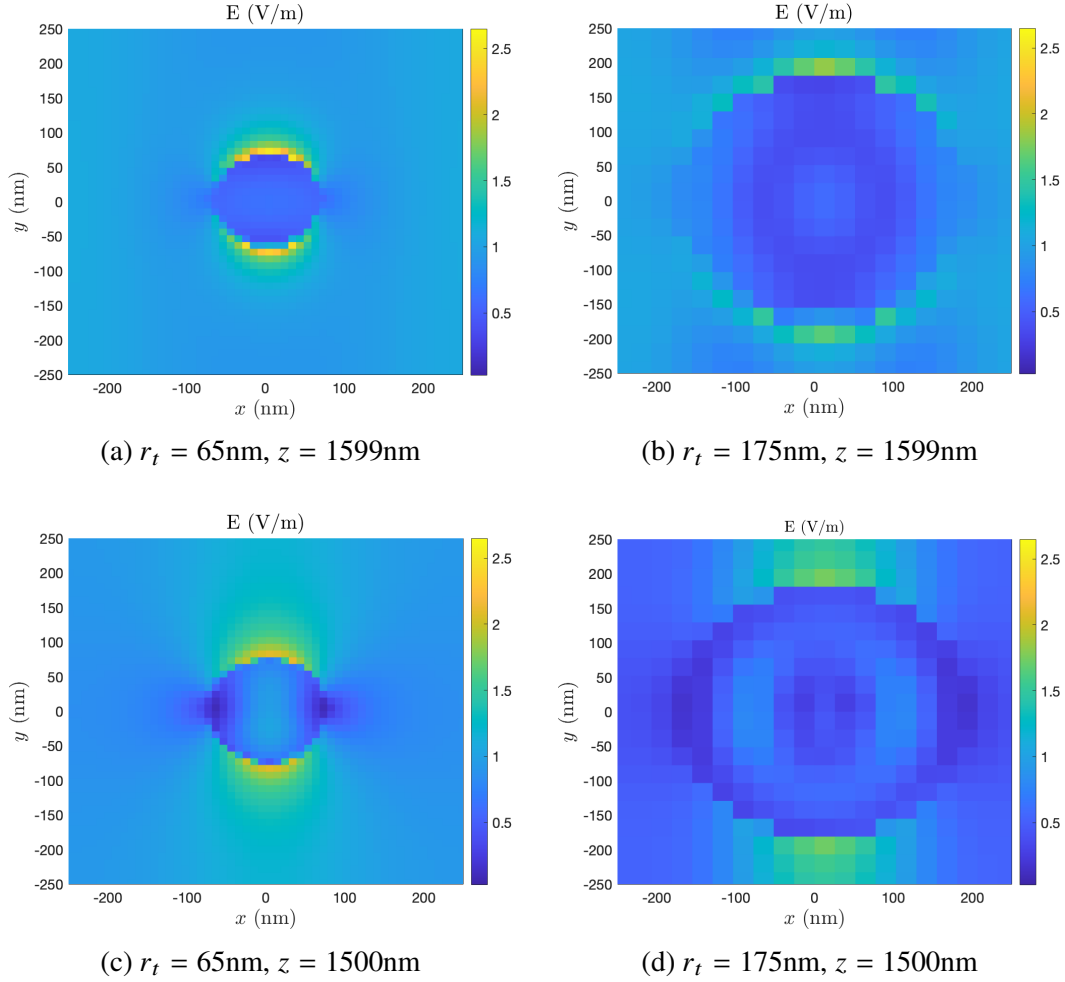


Figure 2.3: x - y cross sections of electric fields in NWs with different r_t and z . The electric field is reported in V/m.

Generation Rate Plots

The effects of the field absorption enhancement can be illustrated better through cross-sectional profiles of the resulting generation rates, which also depends on the ability of the wire to absorb E fields at the given wavelength. Figure 2.4 will compare carrier generation rates for wires with $r_t = 65\text{nm}$ with $r_t = 175\text{nm}$. In both cases, $r_b = 175\text{nm}$. Generation rates are reported in units of 10^{28} carriers. Cross-sections are taken at heights of $z = 1.60\mu\text{m}$ and $z = 1.50\mu\text{m}$:

The color bars have been scaled identically for all plots to make visual comparisons easier. Comparing Figure 2.4a and Figure 2.4b, the generation rate (G) is higher throughout the NW cross section in a tapered NW — in this case, when $r_t = 65\text{nm}$ — than in the cylindrical NW with $r_t = 175\text{nm}$. In Figure 2.4a, $G \sim 2.8 * 10^{28}$

carriers/m³/s while in Figure 2.4b, $G < 2 * 10^{28}$ carriers/m³/s throughout most of the center of the wire, with the generation rate increasing near the edges. Looking ~ 100 nm down from the top of the wire, the light absorption enhancement becomes even more evident. In Figure 2.4c, with $r \approx 72$ nm, the generation rate exceeds $4.5 * 10^{28}$ carriers/m³/s. Notice that the radius in Figure 2.4c is larger than $r_t = 65$ nm because of the NW taper. Meanwhile, in Figure 2.4d, with $r_t = 175$ nm still, the generation rate throughout the wire is almost entirely less than $2 * 10^{28}$ carriers/m³/s and never approaches $3 * 10^{28}$ carriers/m³/s or higher. This helps illustrate why tapering a NW can enhance light absorption and result in a higher J_{SC} than a purely cylindrical NW despite using less absorber material, up to a point.

Since the predicted current density is almost identical for $r_t = 65$ nm and $r_t = 75$ nm, I chose to simulate nanowires with $r_t = 65$ nm and $r_b = 175$ nm for many of the simulation results that follow to stick with the ideal case. The behavior of the $r_t = 75$ nm and $r_b = 175$ nm NWs in the fabricated solar cells in [145] would be similar. However, for Figure 2.5, $r_t = 75$ nm was used for a comparison of the no-ITO versus planar only versus planar and hemispherical ITO configurations to perform this comparison for the record literature geometry specifically.

Dam et al. reports the FDTD simulation results comparing planar versus hemispherical ITO on the E-field within the top of the NW, as well as the resulting boost in absorptance, the Mie scattering efficiency, and the absorptance effects on p-polarized and s-polarized light, respectively [145]. Figure 2.5 shows the effects on the resulting carrier generation profiles, comparing generation profiles at $z = 1500$ nm for these NWs with no ITO, planar ITO only, and planar + hemispherical ITO. These NWs have $r_t = 75$ nm and $r_b = 175$ nm. The x - z cross-section is at $y = 0$. The thickness of the planar ITO layer was chosen to be $t_{ITO} = 300$ nm so that the layer completely covers the NW tip and can form the hemispherical nanoparticle. The radius of the ITO hemisphere is chosen to be $r_{ITO} = 175$ nm to match the bottom radius of the InP NW. These dimensions were chosen through some combination of estimating from the cross-sectional SEM in [145] and choosing dimensions that would likely result based on the NW geometry.

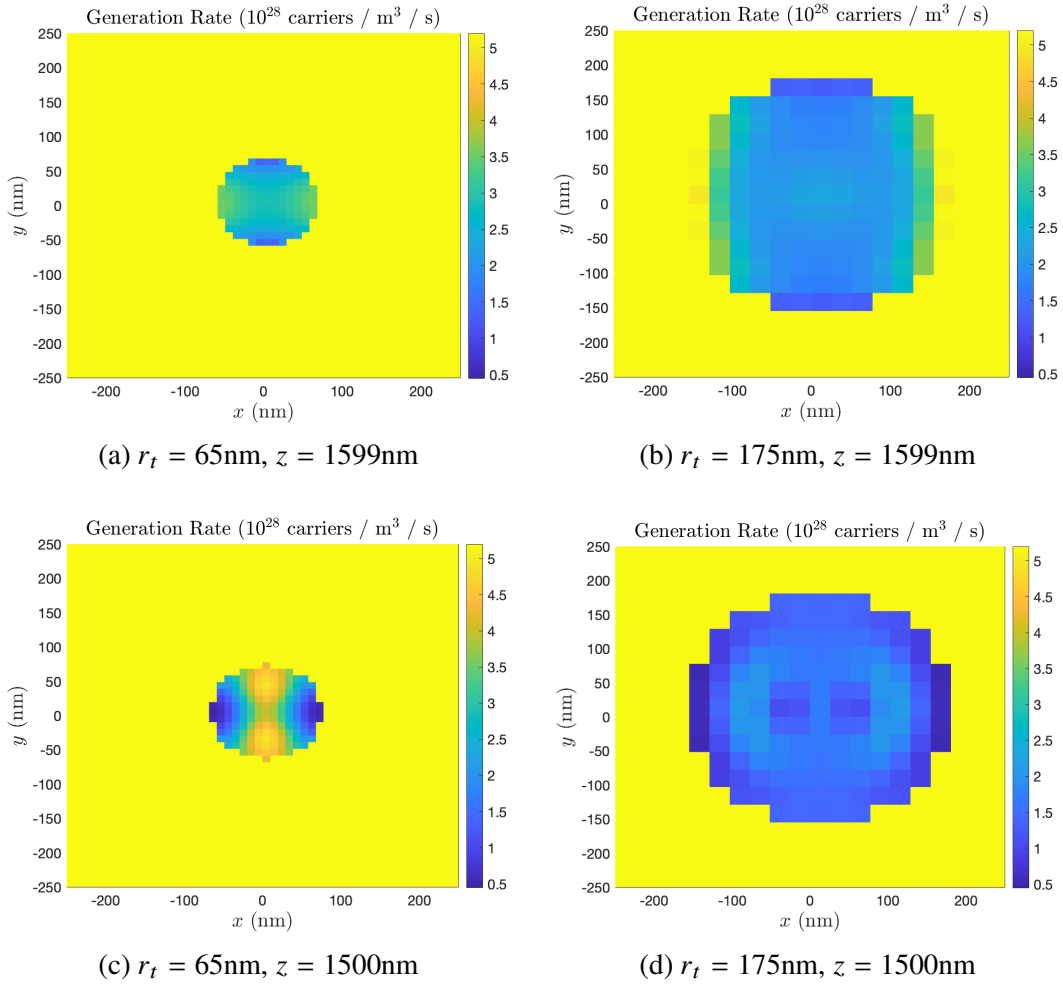


Figure 2.4: x - y cross sections of generation rates of NWs with different r_t and z . The generation rate is reported in 10^{28} carriers.

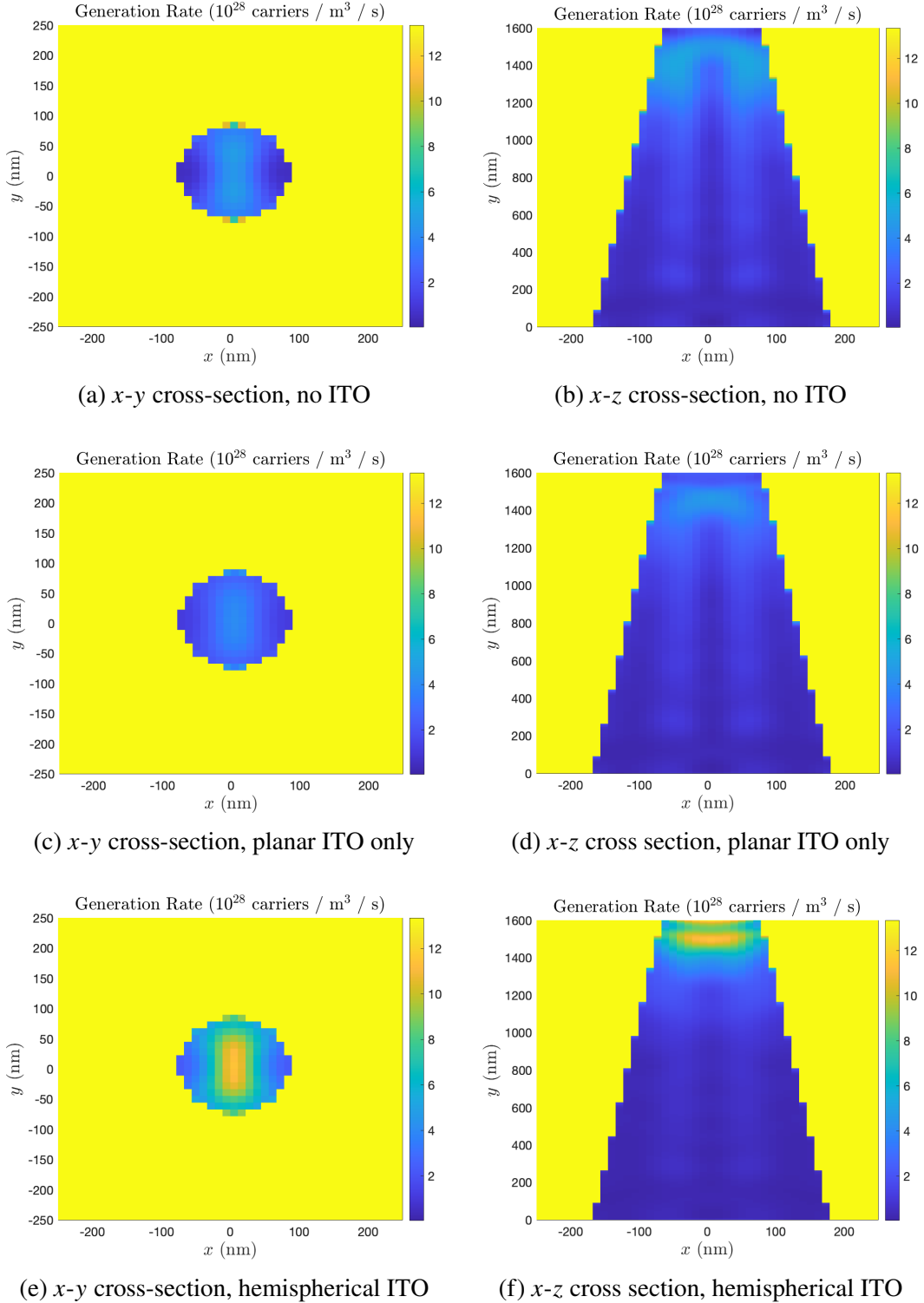


Figure 2.5: Cross sections of generation rates of NWs with and without ITO. 2.5a and 2.5b illustrate the case with no ITO, 2.5c and 2.5d illustrate the case with only planar ITO, and 2.5e and 2.5f represent the case with planar and hemispherical ITO. Here, $r_t = 75\text{nm}$.

The plots of the generation rates illustrate how the hemispherical ITO nanoparticle enhances absorption in the top of the NW compared to the no-ITO and planar-ITO cases. It shows the effect of the Mie scattering phenomenon with the hemispherical nanoparticle forward scattering light into the NW [145]. The x - z cross sections also show that the carrier generation is stronger a bit below the surface than it is right at the surface. On the other hand, the generation rates are lower deeper into the wire for the NW with the hemispherical ITO nanoparticle than for the no-ITO and even planar-ITO case. This is likely because the hemispherical ITO case has more ITO absorbing the incoming sunlight, such that less of it is available to be absorbed, even though Mie scattering helps counter this attenuation by enhancing the surface carrier generation rate.

2.3 Comparison to Planar and Pyramidally-Textured Structures

For comparison, this thesis also reports planar and pyramidal structures of similar thicknesses. Figure 2.6 illustrate schematics of all structures side-by-side for comparison:

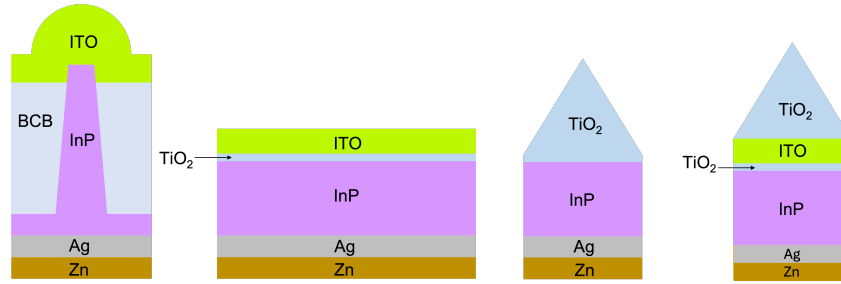


Figure 2.6: Schematics of the simulated NW, planar, and pyrimidal structures. The pyramidal structures are illustrated both with and without a TiO_2 + ITO ARC underneath the pyramids.

The pyramid schematics are illustrated both with and without a TiO_2 + ITO ARC underneath the pyramids. This is because in practice, there will likely need to be a conductive layer under the pyramids to make contact and assist with lateral carrier transport for good performance.

The schematics in Figure 2.6 reflect a single unit cell of the PV structure. However, the structure is a periodic repetition of these individual unit cells. The planar cell just extends indefinitely in the x and y directions. Figure 2.7 illustrates what this periodic structure looks like for the NW and pyramidally-textured cells:

For the planar InP thin film cell, a 10 nm TiO_2 layer was used on top of the InP

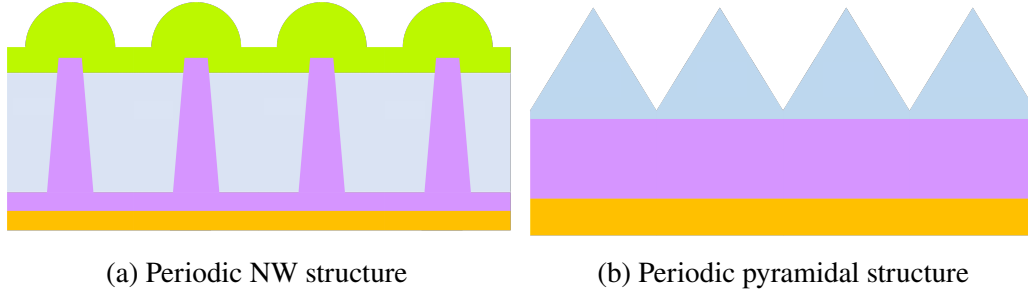


Figure 2.7: Illustration of periodic NW and pyramidally-structured cells.

followed by a 60 nm ITO layer as an AR coating, as reported in [166]. The 10 nm TiO_2 serves as an electron-selective contact (ESC) so that the thin 330-nm InP layer does not require an internal pn junction for carrier collection, similar to the cell reported in [165].

For the pyramidally-textured InP cell, in the ideal case, the 10 nm TiO_2 layer was used as an ESC, and antireflection was enhanced by formation of an array of TiO_2 square pyramids. The base of each pyramid was $b = 450$ nm, while the height of each was $h = 540$ nm. All cells had 50 nm of Ag and 50 nm of Zn as a bottom ohmic contact to p-type InP. However, for the more realistic case, which would require a conductive layer, a 40 nm ITO layer was also included between the 10 nm TiO_2 planar layer and the TiO_2 pyramids. This layer was thinner than the 60 nm ITO used for the planar cell because the ITO is only needed to help make electrical contact, not for ARC purposes. The pyramids already reduce reflection.

Electric Field Plots

Figure 2.8 shows the plots of the electric fields of the NW and the TiO_2 -only pyramidal structures, excluding the ITO, from Figure 2.6. Figure 2.9 shows the resulting generation profiles. These plots focus on the TiO_2 -only pyramidal structures to highlight the difference in E-field and generation profiles between NWs and pyramidally-textured cells, and the TiO_2 -only case is the ideal case.

The x - y cross sections for the planar geometry were omitted because the device symmetry makes these profiles flat and constant throughout the cross section. However, their x - z generation profiles at $y = 0$ will be shown to illustrate how the generation rate evolves throughout all three structures the further light enters the device.

The x - y cross sectional profiles illustrate the differences between the light-absorption enhancement in NWs and pyramidally-structured cells. The electric field in the

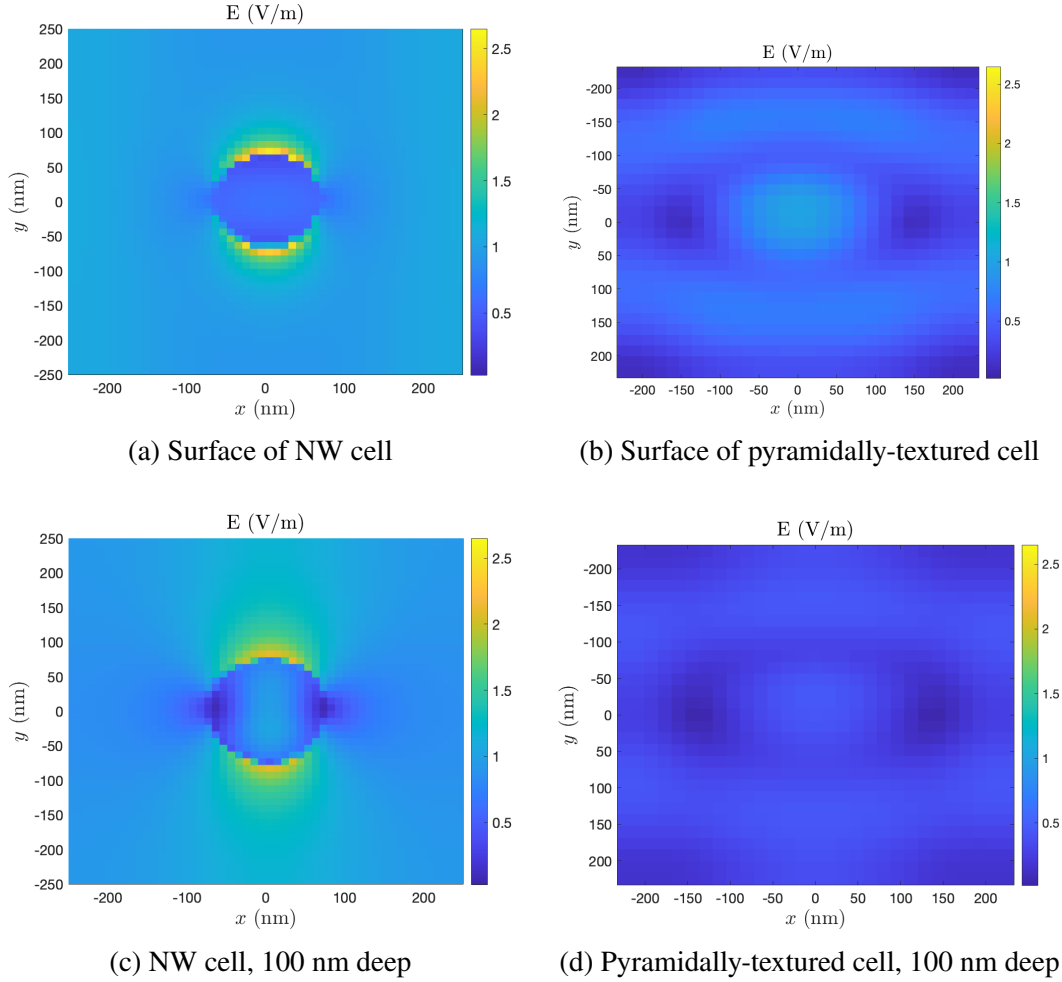


Figure 2.8: x - y cross sections of electric fields in NWs and pyramidally-textured cells. The NW's $r_t = 65$ nm while the pyramid's $b = 450$ nm and $h = 540$ nm. The electric field is reported in V/m.

NW is stronger within the wire at a depth of 100 nm, while the electric field in the pyramidally-structured cell is stronger at the surface. This illustrates that the light absorption enhancement in NWs comes from mode-related coupling while the light absorption enhancement in the pyramidally-structured cells comes from concentrating the light more strongly onto the semiconductor surface underneath the TiO_2 pyramids.

Generation Rate Profiles

The resulting generation rate profiles in Figure 2.9 show how the generation rate at the center of the pyramidally-structured cells is much stronger than the rate in the NWs. However, 100 nm below the surface, the generation rate in the textured cells is much weaker than in the NW at the same depth. These plots allow viewers to

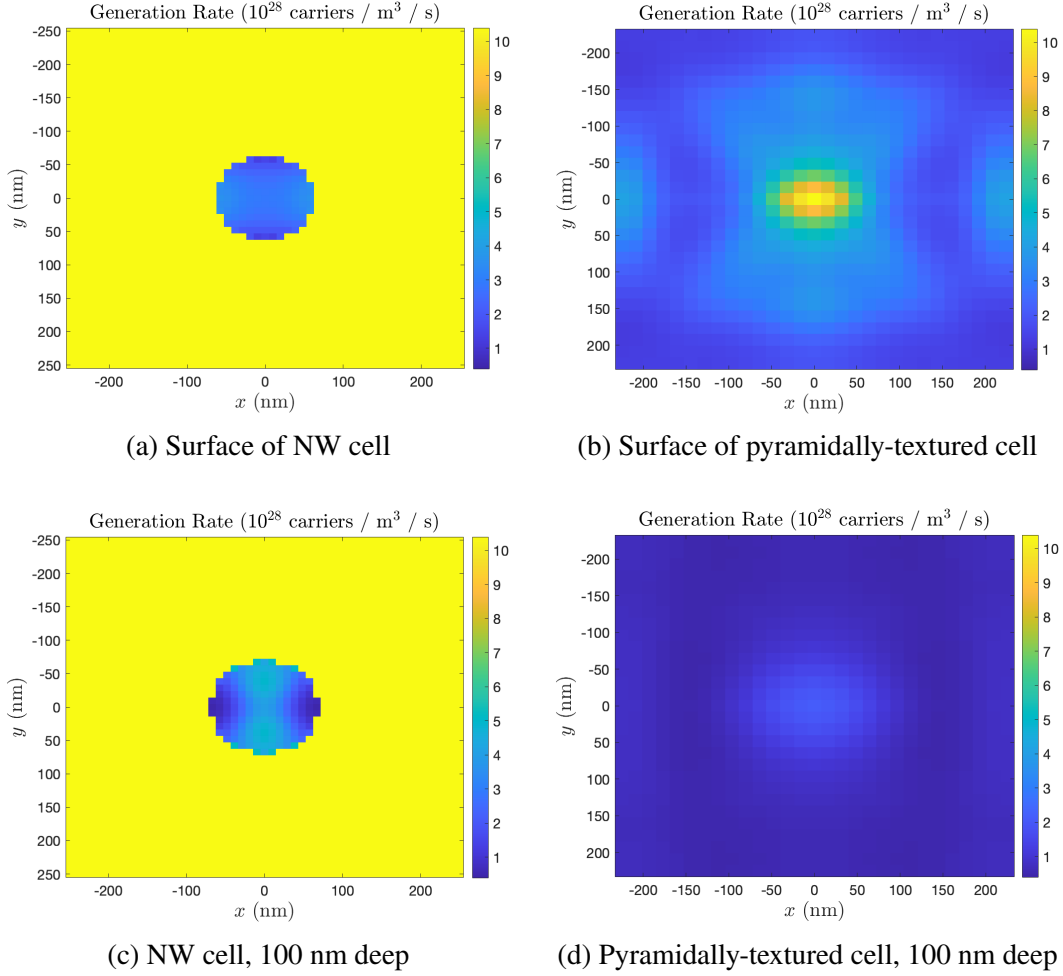
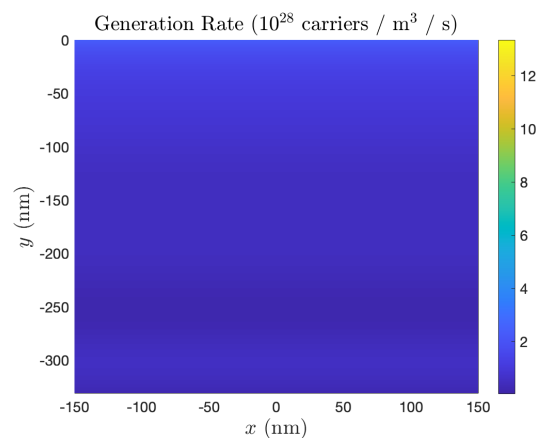


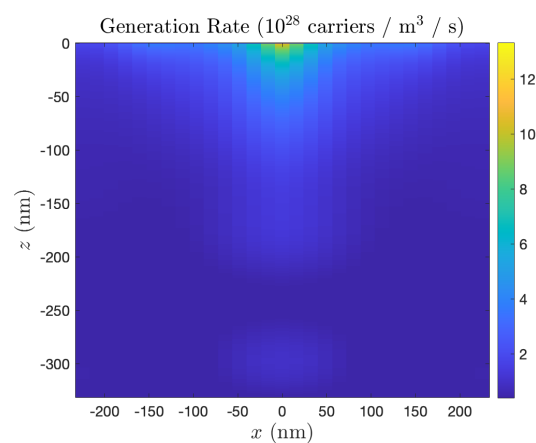
Figure 2.9: x - z cross sections of generation profiles in NWs and pyramidally-textured cells. The generation rate is reported in 10^{28} carriers / m^3 / s. Here, $r_t = 65\text{nm}$. There is no ITO in the NW case.

visualize this light absorption enhancement first-hand at different depths for different structures.

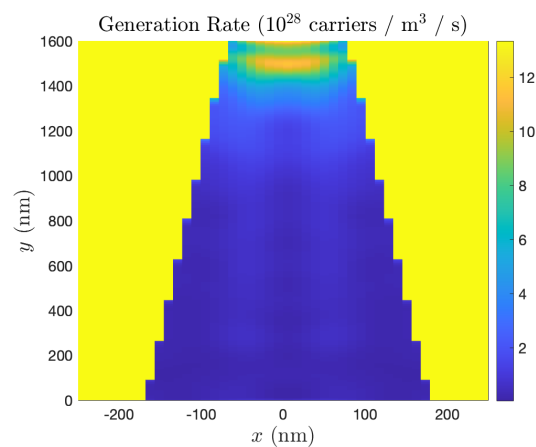
The vertical cross-sectional profiles of the generation rates illustrate how different geometries affect generation rates through the depth of the cells. They illustrate the extent of carrier generation enhancement through surface texturing or nanostructure use. The use of NWs and ITO hemispherical nanoparticles to improve mode coupling and funnel light more efficiently via Mie scattering enhances carrier generation at the NW surface much more intensely than in the textured and planar cells. The carrier generation rate in the planar cell never gets as high as it does near the surface of the textured and NW cells. Visually, the plots show that the generation rate enhancement is strongest in the NW, with a strong carrier generation enhancement



(a) Planar cell



(b) Pyramidally-textured cell



(c) NW cell

Figure 2.10: x - z cross sections of generation profiles in NWs, planar cells, and pyramidally-textured cells. The generation rate is reported in 10^{28} carriers / m^3 / s.

of over 5x throughout the surface of the NW compared to the surface of the planar cell and an enhancement of 2-3x compared to the surface of the pyramidal cell. This visual explains why NWs can achieve comparable total carrier generation despite using less material.

Predicted J_{SC} and Absorption Spectra for the NWs, Planar, and Textured Cells

Table 2.1 summarizes the predicted J_{SC} for the different geometries, capturing how the tradeoffs in these absorption enhancements versus device geometry manifest in the overall effectiveness of light capture in the device.

Table 2.1: J_{SC} of different geometries

Geometry	J_{SC} (mA/cm ²)
NW (with ITO nanoparticle)	35.0852
Planar (ARC, no pyramids)	33.9873
Pyramids (no ITO)	38.0511
Pyramids + Planar ITO	35.8569

Evidently, different methods of absorption enhancement can theoretically achieve similar J_{SC} . Note: Table 2.1 reports the simulated J_{SC} results from the simulations run for the PVSC 2022 conference abstract [6]. However, because mesh settings were changed for more consistent comparisons between the field and generation rate profiles that were later added, the exact J_{SC} values were not able to be replicated. However, previous literature results illustrate that, at least in simulations, J_{SC} s of over 42 mA/cm² can be achieved [80]. This confirms that these values are indeed physical, including the high J_{SC} for the pyramidally-textured cells. Additionally, the J_{SC} calculated will depend on whether you choose to count the charge carriers generated in the ITO, BSF, substrate, etc. Since the BSF, ITO, and substrate are not intended to be the charge carrier generation components, and given that losses will occur compared to the theoretical maximum anyways, the simulations run for the thesis only included the NW itself, and only the portion of the ITO up to the top of the NW.

Fig. 2.11 plots the simulated absorption spectra of the cells to illustrate the differences between the geometries.

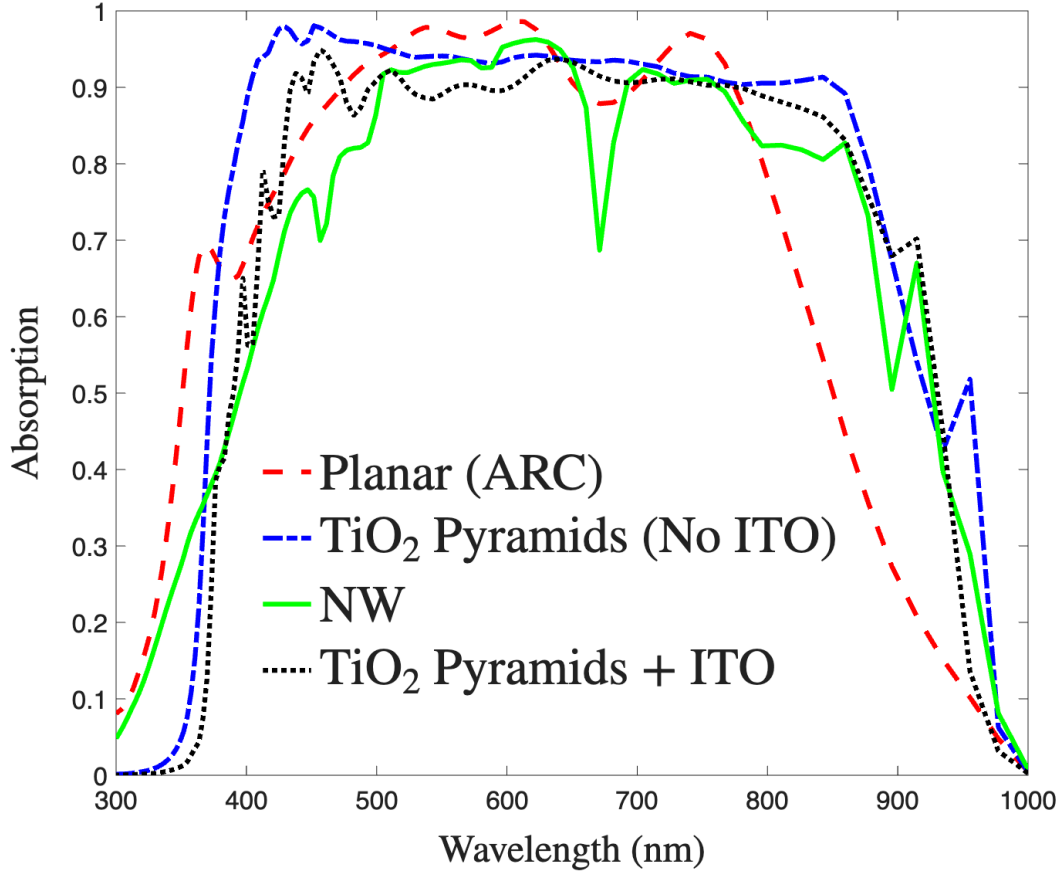


Figure 2.11: Absorption in the structures illustrated in Fig. 2.6.

The planar InP cell with the AR coating enhances absorption at shorter wavelengths more than the other geometries, while the other two geometries better enhance absorption at longer wavelengths. This makes sense because the thickness of all components in the planar InP cell are less than 400 nm, while the nanowire has a height of 1.6 μm , which is on the order of the wavelength ranges examined. The predicted J_{SC} of the pyramidally-structured cells without the ITO conductive layer is the highest. Figure 2.11 illustrates that the pyramidally-structured cell generally outperforms the planar and NW structures at the longer and shorter wavelengths while exhibiting comparable performance throughout the middle of the wavelength range.

However, as mentioned before, one caveat is that the currently-simulated pyramidally-structured cell represents a limiting case, since a transparent conductor is needed on top of the InP to transport charges to the metal ohmic contacts with minimal absorption loss. The planar InP cell with TiO₂ and ITO needs the ITO layer to create the 70 nm thick AR coating since previous work showed that 10 nm TiO₂ was

the optimal thickness for maximizing V_{OC} . However, the TiO_2 pyramids already serve an antireflection function, so the ITO layer will simply hurt its performance.

The ITO layer hurts absorption throughout most of the wavelength range as compared to the structure without ITO since ITO is not completely transparent in the wavelength range of interest. The thinner the ITO used, the closer the performance of such a cell can be to the limiting case shown here. The TiO_2 pyramids themselves can be fabricated using nanoimprinting, which makes them potentially easier and cheaper to fabricate than NWs. While NWs can in theory be fabricated by nanoimprint lithography, in practice the dimensions involved ($r_t = 75nm$) make it more challenging a process to design and execute than fabricating pyramids with bases of a couple hundred nanometers.

Similarly, the performance of the NW geometry suffers due to the ITO. Fig. 2.12 plots the absorption of the NW array described above along with one with only a 50-nm thick planar ITO layer and one with no ITO layer, with the latter representing another limiting but unrealistic situation.

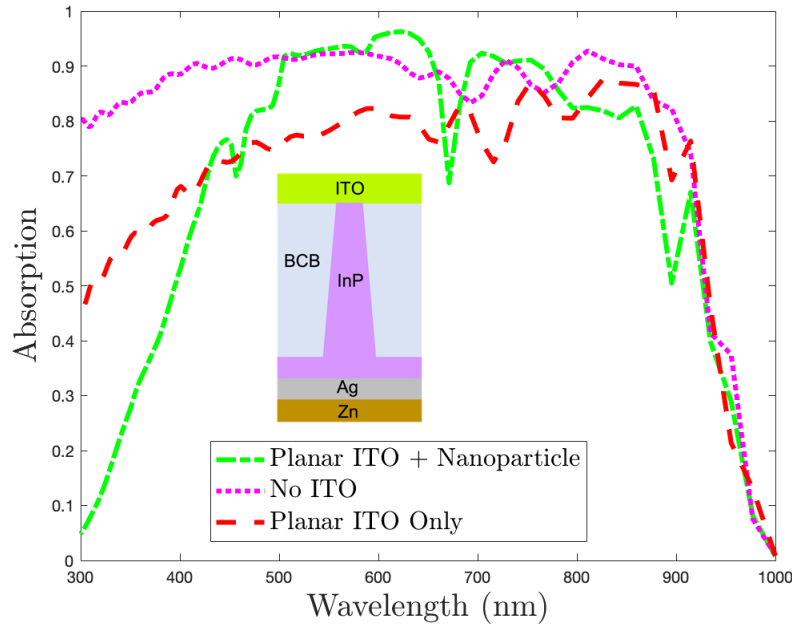


Figure 2.12: Absorption of the NW structure with different ITO configurations and a schematic of the structure with only planar ITO of thickness $t_{ITO} = 50nm$.

The absorption plot shows that the geometry with the ITO hemisphere, which results in Mie scattering of the light into the wire, hurts short-wavelength absorption relative to the structures with and without just planar ITO. This is in part due to the larger

quantity of ITO used in the structure containing the hemispherical nanoparticle, in which the planar ITO layer was 300 nm thick as opposed to the 50 nm layer we used in our simulation. Despite the lower amount of ITO used in the geometry shown in the inset of Fig. 2.12, the NW array with planar ITO alone does not absorb as much light in the middle of the wavelength (500-800 nm) range. Coupling a thinner planar ITO layer and an optimized nanoparticle radius could still further improve the device performance. However, given that the nanoparticles were a byproduct of depositing ITO onto a NW array with the wire top poking through the benzocyclobutene (BCB) infill surrounding it, more work or new fabrication methodologies would be needed to optimize the ITO dimensions for improved performance. Additionally, the creation of the nanoparticles has been difficult to replicate, which currently means we cannot consistently rely on the nanoparticles for absorption enhancement in real devices.

When taking all of these factors into consideration, as well as the fabrication challenges of each method, it becomes clear that a simple heterojunction thin-film planar InP cell with an optimized AR coating warrants further study and consideration for space solar cells alongside structures with more complex means of absorption enhancement. Recent experimental work on fabricating thin films of InP includes the spalling technique demonstrated in [73]. While the fabricated films demonstrated thus far are currently 15 μm thick, further work, both on this technique and other fabrication methods, could help achieve thin InP films.

2.4 Electrical Simulation of Nanowire and Planar Structures

Sentaurus

The optical generation profiles from Lumerical's simulations were imported into Sentaurus Device for electrical simulation. See Philip Jahelka's PhD thesis for detailed information on the Sentaurus workflow and code to accomplish this [59]. Because this thesis focused on the fabrication of NWs and untextured planar solar cells, the Sentaurus simulations also focus on these two. Sentaurus simulations of textured solar cells will be reserved for future work. The Sentaurus simulation results presented in this section were used to optimize solar cell structures with MOCVD-grown layers on top of an InP substrate. These wafers were then used to fabricate solar cells using either standard photolithography and mesa isolation procedures for planar cells, which will be described in later sections in greater detail, or top-down fabrication of NWs using ICP-RIE followed by infill, ITO, and contact deposition.

n^+p versus p^+n Structures for NW and MOCVD Cells

The thesis focuses on n^+p devices for the NW and MOCVD cells. This is because electrons tend to have a longer diffusion length in p-InP than holes do in n-InP, and because an n^+ surface layer has lower recombination than p^+ surface layer [160]. Figure 2.13 illustrates schematics of the optimized structures for planar and NW cells, respectively. Because the window layers were added later, after initial optimization, upon the suggestion of our vendor Microlink Devices, the NW MOCVD stack is 50 nm shorter than the planar MOCVD stack.

It must also be noted that the MOCVD stack includes a 50 nm p-InAlAs back surface field, and the n^+ InP window layer serves as a front surface field in both the thesis and patent cells. This is because the bandgap offset between InP and InAlAs acts as a barrier for electrons, so that they do not directly recombine at the positive terminal without passing through the external load, while the heavy doping in the window layer confines the holes so that they do not directly recombine at the negative terminal without passing through the external load. Remember, to generate power in a solar cell, the current in the device should still be sufficiently dominated by drift current, with electrons going from the p-type layers to the n-type layers and holes going from the n-type layers to the p-type layers, despite operating in positive bias with the p-type layers connected to the positive terminal and the n-type layers connected to the negative terminal.

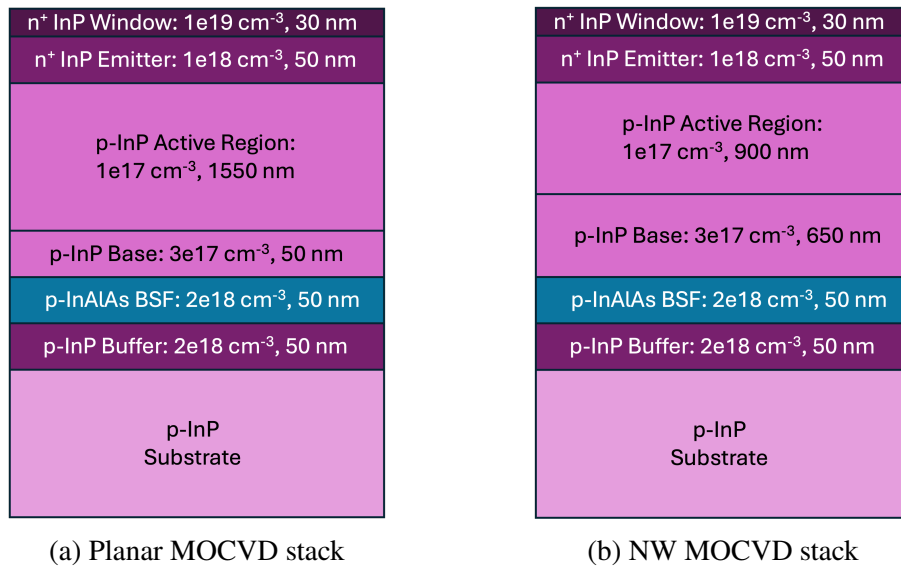


Figure 2.13: Schematics of the planar and NW MOCVD-grown InP wafers, designed from Lumerical and Sentaurus simulations. The NW layer stack has a thicker base region than the planar stack, and is 50 nm smaller.

Figure 2.14 illustrates the band diagrams for the planar and NW stacks as generated from Sentaurus with no applied voltage, based on the Sentaurus simulation results with the generation rate profile imported. The generation rates used for the simulated band diagrams were calculated using a 10 nm TiO_2 + 60 nm ITO ARC on top, while the NW band diagram used the ITO hemispherical nanoparticles. However, only the InP regions are shown in the band diagrams.

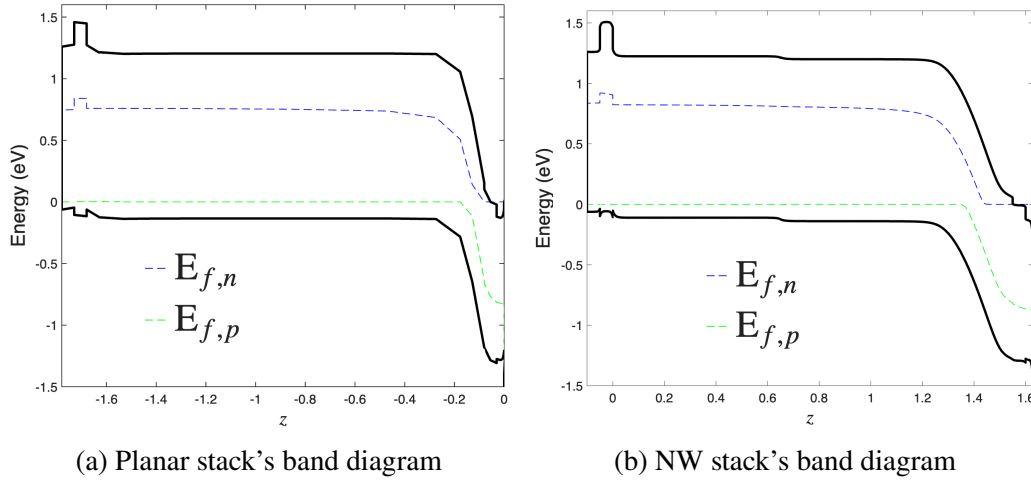


Figure 2.14: Band diagrams of the planar and NW MOCVD-grown InP wafers from Sentaurus at 0 V after the Lumerical-simulated optical generation rate profile was imported. The plot shows the conduction and valence bands in black, as well as the quasi-electron and quasi-hole Fermi levels.

NW versus MOCVD Stacks

The key difference between the two structures is the difference in the thicknesses of the active region versus the lightly-doped base. The NW stack has a much thicker base region than the planar stack, which tends to prefer larger active regions. This might be for several reasons. While the NWs have a higher surface area to volume ratio than the planar structures, The tapered NW geometry has a very different carrier generation profile than the planar geometry, carriers in NWs diffuse axially *and* radially to reach the contacts.

Table 2.2 lists the simulated figures of merit for the planar versus NW solar cells based on the Lumerical optical generation profiles and the Sentaurus electrical simulations. The J_{SC} for the planar structure reflects that achieved with a 10 nm TiO_2 + 60 nm ITO ARC on top, while the J_{SC} for the NWs reflects that achieved with the ITO hemispherical nanoparticles.

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF
Planar	21.287	36.49	919.6	86.67%
NW	16.355	28.33	928.9	84.90%

Table 2.2: Figures of merit comparisons for the planar versus NW cells simulated in Lumerical and Sentaurus. This table reports the efficiencies, short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF).

The simulations predict a somewhat higher V_{OC} for the NW cells, potentially because NWs concentrate light to increase the effective photon flux. However, the predicted J_{SC} is much lower after the recombination mechanisms have been taken into account. The simulated performance for the NW cell is less than that reported in [145], but this is partly because the InP stack is shorter and the material layers are not identical.

2.5 Nanowire Fabrication Methods and Properties

NW fabrication attempts were made using procedures similar to those outlined in [37], with some modifications. Specifically, I used square chips diced from 2" p-type (Zn-doped) InP wafers. I only used a Cr hard mask by defining a pattern of an array of circles directly onto the InP surface using electron-beam (e-beam) lithography, and deposited 50 nm of Cr using e-beam evaporation followed by liftoff. Since only normal taper NWs were made, CH₄ was flowed at a rate of 24 sccm during the ICP-RIE process. Figure 2.15 shows an SEM image of a 5x5 array of Cr circles with radii $r = 100$ nm and distance $d = 500$ nm between them.

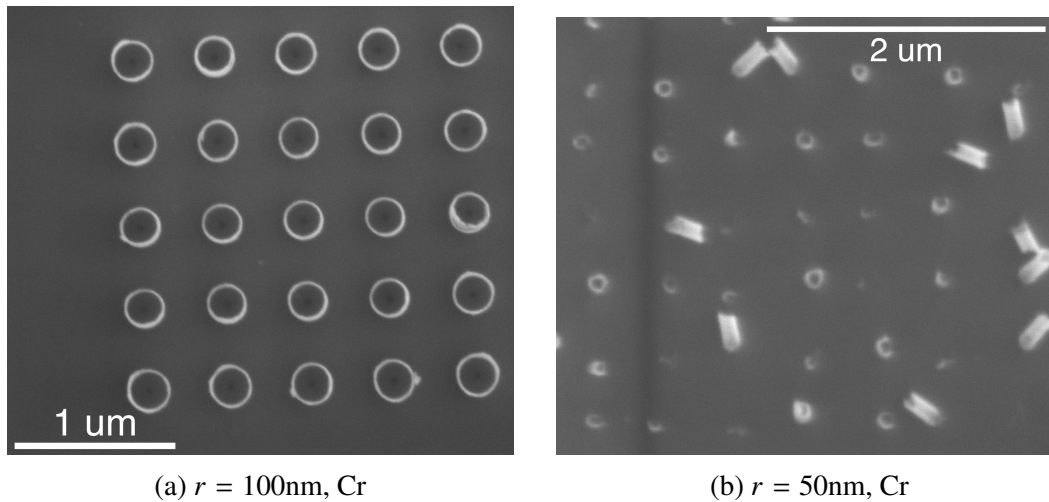


Figure 2.15: Arrays of Cr circles, with $r = 100$ nm and $r = 50$ nm, respectively.

Fabrication attempts with $r = 50$ nm resulted in irregular patterning and metal deposition, where either some of the circles were not written properly into the e-beam or

the metal did not deposit and lift off effectively. This demonstrates the challenge in consistently fabricating arrays with the fine resolution needed for the desired nanostructures. I was able to successfully fabricate some NW arrays, however, through the deposition and etching process outlined earlier. Figure 2.16 illustrates some fabricated NWs with radius $r = 50\text{nm}$.

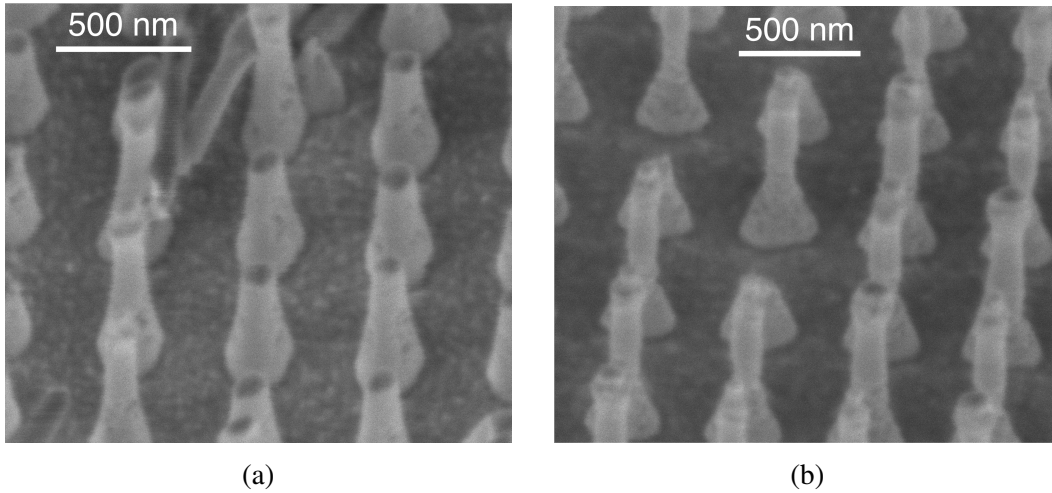


Figure 2.16: Fabricated NWs with $r = 50\text{nm}$. NWs were etched top-down in InP substrates using ICP-RIE.

These fabrication attempts illustrate the difficulty in obtaining conical, tapered NWs. The NWs in Figure 2.16a illustrate the desired conical shape, while Figure 2.16b shows NWs where the top half are quite cylindrical before they start tapering at the bottom half. The image also shows how some of the wires, especially in Figure 2.16b, are broken, and only have the widened tapered base remaining. This illustrates the challenge of getting a high yield of tapered NWs, and these irregularities will affect the resulting absorption spectrum. More work is needed to perfect the tapering fabrication process and improve the NW array yield.

2.6 Conclusion

In conclusion, NW solar cells show promise in achieving lighter, radiation-hard solar cells without much sacrifice in initial device efficiency. This is especially true when paired with light absorption enhancement through Mie scattering via the use of ITO hemispherical nanoparticles that naturally result from the deposition of ITO that is necessary for these NW devices. However, in practice, NW fabrication is incredibly challenging to execute consistently and reliably, and obtaining the desired morphology via etching does not always occur. These structures already exhibit

fragility in fabrication and handling before even being subject to the turbulence of space launch and operation. Moreover, the NWs were fabricated via e-beam lithography, which is a sequential process in terms of patterning the material to create the NW array. A NW square array that measures 3 mm on each side takes around 4 hours to pattern in Caltech's KNI cleanroom. Nanoimprint lithography has been proposed as a method to scale up NW array fabrication, which involves using e-beam lithography to fabricate a template and then using the template to pattern circular arrays for further processing in one go via "stamping." However, in practice, the template can break, and implementing this process also requires care. Given the challenges involved with NW fabrication even before completing the processing steps for finished solar cells, the rest of this thesis will focus on making planar InP solar cells thinner, lower-cost, and more scalable while minimizing efficiency loss from less-precise fabrication methods.

Chapter 3

EPITAXIAL PLANAR SOLAR CELLS

Epitaxial solar cells refer to solar cells whose component layers were formed by a crystalline growth technique that attempts to make new layers adopt the crystalline structure of the growth substrate [45]. One way to create p - n junctions is to deposit p and n -doped layers via MOCVD, which is considered an epitaxial method if it is used to grow crystalline layers. Etching these wafers top-down is a relatively easy way to create p - n junctions in NWs because semiconductor fabrication companies can typically achieve precise crystal layer thicknesses with greater accuracy and reproducibility than lab-grown structures, whether top-down or bottom-up.

The cells in this paper were fabricated using standard photolithography and mesa isolation procedures on top of an MOCVD stack commissioned by Microlink Devices. These procedures will be described in greater detail in Appendix A.1. The stack is shown in Figure 2.13a. The thicknesses and doping concentrations were optimized using Lumerical and Sentaurus. The cells were measured and characterized using current-voltage (I-V) curves, which are plotted as current density-voltage (J-V) curves, and external quantum efficiency (EQE) measurements, which will also be described and reported in Sections 3.3 and 3.4. Along the way, single and double-layer ARCs were investigated, and a single-layer ARC was used to improve the epitaxial cell efficiency. Different metal contact stacks were also investigated to find the simplest ones that would be the most ohmic with the least resistivity.

Note that all I-V measurements presented in this thesis were taken under an AM1.5G spectrum lamp, rather than an AM0 lamp. To truly assess the performance in space, measurements should be taken under an AM0 spectrum.

3.1 Epitaxial Layer Optimization

Sentaurus was used to optimize the MOCVD epitaxial stack used to fabricate the planar solar cells used as references against which this work compares the performance of diffusion-doped cells. The goal is to investigate how closely the planar diffusion-doped cells can match the MOCVD cells, which are expected to be high-performance.

3.2 Planar Solar Cell Fabrication

The basic procedure will be outlined in this section. More detailed troubleshooting tips are provided in Appendix B for practical time-saving tips that can help readers want to rip their hair out of their heads a little less.

Zn-based contacts, paired with Au or Ag, are some of the most practical ohmic contacts to p-InP [68]. A metal stack of Ag-Zn-Ag, with each layer being 50 nm, was deposited using thermal evaporation. This was followed by annealing at 375°C for 5 minutes.

Next, a mesa isolation was performed on the MOCVD wafer to electrically isolate adjacent solar cells with a fixed geometry. The fabricated solar cells were squares with side lengths of 3 mm, so the device areas used were 0.09 cm^2 , not subtracting out the shaded area from the grid contacts. Wet chemical etching was used to perform the mesa isolation. First, the photolithography procedure outlined in Appendix A.1 was used to define the square pattern illustrated in Figure A.1. A 3-minute etch with a 1:1 HCl:H₂O etchant was used for this process. See Appendix B for more detail about the mesa etch.

Then, Ni-Ag grid top contacts were deposited in an electron-beam evaporator using the pattern illustrated in Figure A.2, followed by lift-off. At this stage, functioning solar cells are fully fabricated. From here, an ARC coating can be deposited if desired. However, much of the characterization is performed with bare InP cells as a baseline.

3.3 MOCVD Characterization Results

Light and Dark J-V Curves

Figure 3.1 illustrates the light and dark J-V curves of the best MOCVD cell fabricated without an ARC:

Comparison to the Record Patent Planar InP Cell

The device efficiency is much lower than the record efficiency of 24.17% reported in a 2017 patent application for a crystalline InP cell [153]. This is due to both significantly lower J_{SC} and V_{OC} in the fabricated cell in this thesis. Table 3.2 compares the efficiencies and the following figures of merit for the thesis cell and the patent cell: J_{SC} , V_{OC} , and FF, which indicates how square the J-V curve is and is influenced by the series and shunt resistances in the device.

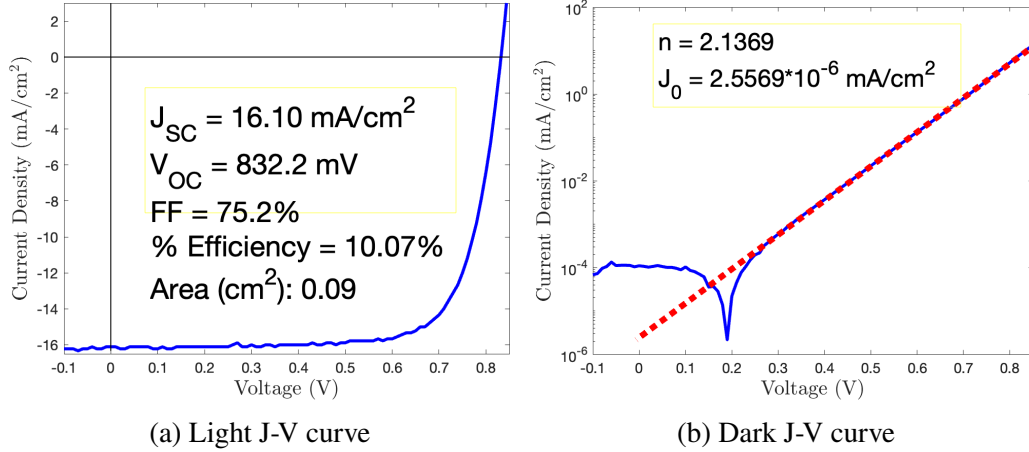


Figure 3.1: Dark and light J-V curves of the best MOCVD cell fabricated. No ARC was used.

The record planar patent cell [153] has a similar structure as the planar cells in this thesis, but with different doping concentrations and thicknesses. Table 3.1 compares the doping concentrations and thicknesses of the different layers in the thesis vs. patent cells. Note that the thicknesses are given in nm while the doping concentrations are given in cm^{-3} .

Cell	t_w	n_w	t_e	n_e	t_i	n_i	t_b	n_b	t_{BSF}	n_{BSF}
Thesis	30	$1\text{e}19$	50	$1\text{e}18$	1550	$1\text{e}17$	50	$3\text{e}17$	50	$2\text{e}18$
Patent	7	$2\text{e}19$	200	$8\text{e}16$	10	—	5000	$5\text{e}16$	100	—

Table 3.1: Thicknesses and doping concentrations of the different layers that are contained in both the thesis and the patent InP cells with an InAlAs BSF. The layer thicknesses are given in nm and the doping concentrations are in cm^{-3} .

Notice that in the patent cell, the window layer is thinner and more heavily-doped, the emitter is thicker and much more lightly doped, and the intrinsic layer is MUCH thinner and undoped, which makes it slightly n -type. However, the base is much thicker and more lightly-doped than in the patent cell than the thesis cell, while the InAlAs is a bit thicker and has no doping concentration listed. Since the patent cell is more than twice as thick as the planar cell fabricated for this thesis, because the goal for the thesis was to make a planar cell with comparable thickness as the NW heights, it makes sense that optimized parameters would be different.

The J_{SC} of the cell fabricated for this thesis is around half of that achieved in the patent cell, and its V_{OC} is over 100 mV lower than the patent cell's V_{OC} . The lower J_{SC} makes sense because the thesis cell's thickness is almost 3x thinner, so

Cell	% Eff	J _{SC} (mA/cm ²)	V _{OC} (mV)	FF
Thesis	10.07	16.10	832.2	75.2%
Patent	24.17	31.155	939.0	82.63%

Table 3.2: Figures of merit comparisons for the cell discussed in the thesis versus the record patent cell. This table reports the efficiencies, short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF).

in fact this illustrates the diminishing returns after increasing the thickness beyond a certain point. Additionally, it must be noted that the patent cells used a bilayer ARC made of ZnS/MgF₂, so the comparison of J_{SC} in particular is not an apples-to-apples comparison. The V_{OC} difference is notable, however, particularly because the patent authors also implemented an InAlAs back surface confinement layer and use a highly-doped front layer of InP, just like the thesis cells, and they cite the InAlAs layer as the source of significant V_{OC} improvement compared to the previous record set in 1990. Additionally, they note that their ARC lowers the FF by a few percent compared to the previous record cell, but it is still higher than the FF of the thesis cell. This is to be expected, though, given the higher V_{OC} of the patent cell.

The dark J-V curve of the patent cell is not provided, but the dark J-V curve of the thesis shows that the diode ideality factor is $n \approx 2.14$ after fitting a straight line to the logarithm of the dark I-V curve due to the equation

$$\ln \left(\frac{J}{J_0} \right) \approx \frac{qV}{nkT} \quad (3.1)$$

from which n can be estimated by performing a linear regression and extracting the slope of the J-V curve. The red dashed line in Figure 3.1b allows for the calculation of n . The diode ideality factor of $n \approx 2.14$ indicates that the recombination mechanisms in the device are largely limited by both carriers and include some combination of depletion region recombination and trap-assisted Shockley-Read-Hall (SRH) recombination, with some Auger recombination thrown in to spice things up [49]. The very neat linear fit of the dark log J-V curve indicates negligible leakage current and minimal shunting as well as minimal series resistance, meaning excellent metal contacts. Pathways for device improvement would include incorporating an ARC to improve J_{SC} and addressing the recombination mechanisms in this device.

3.4 Anti-Reflection Coatings (ARCs)

General Principles of ARCs

Semiconductors have rather reflective surfaces, which prevents a significant fraction of photons from even having a chance to get absorbed by the material to generate charge carriers and electricity. In the visible and near-IR (NIR) range, InP reflects 30-40% of the incoming photons at those wavelengths [55]. This suggests that an ideal ARC could improve the J_{SC} by at least 30%. ARCs rely on interference effects, and involve choosing materials with the right refractive indices and thicknesses [48]. Multi-layer ARCs can reduce reflection more than single-layer ARCs [118]. However, there are diminishing returns. This is especially true when considering parasitic absorption that prevents the non-reflected photons from being absorbed by the InP itself and the increased fabrication complexity.

Material Choice for ARCs

Depending on the wavelength range in which reflection reduction is desired, the optimal index of refraction for a single-layer ARC material ranges from 1.86-2.10 [48]. The bandgap of InP corresponds to a wavelength of 933 nm, so based on the index of refraction of InP at that wavelength [16], that would justify an ARC index of refraction of $n = 1.86$ [48]. This would give rise to materials such as Al_2O_3 , which has an index of refraction of $n \approx 1.62 - 1.65$ for thin films [29]. However, the greater reflection at shorter wavelengths ($\lambda \sim 400\text{nm}$) encourages an ARC index of refraction of $n = 2.10$ [55] [48]. This would favor a material like Ta_2O_5 , which has an index of refraction of $n = 2.06 - 2.20$ [22]. Previous work on planar InP has used Ta_2O_5 as an ESC combined with ITO to form an ARC on undoped InP to yield a solar cell with a 19.1% efficiency [90].

Titanium Oxide and Silicon Oxide ARCs

Other papers on InP solar cells commonly use ARCs that are at least 70 nm thick [165]. Thus, methods like e-beam evaporation and sputtering are needed to deposit materials. Since two-layer ARCs achieve better broadband antireflection than single-layer ARCs, and given the materials most readily available for deposition in the tools available, the thesis aimed for a TiO_2/SiO_2 two-layer ARC. PV Lighthouse's wafer ray tracer suggests that, for a single layer, Al_2O_3 performs better for antireflection on InP at shorter wavelengths than TiO_2 [74]. However, it performs poorer at longer wavelengths, and altogether PV Lighthouse predicts comparable performance in terms of predicted photocurrent generation based on the resulting InP

absorption after ARC use [74]. For these reasons, the thesis focused on depositing and optimizing TiO_2 and SiO_2 for ARC purposes.

To avoid wasting expensive InP substrate material that is more difficult to source than Si, many initial material depositions and measurements were run on silicon instead of InP. Then, a single-layer TiO_2 layer was attempted on an InP cell as an initial ARC test. Because of the experimental pitfalls along the way, further ARC work was set aside in favor of other optimization directions and diffusion doping work. However, future work can use a two-layer $\text{TiO}_2/\text{SiO}_2$ coating to further improve the J_{SC} . Because Ti_3O_5 was eventually used in place of TiO_2 , with oxygen flowed into the e-beam evaporator at a flow rate of 2 sccm to form TiO_2 via reactive evaporation, the ARC plots will label plots accordingly based on the choice of source.

Reflection Measurements

Figure 3.2 shows the reflection spectrum measured in the Cary UV-Vis spectrophotometer. The Ti_3O_5 layer is intended to be around 60 nm thick and the SiO_2 layer is intended to be around 100 nm. There is a discontinuity at around 800 nm in the

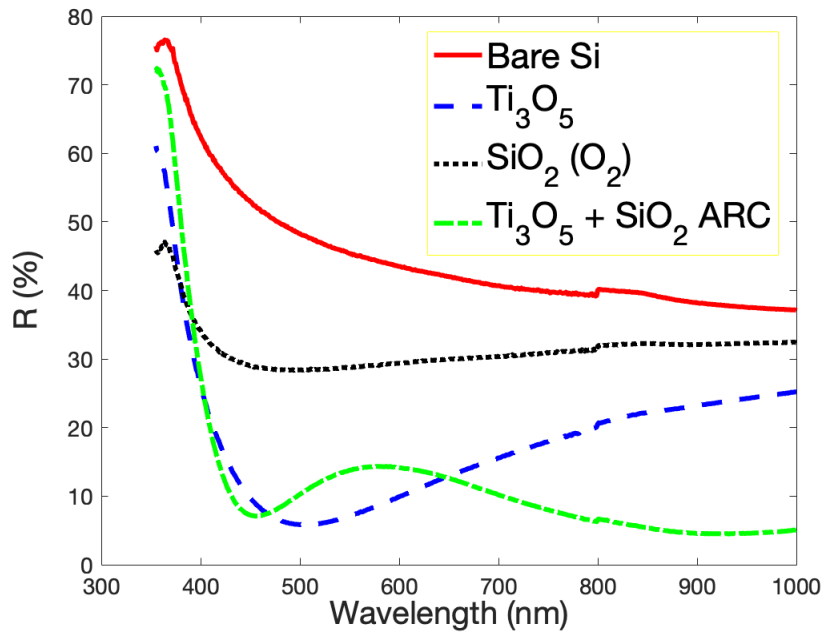


Figure 3.2: Reflection spectrum of bare Si, Si with Ti_3O_5 and SiO_2 as single-layer ARCs, and Si with both Ti_3O_5 and SiO_2 forming a double-layer ARC.

reflection spectrum because of a switch in detector type during the measurement across the spectrum. Though the system runs a calibration to attempt to address this, the calibration is imperfect.

Figure 3.2 shows that a single-layer Ti_3O_5 layer was a better ARC than a single-layer SiO_2 , and that a two-layer ARC achieves meaningful broadband reflection reduction, although the two-layer ARC exhibits worse antireflection at mid-range wavelengths ($\sim 450\text{-}650\text{ nm}$) than a single-layer Ti_3O_5 ARC. This illustrates how interference effects at these thicknesses can create non-linear effects in antireflection, and that "the whole is not simply a sum of its parts."

To execute intermediate steps well and understand performance improvements along the way before implementing more complex processes, a single-layer 60-nm TiO_2 was attempted on InP. Figure 3.3 shows the result: Its performance on InP is similar

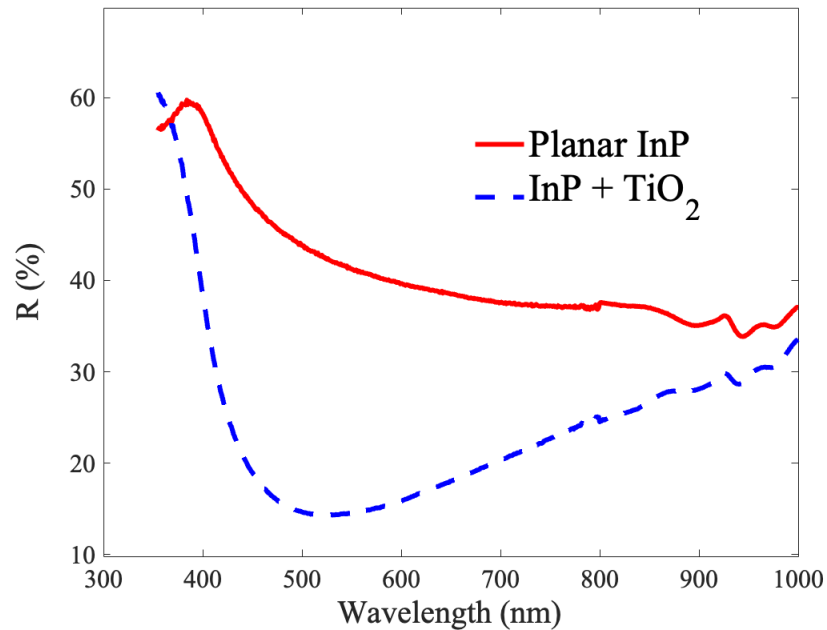


Figure 3.3: Reflection spectrum of bare InP and InP with TiO_2 as a single-layer ARC.

to that on Si. There is a bit more reflection at longer wavelengths in InP than in Si, which makes sense since InP has a higher bandgap, so more of the longer-wavelength photons are unable to be absorbed. Otherwise, however, the antireflection behavior of TiO_2 on InP was similar to its behavior on Si.

3.5 Predicting J_{SC} Enhancement with a $\text{TiO}_2 + \text{SiO}_2$ ARC

The enhancement of the J_{SC} due to an ARC can be predicted using Lumerical simulations to compare the J_{SC} with and without an ARC. These simulations account for the light absorption that occurs in the ARC and calculates the predicted J_{SC} from the generation rate profiles that result from the remaining light that makes it through the ARC. These simulations can be run with an AM 1.5G and an AM0 spectrum.

Table 3.3 illustrates the predicted J_{SC} for the cells with and without an ARC under both an AM 1.5G and an AM0 spectrum.

The ARCs used in these simulations include a 60-nm TiO_2 -only ARC, since that was the one tested experimentally, as well as the more ideal 10 nm TiO_2 layer paired with a 60 nm ITO layer, as used in some of the ESC cells reported in the literature [166]. When the ARCs were activated, a mesh override region was used to ensure that the 10 nm TiO_2 layer in particular was properly resolved in the mixed ARC. However, this override region was also used with the 60 nm TiO_2 ARC. The mesh override covered the entire ARC, with a maximum z mesh step size of 1 nm. When the ARC wasn't activated, the mesh was disabled to save simulation time.

Cell	J_{SC} (AM 1.5G)	J_{SC} (AM0)
No ARC	24.13 mA/cm ²	29.30 mA/cm ²
TiO_2 ARC	28.81 mA/cm ²	34.36 mA/cm ²
TiO_2 + ITO ARC	32.45 mA/cm ²	38.92 mA/cm ²

Table 3.3: Predicted J_{SC} in Lumerical on a thin-film planar InP with no ARC, a 60-nm TiO_2 -only ARC, and a 10-nm TiO_2 + 60 nm ITO ARC.

The table shows that there was a slightly proportionately larger improvement under the AM 1.5G spectrum than under the AM0 spectrum for both ARCs. However, both are in the same ballpark of 18.33% for the TiO_2 -only ARC and $\sim 33.66\%$ for the TiO_2 + ITO ARC.

3.6 Solar Cell Measurements With and Without an ARC

J-V Curves

Figure 3.4 compares the performance of a different fabricated cell with and without a TiO_2 ARC to avoid potentially ruining or destroying the best cell, especially because setting up the measurement involved maneuvering sharp probes in the dark at the surface. This was particularly the case because using the sample's actual reflectance spectrum instead of a generic reference InP reflectance spectrum was desired, and measuring that in the spectrometer risked damaging or cracking the sample during setup. Table 3.4 compares the figures of merit from the light and dark J-V curves of the two cells.

Even this single-layer ARC, which was not very broadband, boosted the J_{SC} by over 4 mA/cm², which represents over a 28.9% increase in J_{SC} . PV Lighthouse predicts that a 60-nm TiO_2 ARC on a standard 350 μ m InP substrate could boost J_{SC} from

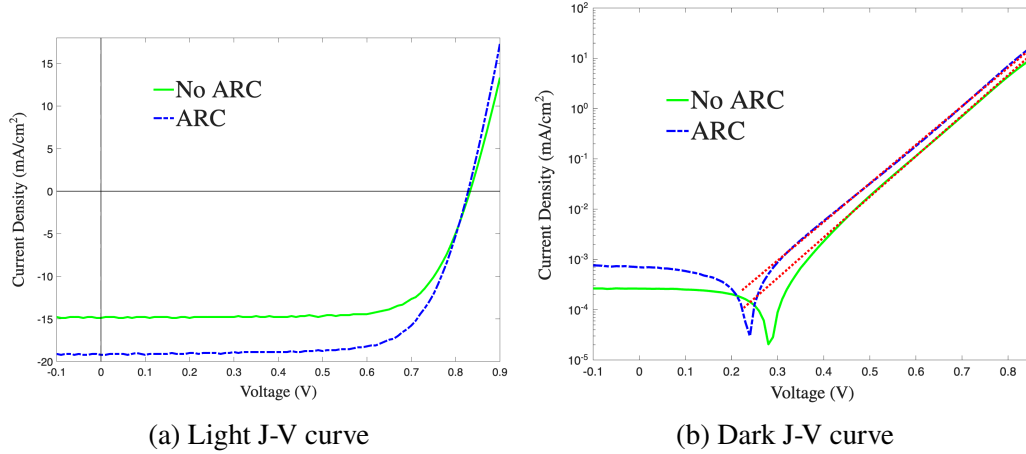


Figure 3.4: Light and dark J-V curves of an MOCVD cell with and without an ARC. The red dashed lines represent the slope of the log of the dark J-V curve to extract the value of n . The device area was 0.09 cm^2 .

Cell	% Eff	$J_{SC} \text{ (mA/cm}^2\text{)}$	$V_{OC} \text{ (mV)}$	FF	n	$J_0 \text{ (mA/cm}^2\text{)}$
No ARC	9.08	14.92	832.8	73.1%	2.14	$2.08 * 10^{-6}$
ARC	11.47	19.23	828.3	72.0%	2.19	$4.67 * 10^{-6}$

Table 3.4: Figures of merit comparisons for MOCVD-grown cells with and without a single-layer 60 nm TiO_2 ARC.

$\sim 24 \text{ mA/cm}^2$ to $\sim 32 \text{ mA/cm}^2$, which would be a 32% boost in J_{SC} . The actual J_{SC} boost is slightly less than the 34.5% improvement predicted by the 10 nm TiO_2 + 60 nm ITO ARC and even the 32% boost predicted in PV Lighthouse for the single-layer 60 nm TiO_2 ARC. This may be in part because the TiO_2 properties used in PV Lighthouse are for ALD-synthesized TiO_2 rather than evaporated TiO_2 , which would likely have different optical properties because of the speed, even-ness, and quality of deposition from the different deposition techniques.

Interestingly enough, the Lumerical simulations of the TiO_2 -only ARC predicted a 19.39% boost. This is likely reflective of the material properties of the TiO_2 layer as modeled in Lumerical. The FDTD model does not match the data for the n (real) index of refraction given for the " TiO_2 - Ioffe" version of TiO_2 provided by Lumerical, particularly at longer wavelengths. This illustrates how important it is to get realistic, experimental refractive index data for optical modeling. The material properties were optimized for good fitting of the k (imaginary) index of refraction to ensure the absorption was accurately captured, but the misfitting of the n values means that interference effects might not be accurately captured, especially at longer wavelengths.

However, despite this, the single-layer TiO_2 ARC in this work achieves a significant fraction of the simulated J_{SC} boost predicted.

Similar to the patent cell versus the previous record planar InP cell from the 90s, the V_{OC} and FF mildly drop after the deposition of the ARC compared to the bare InP cell. The dark J-V curve, which illustrates a slightly higher n value and dark short-circuit current density J_0 for the cell with the ARC than without, confirms that the ARC does worsen the surface a little and increase recombination. However, the J_{SC} boost more than compensates for these reductions to yield an overall efficiency improvement of 26.3% through the use of an ARC.

This shows the promise of an ARC in improving device efficiency. Future work can use two-layer ARCs to further improve light capture and device efficiency by better reducing reflection across a broader portion of the spectrum.

EQE Measurements and Extracted Parameters

EQE measurements were taken for this MOCVD cell with and without an ARC. The EQE measurement, combined with the reflectance spectrum, will yield the cell's internal quantum efficiency (IQE), which provides information about the carrier collection of the absorbed photons. Effectively, it is the EQE assuming complete absorption, with no reflection or transmission. Sze and Ng derive the IQE, which they refer to as the spectral response, of a simple p-n junction solar cell in terms of material and device parameters such as minority carrier diffusion length, diffusion coefficient, surface recombination velocity, absorption coefficient, minority carrier lifetime, base and emitter widths, and depletion width. These, in turn, depend on doping concentrations in the different layers [121]. Known values can be used to extract device parameters such as carrier lifetime and diffusion lengths using Mathematica or Python. The fits presented in this thesis were obtained using a Mathematica script initially written by Philip Jahelka and modified to include the full model as presented in Sze and Ng [121].

Defining Parameters

Because parameters such as diffusion coefficient would depend in part on material quality, and the solar cell structures here are not simple p-n junctions but have multiple p and n-doped layers with different widths and doping concentrations, these parameters should not be hard-coded into the model. Instead, they should be used as starting points, but a reasonable range should be permitted to balance

physical realism of the parameters with fit to real-world device data. For instance, since the device has a heavily-doped window layer in addition to an emitter layer, the fitted emitter width W_e was allowed to be between 30-80 nm, with the 30 nm reflecting the width of the window layer and the 80 nm reflecting the combined width of the emitter and window layers. Similarly, the base H was allowed to range from 1.5-8 μm based on the widths of the p-type layers. It seems that the upper end for H needs to be increased beyond the 1.7 μm that represents the physical thickness of all the p-doped layers to avoid the fitting script pushing up against a 1.7 μm upper limit. This suggests that the multiple p-doped layers and the InAlAs BSF has the same effect as a longer p region in a simple p-n junction cell.

The depletion region width W_d was allowed to range from 30-140 nm since the minimum p and n dopings are 10^{17} and 10^{18} cm^{-3} , respectively, while the highest are $2 * 10^{18}$ and 10^{19} cm^{-3} , respectively [119].

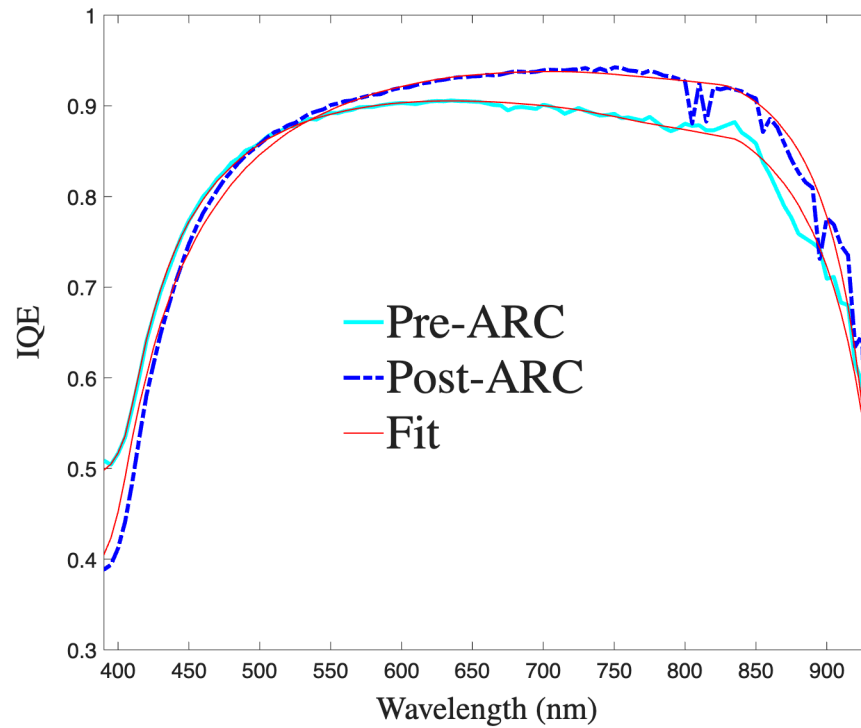


Figure 3.5: IQE curves of the measured MOCVD planar cell with and without a single-layer 60 nm TiO_2 ARC. The IQE fits are plotted in thin red solid lines.

Figure 3.5 presents the experimental IQE based on the measured EQE and measured reflectance spectrum of the InP used, as well as the fitted curve using the Mathematica script and the spectral response model presented in Sze and Ng's book [121]. Table 3.5 presents the key fitted parameters based on the Mathematica script: surface

Parameters	Pre-ARC	Post-ARC
SRV (cm/s)	$9.76 * 10^6$	$1.34 * 10^7$
L_n (μm)	1.36	1.54
L_p (μm)	3.30	0.602

Table 3.5: Extracted parameters from I-V and QE measurements. The table reports the SRV and carrier diffusion lengths.

recombination velocity (SRV), electron diffusion length (L_n), and hole diffusion length (L_p). The model registers the emitter width as ~ 30 nm for the pre-ARC cell and ~ 42 nm for the post-ARC cell, which means it is mostly registering the window layer as the equivalent of an emitter in a simple p-n junction cell. H is fitted to be $3.79 \mu\text{m}$ for the pre-ARC cell and $\sim 7.97 \mu\text{m}$ for the post-ARC cell, which is more than the thickness of all the p -type layers combined. The depletion width W_d was still restricted to remain in the 130-140 nm range based on the doping concentrations $n_e = 10^{18} \text{ cm}^{-3}$ of the n -type emitter and $p_i = 10^{17} \text{ cm}^{-3}$ as the p -type intrinsic region as shown in Figure 2.13a. The script pushed $W_d \rightarrow 130$ nm, which suggests that the model would predict a lower depletion width if permitted. This is surprising since lower depletion widths come from higher doping concentrations, while the substrate on which the cell is grown is undoped.

Because convergence of the model and the fitted values can depend on the parameter ranges specified, the thesis will include the ranges used for various parameters in the model from Sze to assist with reproducibility [121]. Table 3.6 includes these ranges for the pre-ARC and post-ARC cases. $K_p \equiv S_p L_p / D_p$ and $K_q \equiv S_q L_q / D_q$

Parameters	Pre-ARC	Post-ARC
c	0.99-1.04	0.99-1.09
H	1.5-8	1.5-8
W_e	0.03-0.08	0.03-0.08
L_n	0.001-5	0.001-5
L_p	0.1-20	0.1-20
W_d	0.13-0.14	0.13-0.14
K_p	0.1-1000	0.1-1000
K_q	0.1-1000	0.1-1000
$ d\lambda $	10.5	3.5

Table 3.6: Parameter ranges for the IQE model in Sze to fit the IQE curves for the pre-ARC and post-ARC cells.

are defined in terms of the surface recombination velocity S , diffusion coefficient D , and diffusion length L for holes and electrons, respectively. The subscript q is

used in place of e because Mathematica seemed to throw a fit when e was used as a subscript. These definitions are used since those terms show up several times in the mode.

Prefactor c and Offset $d\lambda$

The model also includes a prefactor, c , that multiplies the model to scale the modeled IQE to the experimental IQE, as well as a wavelength shift $d\lambda$, that reflects a discrepancy between the detector's measured wavelength and the "actual" wavelength. Phil mentioned that the monochromator had an offset of 7 nm, so ideally the $d\lambda$ should have a magnitude less than 3.5. The fitted values of c are 1.02 and 1.08, respectively, for the pre-ARC and post-ARC case, while the $d\lambda$ fitted values are 10.3 nm and 3.48 nm, respectively. Some of these values are rather high — previous uses of this script had restricted c to remain between 0.99 and 1.01, while it restricted the magnitude of $d\lambda$ to be less than 3.5 nm. This means that the "pure" model predicts IQE values that are 2-8% lower than the real values and a spectrometer offset of up to ~10-ish nm.

This is likely because the IQE model is a simplified one for a simple p-n junction. On the other hand, this cell is a more complex heterostructure, with multiple p and n-type layers with different doping concentrations and a heterostructure with a layer — InAlAs — that has a different composition and bandgap than the rest of the cell. In particular, the n -type region has a thin, heavily-doped window layer on top of a lightly-doped, slightly thicker emitter layer. It also has a four-layer p-type region with different thicknesses and doping concentrations, including an InAlAs layer with a higher bandgap that can reflect electrons back into the p-InP layers. Because the rest of the model does not fully capture the effects of this more complicated heterostructure, such as the carrier reflection due to the InAlAs BSF and the built-in fields from the varying carrier concentrations, these effects are likely being folded into the values of c and $d\lambda$. Additionally, the increase of the fitted L_n between the pre-ARC and post-ARC cases does not make sense. However, the decrease in L_p between the pre-ARC and post-ARC cases can be explained by surface damage to the n -type layers after ARC deposition, which may also be penetrating the surface and affecting the top n -type layers.

Device Performance Analysis

Nonetheless, the fitted parameters provide a starting point to understand and confirm some key aspects of device understanding. The increase in SRV from the pre-ARC to post-ARC case confirms the observation from the light and dark J-V curves, based on the V_{OC} and J_0 values, that there is more recombination after the ARC is deposited than before. These values are significantly higher than the low SRVs (500 cm/s) observed in p-type and n-type InP, so there is likely room for improvement in device SRV even if the fabrication process might degrade the SRV. Note that SRV indicates the propensity for surface recombination, so lower SRVs are desirable. However, any passivation methods used must be careful not to etch the InP because the top window layer is quite thin — only 30 nm — and etching away this window layer would affect the resulting performance since the cells were optimized to have a window layer of 30 nm.

The cell exhibits broadband carrier collection of absorbed photons, especially within the 500-850 nm wavelength range. The spectral response drops off sharply at wavelengths shorter than ~ 450 nm and wavelengths longer than ~ 850 nm. The lower spectral response at shorter wavelengths is likely due to the absorption of the photons in the *n*-type layers before reaching the p-n junction to be absorbed and collected for useful electricity generation. Meanwhile, the drop off in the spectral response at longer wavelengths is likely because those wavelengths are still shorter than the thicknesses of all the p-type layers combined as well as the lower fitted L_n values than the L_p values. The L_n values in both cases are shorter than the thickness of the *p*-doped region of the device, which suggests that the electrons are not being captured effectively at the rear of the device. Literature measurements show that L_n can be as high as 5 μm even in a *p*-type layer with a doping concentration of $3 \times 10^{18} \text{ cm}^{-3}$, so there is likely room for improvement for the electron diffusion length in these devices [92].

Takeaways: ARCs versus No ARC

Nonetheless, the ARC boosts spectral response at mid and long wavelengths. This could be because the ARC could enhance photon recycling by reflecting photons generated within the device from radiative recombination, increasing the probability that they are re-absorbed by the device and able to be collected rather than escaping the device. The ARC can also increase the optical path length of photons that manage to enter the device in general, since now there is a front layer in addition to

the back metal layer that reflects photons back into the device. However, the overlap of the pre-ARC and post-ARC spectral responses at shorter wavelengths below 500 nm suggests that the enhanced photon recycling plays a stronger role. This is because optical path length enhancement should help photons of all wavelengths, but the photons generated from radiative recombination would be closer to the InP bandgap, which corresponds to $\lambda \approx 922$ nm, so enhanced photon recycling would favor enhancement of long-wavelength photon collection. This is what is observed in the IQE graphs.

Altogether, despite the increased recombination due to surface damage from the ARC, the antireflection effects and carrier collection enhancement due to the ARC more than compensate, yielding significant device efficiency improvement.

3.7 Ohmic Contact Resistivity

Background

Ohmic contacts are interfaces between a metal and a material that permits electricity flow, such as another metal or a semiconductor, that exhibit a linear current-voltage (I-V) relationship and low resistance compared to the bulk device resistance [136]. In solar cells, ohmic contacts facilitate effective carrier collection or injection [136].

Factors that influence ohmic contact formation include semiconductor doping, Schottky barrier height, and tunneling versus thermionic emission [136]. Higher-doped semiconductors yield narrower depletion regions and lower potential barriers, which leads to lower contact resistances [136]. This in part motivated the highly-doped n-type window layer, especially since the top surface requires grid contacts, which means less metal is used [136]. This necessitates low-resistance interfaces. Tunneling emission is the main conduction mechanism between metals and heavily-doped semiconductors because of this narrow depletion region [136]. Moderately-doped semiconductors, on the other hand, exhibit thermionic emission and rely on there being sufficient thermal energy to overcome the conduction band barrier [136].

The Schottky barrier height is influenced by the work functions of the metal and semiconductor in question [136]. n-type semiconductors prefer metals with low work functions, such as aluminum or titanium, to facilitate electron transport via a low Schottky barrier height [136]. Meanwhile, p-type semiconductors prefer metals with higher work functions, such as gold or platinum, for better hole injection [136]. However, other factors can also come into play. For instance, InP has a high electron

affinity, which makes it challenging to achieve low-resistance ohmic contacts. In practice, factors such as interface contamination, intervening insulating layer, edge leakage current, or deep impurity levels cause real-world ohmic contact options to deviate from that which would be predicted by Schottky barrier calculations based on the semiconductor's electron affinity and the metals' work function [120].

Contact Annealing

Some metal stacks need to be annealed post-deposition to create ohmic contact with the semiconductor surface [136]. This promotes interdiffusion between the metal layers involved and the semiconductor, which can in turn reduce contact resistance [136]. There are several charts out there providing a detailed list of various possible ohmic contact metal stacks and annealing conditions [155] [68]. In line with the earlier discussion on doping concentration and the formation of ohmic contacts, these tables provide doping concentrations along with type, annealing temperature and time, and specific contact resistance [68]. Though these charts have reported on several In-based ohmic contacts, in which the In was used as a wetting layer for good adhesion [155], much of the literature reporting on ohmic contacts focuses on other metal stacks that do not contain In, like nickel for n-InP [26] and Au-Zn for p-InP [47]. This is in part because In has a relatively low melting point of 156.6°C, which can cause problems in later high-temperature processing steps, especially for p-type Ohmic contacts, which need to be annealed at temperatures of 375°C and higher [69].

Anneal Temperatures

Specific contact resistivities for solar cells have been measured in the 0.02-0.03 Ω cm² using Ag electrodes on the front of Si solar cells [87]. However, these cells were fired at temperatures of 840°-960°C, which would be undesirable for InP cells. This is because of its own lower melting point compared to Si, the high vapor pressure of P in particular compared to Si, and the rapid diffusion of dopants like Zn. Thus, it was challenging to achieve low specific contact resistivities. This will be discussed more in the Appendix. In the MOCVD cells, the n-type layers are also less than 100 nm thick, which means it is crucial that the annealing process does not force the metal atoms deeply enough into the device to puncture the p-n junction. This is particularly a problem for Au-based contacts to p-InP [47]. Another challenge with ohmic contact formation was the annealing atmosphere, which will also be described in greater detail in the Appendix. In short, however, much of the initial annealing —

including for the specific resistivity measurements — was performed in a glovebox, which made sample manipulation in an inert atmosphere challenging. This made rapid anneals less than 1 minute difficult to implement in practice. Though those working on materials like GaAs have low-temperature options available, such as a 2-hour tube furnace anneal in forming gas at 180°C, achieving ohmic contact to InP at temperatures below 300-350°C seems challenging, which can cause problems with dopant diffusion in the MOCVD cells with thin n-type layers and the diffusion-doped cells.

Transfer-Length Method Measurements

For initial solar cell work presented in this thesis, transfer-length method (TLM) measurements were taken to understand the starting point for the fabricated devices and the extent of the room for improvement [50]. The main aim was to also check for ohmic versus rectifying behavior in the contact resistivities. However, reducing the contacts' specific resistivities will be reserved for future work. Additionally, since p-type InP wafers from University Wafer, with a doping concentration of $4\text{-}5 \times 10^{18} \text{ cm}^{-3}$ were used for TLM measurements due to availability at the time of purchase, the resistivities measured for the n-type metal stacks on p-InP will likely be higher than what would be measured on wafers being used for solar cell devices, where they would be contacted to n-InP. These measurements can be useful to investigate the impacts of contact annealing, however, since annealing improves the contact between the metal and semiconductor surface and helps reduce surface defects via semiconductor atom migration. These effects should be independent of the doping type. As long as rectifying behavior was not observed, future work can focus on optimizing anneal conditions and metal layer thicknesses, if needed, to achieve better contact resistivities to improve device performance.

Ag-Zn-Ag for p-InP and Ni-Ag for n-InP

The baseline contacts used were Ag-Zn-Ag for p-type InP and Ni-Ag for n-type InP [47] [26]. Because some of the references did not provide % weights for the Zn or Ni [51], equal thicknesses of 50 nm for each metal were used as starting points for the contact compositions. Though much of the literature annealed p-InP Zn-based ohmic contacts at temperatures at or above 400°C, this work found that a 375°C anneal for 5 minutes achieved non-rectifying ohmic behavior. The work on Ni-based n-InP contacts by Erickson et. al. illustrated the lowest contact resistivity on the order of $10^{-5} \Omega \text{ cm}^2$ being achieved for a 5-minute anneal at 325°C, with

the resistivity rising almost an order of magnitude but still remaining below $10^{-2} \Omega \text{ cm}^{-2}$ [26]. Thus, previous literature work suggests that a single, 375° C anneal after depositing both front and back contacts can achieve a sufficiently good ohmic contact while limiting the heat exposure of the devices.

The TLM measurement procedure and logic is explained in [50]. Figure 3.6 shows the TLM mask used to deposit metal strips on the semiconductor samples. The masks were cut from kapton, which allows patterning by securing the mask and the sample to the evaporation apparatus — either in the e-beam evaporator or the thermal evaporator — and avoided the time and resource-intensive alternative of using photolithography and commissioning a photolithography mask. The distance between the strips is varied from 0.5 mm to 2 mm. Placing probes on non-adjacent strips increased the number of distances that could be measured, increasing the number of data points — possible distances that can be measured include 2 mm, 3 mm, and more. The results of the TLM measurements are presented in Figure 3.7

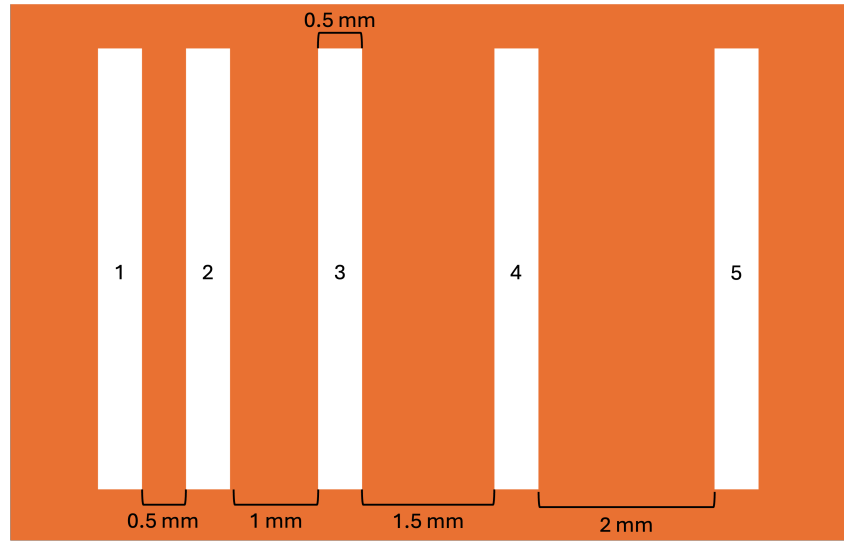


Figure 3.6: Schematic of the TLM mask cut from kapton. Each of the strips is 0.5 mm wide, and the distance between adjacent strips varies from 0.5 mm to 2 mm.

for Ag-Zn and Ni-Ag contacts. I-V measurements were taken with two probes, with one probe on each strip (e.g. 1 and 4). The further the metal strips are from each other, the more likely the I-V curve is to be non-linear, so attempts were made to fit and measure strips as far apart from each other as possible, limited by the size of the diced InP chips. The Ag-Zn results presented in Figure 3.7 were annealed at 375° C for 5 minutes, but the Ni-Ag contacts presented in that figure were not annealed.

The chip sizes were not all uniform since they were diced by hand. Thus, the heights of the bars were not all the same, and they were estimated. As a result, the specific resistivities listed should be taken as approximations. The specific resistivity $\rho_{\text{Ni-Ag}}$ of the Ni-Ag contact is higher than that of the Ag-Zn contact, $\rho_{\text{Ag-Zn}}$. This is expected since Ni-Ag is ohmic to n-InP, not p-InP. While lower resistivity is desired for concentrator cells, $1 \Omega\text{cm}^2$ suffices for solar cells with a light intensity of 1 sun shining on them.

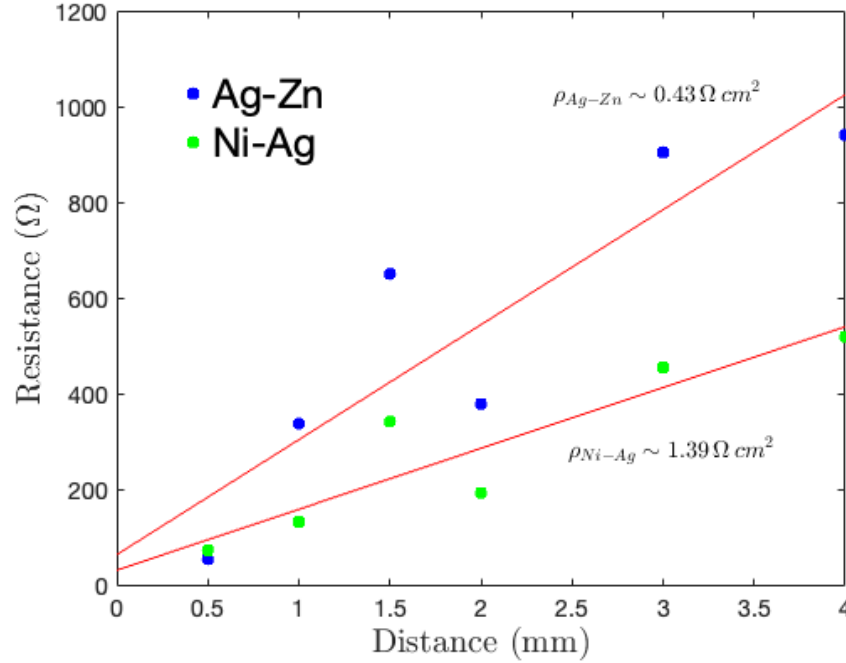


Figure 3.7: I-V curves measuring the current between two strips of metal in TLM measurements on Ag-Zn and Ni-Ag contacts to p-InP.

To confirm ohmicity of the contacts, albeit with high specific resistivities, Figure 3.8 presents the I-V curves of the same strips of Ag-Zn and Ni-Ag on the p-InP wafers measured. Only one pair for each was chosen to be plotted — the pair furthest apart on the sample, to best detect any non-ohmicity that might exist. The Ag-Zn strips were 4 mm apart, while the Ni-Ag strips were 5.5 mm apart. Linear fits are shown in red dashed line to illustrate the extent of deviation from a linear I-V curve for each. The Ag-Zn I-V curve is linear, but the Ni-Ag one is not. This is to be expected, since the Ni-Ag contacts were deposited on p-InP but it is ohmic on n-InP.

Alternative Ohmic Contact Measurements

Several other alternatives were attempted, either to see if better contact resistivities could be achieved or whether lower-temperature anneals were possible. Figure

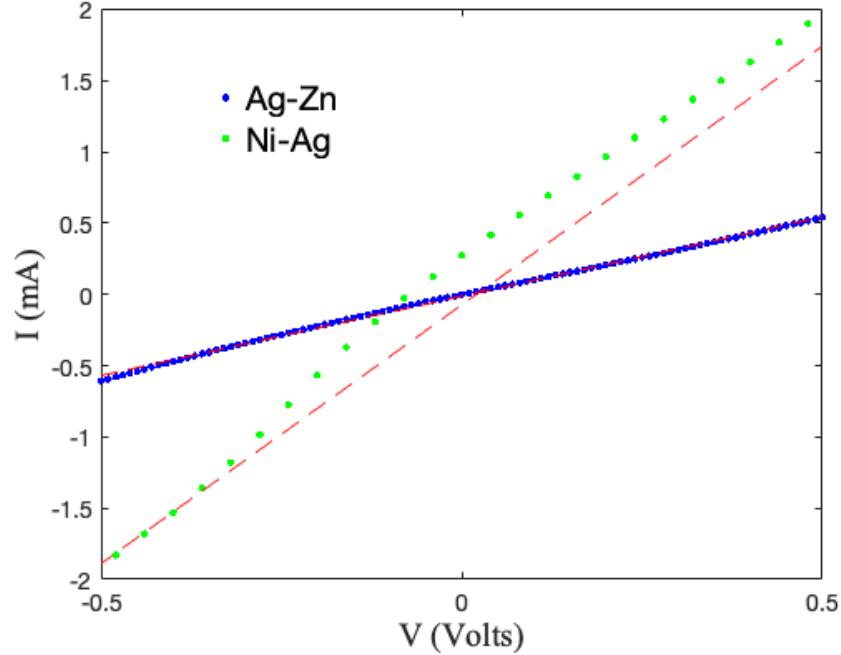


Figure 3.8: I-V curves of the Ag-Zn and Ni-Ag TLM measurements. The Ag-Zn strips are 4 mm apart while the Ni-Zn strips are 5.5 mm apart. The red lines plot linear fits to each.

3.9 illustrates plots of these I-V curves and linear fits to demonstrate the extent of ohmicity — or lack thereof — achieved by these contacts. The Pd-Ag-Zn and Ag-only contacts were intended to be ohmic for p-InP, and was annealed overnight at 200°C. The Pd-only and Ni-Ge-Au contacts were annealed for 10 s at 400°C. The Ag-only and the Pd-containing contacts exhibit visibly non-linear I-V curves. The Ni-Ge-Au, which was intended to be an n-type ohmic contact, performs the best even on p-InP, but its TLM resistivity had been calculated to be $\rho_c \approx 1.37 \, \Omega \, \text{cm}^{-2}$, which was comparable to that of Ni-Ag alone, so sticking to the simpler Ni-Ag should suffice.

Thus, these contact attempts demonstrate that, at least for trials thus far, Ag-Zn-Ag and Ni-Ag are sufficiently good starting points for ohmic contacts to InP. However, to improve contact resistance, future efforts can work on implementing rapid thermal annealing or trying furnace-based anneals to achieve lower specific contact resistivities. For instance, a book on doping in III-V semiconductors reports that a typical alloying cycle for AuZn contacts with 5% weight Zn on GaAs only requires a 20s anneal at 380°C. Future work can explore whether a similar rapid thermal anneal could work on InP [115].

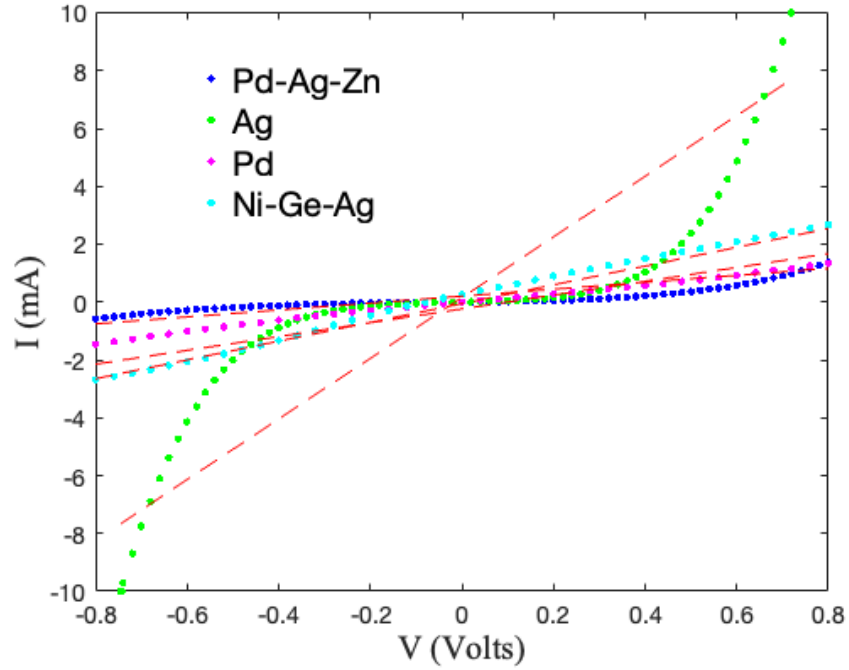


Figure 3.9: I-V curves of the Pd-Ag-Zn, Ag, Pd, and Ni-Ge-Ag contacts. The red lines plot linear fits to each.

3.8 Conclusion

Light and Dark J-V Curves

The work on the epitaxial planar InP solar cells establishes a solid foundation upon which to build for future work, both in this thesis and beyond. It investigates the figures of merit from factory-grown optimized epitaxial cells, illustrating the extent to which experimental results deviate from computational models and establishing a baseline against which to compare thin-film and diffusion-doped cells with our fabrication processes. The efficiencies deviate from the record planar cell reported due in part to an active region that is half as thick and parameters that were optimized accordingly. The dark J-V curves indicate that depletion region and trap-assisted SRH recombination are the primary mechanisms that likely need to be mitigated in these cells and throughout the fabrication process to improve device efficiency. ARCs, even simple ones, were shown to enhance J_{SC} and overall device efficiency even at the expense of slightly-increased recombination. J-V curves and EQE measurements suggest this is due to increased carrier absorption from the antireflection effects as well as increased photon recycling and optical path lengths that enhance longer-wavelength carrier collection in the device in particular.

Improvements: ARCs and Ohmic Contacts

Reflection measurements on Si illustrate the potential that a double-layer ARC would have to further enhance these improvements, though the EQE measurements illustrate the room for improvement in addressing device recombination via improved surfaces. The low electron diffusion lengths suggest that despite these wafers being factory-commissioned, there might be room for improvement in the device quality within these devices, although more experimental and characterization work would be needed to say for sure. For instance, TRPL measurements could be used to measure the minority carrier lifetimes at play. Lastly, ohmic contact resistivity tests confirm that, with the materials available and the desire for low-cost, widely-available materials throughout the fabrication process, Zn-based contacts, paired with Ag and / or Au, are necessary to make proper ohmic contact to p-InP. It is also necessary to anneal them at a temperature of at least 375°C to achieve ohmic contacts — unannealed contacts will not be ohmic. However, for contact to n-InP, Ni-Ag suffices, and annealing is not as crucial. Alternative contacts do not seem to show sufficient superiority in these studies, but further studies on n-InP or undoped InP (which is slightly naturally n-type), with a rapid thermal annealer or detailed furnace trials, may be useful for further confirmation. Along the way, valuable experimental challenges and troubleshooting tips were also discovered, which are detailed more extensively in the Appendix.

This sets the stage in future work for a baseline of inherent wafer and device quality from a high-performance epitaxial growth process, particularly for devices of the desired 1-2 μm thickness, the improvement potential and drawbacks from ARC usage, and the possible ohmic contact choices as well as realistic resistivity improvements from different metal combinations.

Future Work

While most of the future work will focus on diffusion-doped thin-film cells, some studies on MOCVD-grown cells can still be beneficial to establish a baseline, compare p^+n cells with n^+p cells, and get to radiation hardness testing quicker since the cells will likely start higher-efficiency than their diffusion-doped counterparts. The following are future studies that can be done with MOCVD-grown wafers to achieve thin-film, radiation-hard cells, not just improve performance:

- Spalling the MOCVD-grown InP wafers and fabricating solar cells out of them.

- Given the higher efficiency achieved with the MOCVD wafers, these cells would serve as a baseline for spalled InP cell efficiency.
 - This would also give an idea of how good n^+p spalled cells could get compared to p^+n spalled cells made from diffusion doping.
- Radiation hardness testing of spalled MOCVD solar cells
 - Since the MOCVD cell fabrication should yield higher-efficiency cells, it should be quicker to test the radiation hardness of spalled MOCVD cells than spalled diffusion-doped cells.
 - This would also give an idea of the radiation hardness of n^+p spalled InP cells.
 - Electron and proton irradiation should both be tested if possible.

Chapter 4

DIFFUSION DOPING METHODS

4.1 Background

As explained in Section 1.3, diffusion doping is the most commonly-used commercial method for creating p-n junctions in solar cells. They are used in commercial crystalline silicon solar cells [67] [159].

Compound semiconductors face challenges in diffusion doping compared to Si for several reasons. For starters, the As in GaAs and the P and InP have higher vapor pressures than Ga and In, respectively [85]. This means that the temperatures needed for diffusion would often result in the loss of the more volatile material [85]. Special care is often needed to counter the loss of said volatile elements from the semiconductor sample being doped [85]. For the diffusions conducted in this thesis, Cd_3P_2 and Zn_3P_2 powders are used as diffusion sources, instead of elemental Cd and Zn, to provide enough phosphorous partial pressure to counteract the P outdiffusion from the sample.

Justification for Doping versus Carrier Selective Contacts

A functioning solar cell requires, broadly speaking, the separation of positive and negative charges. This must be done in such a way that electrons have to pass through the solar cell and the device being powered in order to reach the positive terminal and vice versa for holes reaching the negative terminal. Doping is one way to achieve this. Using carrier selective contacts is another, as demonstrated in [90] and [165]. Since ALD can be scaled for industrial use, and the carrier separation occurs at the interface, this carrier selective contact structure is feasible for scalable solar power [150]. The sharp interface at which the carrier separation occurs in these cells also means that the InP substrate can be as thin as desired, contingent on the limitations of thin-film fabrication methods such as spalling.

However, diffusion doping has some likely advantages over the carrier-selective contact approach, especially for space solar cells. Notably, space radiation creates defects in the semiconductor material, which will reduce the carrier lifetime and diffusion lengths within. Diffusion-doped junctions, with their tapering doping profiles, give rise to a relatively extensive built-in field that separates charge carriers via

drift rather than blocking majority carriers at the carrier selective contact interface. A large built-in field relative to zero-field regions means that carriers do not have to rely as much on diffusion to reach the desired contacts. This means the lower diffusion lengths in solar cells damaged due to space radiation would likely have less of a negative impact on the performance of diffusion-doped solar cells than on the carrier selective contact cells. Though this should be experimentally verified, especially in thin-film cells where the diffusion lengths might not be as strong a limiting factor in cell performance either way, it motivates the thesis choice to focus on diffusion doping, and leave further carrier selective contact efforts to future work. Additionally, NREL work has discussed the improved radiation resistance that results from graded doping, which diffusion doping naturally achieves [102].

Dopant Options

In general, the following dopants have been reported in the literature to act as acceptors: Be, Mg, Zn, Cd, and Hg [115]. Be and Zn are also used for ohmic contact metallizations to p-InP [115]. In practice, however, Be and Mg readily form oxides at high temperatures, and BeO is toxic, while MgO can lead to electrical inactivation. Thus, Be is often not used in practice, and Mg would require careful processing. Hg has a high vapor pressure, as well as a higher ionization energy than many other donors, which makes then unviable as donors [115]. This leaves Cd and Zn as p-type dopants, especially for diffusion doping.

Meanwhile, the following have been reported to act as donors: Si, Ge, Sn, S, Se, and Te [115]. In practice, Si incorporated into InP substrate wafers via LEC during ingot growth only achieves electron concentrations on the order of 10^{16} cm^{-3} [144]. This is on par with undoped InP, which naturally skews n-type [144]. Ge exhibits extensive self-compensation in InP, even at high doping concentrations [133]. This phenomenon occurs in compound semiconductors when a material compensates for dopants of one type (n or p) by adjusting to these impurities to create defects of the opposite type. This compensation makes Ge a less effective and desirable n-type dopant compared to the alternatives. However, AuGe with 12% weight Ge is used as an ohmic contact to n-InP, with a 20 second anneal at 420°C [115]. Strong redistribution of Sn at high temperatures and kinetic limitations at low temperatures limit their use as dopants for III-V semiconductors [115]. Te atoms diffuse fast, and their effective incorporation into III-V semiconductors is very dependent on growth conditions, which generally makes Te impractical as an InP dopant [21]. In practice, S is the most common n-type dopant for InP, and can be used to dope InP during

crystal growth, epitaxial growth, or via diffusion [154] [78] [38].

In short, this leaves Zn and Cd as the most viable dopants for diffusion doping to create p-InP and S as the most viable dopant for diffusion doping to create n-InP.

p⁺n versus n⁺p Structures

To make a diffusion-doped solar cell, one can either start with an n-type InP wafer and create a p-doped emitter or start with a p-type InP wafer and create an n-doped emitter. Previous work on diffusion-doped solar cells has suggested that p⁺n thermally-diffused structures could achieve higher maximum efficiencies than n⁺p structures [36]. This was based on their measurements of Cd-doped n-InP cells compared to their experimental projected maximum V_{OC} , and the team predicts this is because of the large number of defects present after n-type doping of p-InP [36]. Their work's preliminary irradiation measurements also suggest that p⁺n cells hold up better for Cd-doped cells than n⁺p cells with cadmium-doped substrates, but that p⁺n Zn-doped do worse than both [36].

Sulfur versus Zinc versus Cadmium

Other work has illustrated that shallow junctions are easier to fabricate with sulfur (S) doping of p-InP instead of Zn or Cd doping of n-InP [35] [141]. For low-doped n-InP substrates, Cd diffused over 2 μm into the surface in 1 hr at 575°C while S diffused less than 150-200 nm into low-doped p-InP even at temperatures above 600°C and diffusion times from 1-3 hours [35] [141]. This may be in part because at the high diffusion temperatures needed for S, an oxide layer formed despite surface pre-treatment before diffusion that may serve as a barrier against In or P outdiffusion [35][141]. However, S doping of p-InP requires a separate source of P, such as red phosphorous, to compensate for the outgassing of P from the InP sample [35]. Meanwhile, Cd_3P_2 or Zn_3P_2 can be used for p-type doping to achieve the same, reducing the number of materials and sources of error in experimental execution. Using Cd_3P_2 and Zn_3P_2 instead of elemental Cd and Zn also reduced surface pitting and improved diode quality [31].

Preliminary work on diffusion doping in InP suggests that Cd is a better p-type dopant choice than Zn. Not only does it have a lower diffusion coefficient in InP than Zn, allowing for shallower junctions, but Cd also seems to exhibit greater radiation hardness than Zn [156] [36]. The effect of using Cd versus Zn as the p-type dopant, whether in the emitter or the substrate, seems to override the choice

of p^+n versus n^+p for both the projected maximum efficiency and the radiation hardness [36]. This may be in part because Zn seems to generate more dislocation densities than Cd if the samples are subject to high-temperature processes after the p-type dopant is incorporated, which makes sense given the greater diffusion coefficient of Zn [35].

However, Zn cells still have room for improvement compared to what was reported in the literature. This is because a post-diffusion anneal can increase the effective carrier concentration of the p^+ Zn layer [147]. Without this anneal, the electric charge carrier concentration of the holes is up to an order of magnitude lower than the physical dopant concentration [147]. Zn is also less toxic than Cd, further motivating its use, especially when considering end-of-life disposal along with minimizing toxic exposure during initial fabrication. Thus, this work explores diffusion doped cell fabrication with annealed Zn diffusions and compares them to Cd-doped cells.

Dopant Diffusivity

As will be discussed in the next section, Zn diffuses more readily in InP than Cd, while S doping requires much higher temperatures compared to Zn and Cd doping [35] [141]. This means that creating an n^+ layer on a p-doped substrate could potentially cause the p-type dopants to shift around and create defects compared to creating a p^+ layer on an n-doped substrate. Given previous works' performance predictions and practical experimental conditions, this work chose to prioritize p^+n structures using undoped InP substrates, which are intrinsically slightly n-type with low doping concentrations of $\sim 10^{16} \text{ cm}^{-3}$. It investigated both Cd and Zn dopants and reports on the challenges encountered. Previous work highlights that fabricating reproducible p^+n InP structures by thermally diffusing Zn into InP is particularly challenging because of Zn's high diffusion coefficient [33]. Note that the anneal, and resulting change in carrier concentration, affects the interpretation of junction depth data [100].

It is also noteworthy that Zn and Cd diffuse to greater depths in InP than in GaAs because of the larger diffusion coefficient for Zn in InP than in GaAs [19] [40] [157]. This will make achieving thin p^+ emitters in InP much more challenging for anyone working on InP than for their peers working on GaAs, which is a crucial, fundamental step in achieving high-performing solar cells with sufficiently good carrier collection and low recombination. Work in this lab group has demonstrated

that multi-hour Zn diffusions into GaAs can yield emitters that are thinner than 200 nm, while diffusion depths into InP are several microns deep even with shorter diffusion times [141]. Thus, anyone working on InP will be fighting an uphill battle compared to those working on GaAs.

Tube Configuration

There are three main tube configurations for diffusions: open, closed, and leaky tube diffusion. Open-tube diffusion involves placing the wafer and dopant source in a quartz tube furnace with with a carrier gas, such as: N_2 ; H_2 ; Ar; or some mixture of those [39] [148]. The tube is open at both ends. In a closed-tube diffusion setup, the wafer and dopant source are sealed in a quartz ampoule under vacuum or with inert gas pumped into it. The leaky-tube setup is in between the open and closed-tube setup: the wafer and dopant source are placed in a semi-sealed liner or box, with a controlled leak to the outside [148].

Closed-Tube Diffusion

The closed-tube, or sealed ampoule, technique is the oldest, and has achieved high Zn concentrations and steep diffusion profiles InP [146]. It also provides surface protection against thermal damage [101]. On top of that, sealed ampoule setups tended to yield the lowest diffusivities for Zn diffusion into GaAs because of the larger As overpressure that is able to exist in a sealed ampoule setup when $ZnAs_2$ [148]. A similar phenomenon would likely occur with the use of Zn_3P_2 to diffusion dope InP. This is helpful, for a material with as high a diffusivity as Zn, to try and create more controlled p-n junctions. However, variations in Zn and P vapor pressure specifically results in poor reproducibility in doping concentration and junction depth [146]. This means that small variations in ampoule loading, sealing, dopant source and chip placement, and other such variables can lead to run-to-run variations in doping concentration, junction depth, and surface morphology. Ampoule-based methods in general can also exhibit notable batch-to-batch variability. Studies of photodiodes made from ampoule-based versus MOVPE-based doping showed that the former had reverse bias currents that varied between 0.1 and 1 nA even for a single batch / wafer — a factor of 10 — while the latter exhibited much less variation [146]. Additionally, sealed ampoule diffusion requires ampoule loading, evacuation, sealing, and re-opening that's labor-intensive, allow only a few wafers to be processed at a time, risk ampoule breakage during heating and cooling, and is difficult to automate. This makes sealed ampoule diffusion unsuitable for

commercial production with larger wafers or automated processes [71] [146].

Open-Tube Diffusion

Open-tube diffusion, on the other hand, allow for easier large-area diffusion, and is the process used for commercial Si doping [105] [101]. However, open-tube diffusion would be toxically dangerous to implement with Cd doping. It is also more difficult to maintain saturated vapor pressure in an open-tube setup, which lends itself to greater surface damage [148]. Previous work on InP solar cells has used open-tube diffusion to diffuse S or Se to create n-on-p solar cells [18]. Open-tube diffusions are more feasible for these elements because S and Se are less volatile and diffuse less readily, as evidenced by the need for higher diffusion temperatures. However, Cd and Zn diffusions to make p-on-n cells were made using closed-ampoule diffusions [34].

Leaky-Tube Diffusion

This work uses a leaky-tube diffusion approach to balance the advantages of open-tube and closed-tube diffusions. Leaky-tube approaches allow for a stagnant, inert, dopant-rich atmosphere to exist around the wafers and dopant source without the cumbersome sealing and re-opening steps necessitated by closed-tube diffusions. Care must be taken when handling Cd_3P_2 in particular, particularly at high temperatures, to limit toxic exposure.

4.2 Diffusion Experimental Procedure

Diffusion doping began with single-side polished undoped InP substrates that were cleaned with acetone and isopropyl alcohol. Then, they were loaded into a glass ampoule sealed off with quartz wool along with Cd_3P_2 or Zn_3P_2 powder in a smaller glass vial with a hole in the cap to allow for diffusion. The powder was kept out of contact with the chip to prevent surface damage. The air was pumped out of the system with a vacuum pump, and then forming gas (95% N_2 , 5% H_2) was refilled into the system to prevent oxidation at elevated temperatures. The whole system was then loaded into a quartz tube furnace that was pre-heated to the diffusion temperature of choice, and the system was maintained at this temperature for the desired diffusion time with forming gas flowing through the furnace. After that time elapses, the furnace was turned off and the forming gas continued to flow until the system had cooled down to at least 250°C to prevent accidental oxidation from exposure to air

at elevated temperatures. Fig. 4.1 is a schematic of the diffusion-doping setup. Photographs are included in Appendix A.

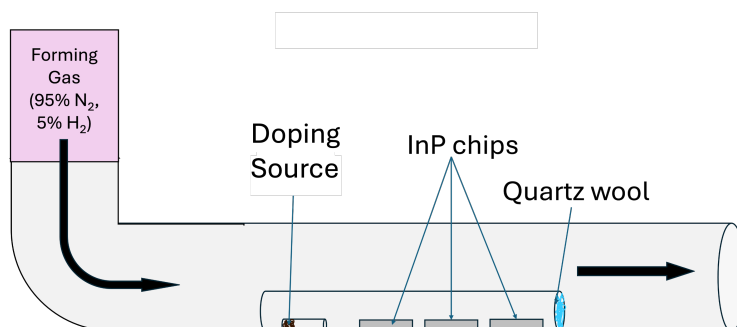


Figure 4.1: Schematic of the diffusion-doping setup. The glass vial containing the InP chips and diffusion doping source was pumped and then purged with forming gas. Forming gas is also flowed through the furnace, which is maintained at a given temperature for a given time for the diffusion process. Quartz wool is used to seal off the smaller tube to prevent volatiles from escaping.

After the samples have been cooled and retrieved, the unpolished back of the chip is etched with acid to remove the p-type surface doping from the back side.

4.3 Substrate Surface Before and After Diffusion

Figure 4.2 presents confocal microscope images of p-InP substrates before and after Cd diffusion. The diffusions were carried out for 1 hr at 560°C using Cd₃P₂ powder as the Cd source and the procedure outlined in Section 4.2. The surfaces look

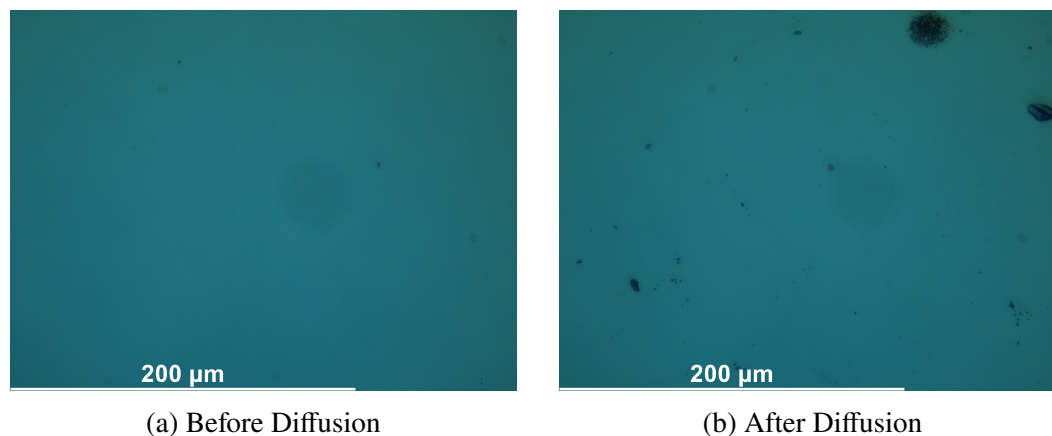


Figure 4.2: Confocal images taken at 40x magnification of InP substrates before and after a 560°C 1-hr Cd diffusion.

noticeably worse, with more dark spots on the substrate. Cd diffusions in particular were especially sensitive to visible oxidation. During some diffusion runs, the

surface would come out looking golden-brown throughout, although etching the samples in a dilute 1:100 HCl:H₂O solution would eat away at the top discolored layer and leave behind a fresher InP surface. Ways to avoid this are detailed in the Appendix, but even for relatively clean diffusions as seen with the naked eye, the confocal images show what Cd diffusions do to the surface. The photos are shown at 40x magnification, and show the cleanest, least-discolored sections of the chip to illustrate the potential of clean diffusions with limited oxidation.

4.4 Surface Treatment

Previous Passivation Studies

Previous work had found that thermal diffusion can destroy the surface stoichiometry of the sample [33]. The same work illustrated that chemical treatment of InP with HNO₃ and HF created a thin layer of non-stoichiometric In(PO₃)_x with $2 < x < 3$, that was more stable and had better intrinsic passivation properties than the double-layer In₂O₃-In(PO₃)_x that forms on InP treated with *o*-H₃PO₄ or H₂SO₄ [33]. Results were overall mixed on the effects of various factors, such as surface doping concentration and type as well as elevated temperature anneals, on the interface states between the surface oxides and substrate. There was no clear correlation or trend between doping type (p versus n), heavy versus light doping, or low versus high temperature post-treatment anneals [33]. Since HNO₃ generally worked the best out of the chemical oxidizers used, and it was readily available, it was tried as a pre-diffusion surface treatment for InP to see if it would improve the surface quality of the sample post diffusion [33]. Confocal images were taken and will be presented in the next section.

Previous work fabricated cells from samples where diffusions were performed through chemically or anodically-grown P-rich cap layers [36] [31]. However, at the time of this work, the exact process parameters and relevant chemical compositions were unable to be identified from the publicly-available literature. Thus, after initial investigations of HNO₃ treatment, the thesis focused on diffusions performed simply on samples with and without the native oxide. In doing so, it aimed to establish a baseline and focus on simple, easily-reproducible steps to minimize sources of variation in an already-finicky process. Once the behavior and performance of this baseline is well-understood, particularly within the unique conditions of this lab's equipment, future work can build on this understanding to introduce additional improvements such as the use of the PNP etchant mentioned in previous works [31].

Confocal Images of HNO_3 -Treated InP

Figure 4.3 illustrates p-InP surfaces before and after HNO_3 treatment. The treated sample was immersed in HNO_3 for 1 hr under the illumination of a desk lamp. It is

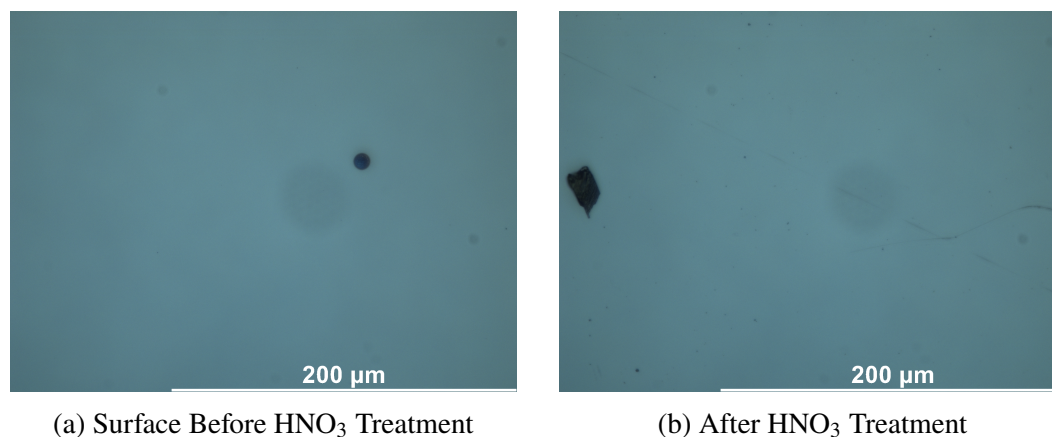


Figure 4.3: p-InP surface before and after immersion in HNO_3 for 1 hr under illumination.

evident that, overall, the surface is a bit more discolored after the HNO_3 treatment than before. There is also evidence of streaking and lines on the surface. HNO_3 treatment seems to visually worsen the quality of the surface.

HNO_3 -Treated Substrates Before and After Diffusion

Figure 4.4 shows the surface of a p-InP chip treated with HNO_3 for 1 hr under illumination before and after a 1-hr Cd diffusion at 560°C using the procedure outlined in Section 4.2. The visible discoloration and roughening of the treated

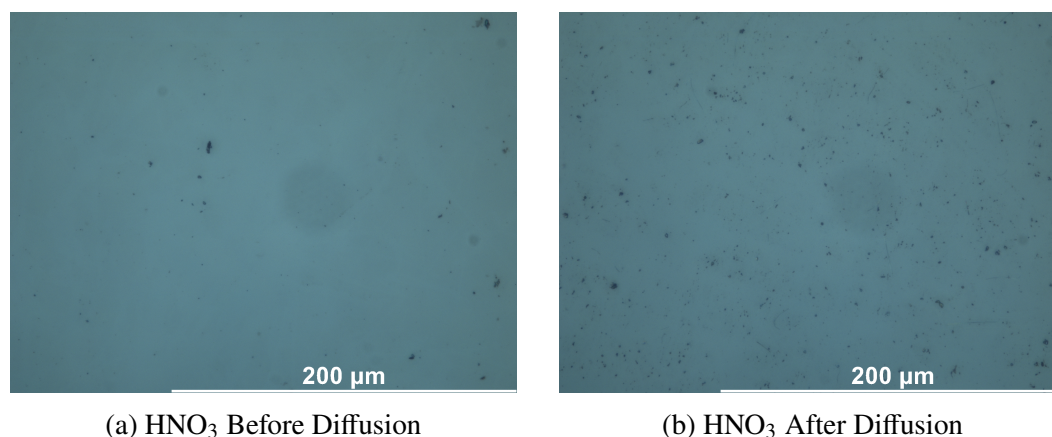


Figure 4.4: p-InP surface before and after immersion in HNO_3 for 40 minutes under illumination.

surface after diffusion is worse than that of the untreated surface. While diffusions

were not consistent, and varied in resulting surface quality and discoloration, this investigation suggests that there is not a clear advantage in using an HNO_3 pre-treatment before diffusion from a surface quality perspective. Therefore, the current work focuses on diffusions on untreated InP substrates. Future work can build on the work in this thesis by trying other oxides studied in Faur's work, such as the anodic oxides mentioned [33].

Preliminary Surface Acceptor Concentration With and Without HNO_3

FastHall measurements were taken for both bare InP and HNO_3 -treated samples. The "bare" InP samples on these measurements still had the native oxide on the surface. Chips can be any shape as long as four well-separated contact dots can be defined along the perimeter, but it is easier if the samples are rectangular or square, or at least some kind of quadrilateral [107]. The easiest way to define the Hall contacts at the corners is to use "marker photolithography," as defined in Appendix A.2. However, before Phil came up with this idea, initially tape or paper strips were used to cover the portion of the chip where metal contacts were not desired. Using tape resulted in residue, however, and though samples can be cleaned afterwards, it risks removing or ruining the metal contacts deposited.

The Hall measurements report the measured carrier mobility (μ_p), sheet carrier concentration (n_s), and n-type count versus p-type count, among other measurements. Table 4.1 reports the mobility (μ_p) and sheet carrier concentration (n_s), of the bare InP samples and samples treated in HNO_3 for 1 hr. These samples were then diffused for 10-60 minutes, in increments of 10 minutes. Two chips were doped in each run, and one was treated with HNO_3 while the other was left untreated. Only diffusions of 40, 50, and 60 minutes in duration registered a proper Hall measurement with sufficiently Ohmic contacts detected during the contact check. Thus, only those are reported. It also reports the predicted surface carrier concentration p based on μ and this chart [56]. From there, it attempts to provide lower bound on the diffusion depth d by assuming the surface concentration is the same throughout the junction. This depth can be given by

$$d (\mu\text{m}) = \frac{n_s}{p} * 10^4 \quad (4.1)$$

The diffusions were carried out at 560°C for 1 hr using Cd_3P_2 as the dopant source. To do an "apples-to-apples" comparison, "bare InP" samples from the same diffusion run as the chosen HNO_3 samples of a given treatment time (e.g. 1 hr) were chosen, even though the bare samples themselves were not treated.

Type	μ_p ($\text{cm}^2/\text{V}\cdot\text{s}$)	n_s (10^{12} cm^{-2})	p (10^{18} cm^{-3})	d (μm)
Bare InP (40 min)	36.19	948	4	2.37
HNO ₃ (40 min)	36.5	274	4	0.685
Bare InP (50 min)	65	6700	1	67
HNO ₃ (50 min)	24.3	7600	9	8.444
Bare InP (1 hr)	63.46	43.267	1	0.4327
HNO ₃ (1 hr)	33.06	70	6	0.1167

Table 4.1: Surface mobilities, sheet resistance, and estimated doping levels and depths of p-type carriers on Cd-doped InP samples both with and without HNO₃ treatment for 1 hr under illumination.

These results suggest that the HNO₃ layer can enhance the surface doping concentration and result in shallower p-n junctions. Though the predicted d values are not all realistic — particularly for the 50 minute diffusions — it serves as a starting point for the doping concentrations and depths that can be expected with this process. Some Cd₃P₂ had sprinkled out of the cuvette during handling of the 50-minute diffusion run, which may have resulted in the much higher surface carrier concentrations for the 50-minute diffusions compared to the 40-minute and 60-minute diffusions.

First, these results illustrate that desired emitter doping concentrations of $\sim 10^{18} \text{ cm}^{-3}$ can be achieved with diffusion durations of at least 40 minutes and above with Cd₃P₂ as a dopant. These results also demonstrate that, if desired, an HNO₃-grown oxide layer may enhance doping concentration relative to a bare sample and result in shallower junctions. However, given the small size of the quartz test tube used for the diffusions, doping may not have been uniform for the two chips in the setup. Additionally, as noted earlier, the HNO₃ seemed to result in rougher surfaces, so the advantage from higher doping concentrations and shallower junctions may be offset by surface quality and resulting recombination when it comes to the final device performance.

Nonetheless, these investigations go beyond previous work by illustrating the potential degradation of surface quality, potential increase in surface concentration, and potentially even shallower diffusion depth. It suggests that further investigation may be worthwhile for potential device improvement, if the higher doping concentration and shallower doping depth are consistent, reproducible results and offset the surface quality reduction. However, future work will stick to untreated samples and focus on optimizing the "core" diffusion process.

4.5 Optimizing Diffusion Parameters

The two main diffusion parameters to optimize were temperature and time. Both dictate the depth and shape of the diffusion profile [141]. In the case of Zn diffusions, the anneal temperature must also be optimized to achieve maximum Zn electrical activation while minimizing the extent to which the post-diffusion anneal causes the Zn to diffuse deeper into the device and create a deeper p-n junction.

Temperature Optimization

Previous work tried diffusion temperatures from 500-550°C for Zn-doped cells and 550°C-660°C for Cd-doped cells [34] [31]. Interestingly, the diffusion depth for Zn was shallower at 540°C than at 500°C, which is counterintuitive [34]. Other work has also found that diffusions at 540°C were more difficult than at 505°C [77]. The diffusion depth for Cd was deeper at 650°C than 560°C, as expected. Though the literature reports on the complexity of Zn diffusion in InP, such as the formation of relatively-immobile neutral complexes like $V_PZn_{In}V_P$ that compete with conventional substitutional-interstitial mechanisms, their temperature dependence is unclear [140]. It does highlight, however, the importance of empirically testing various temperatures within a reasonable range instead of extrapolating too much.

Cd Diffusion Temperatures

For Cd diffusions, Faur's work reported on 650°C diffusions, after which the emitter was thinned down from its depth of more than 2 μm [34]. However, their work also found low etch pit densities and a shorter diffusion depth of less than 2 μm at 560°C diffusions [32]. This informed a starting point of 560°C for the Cd diffusion. Since successful Cd diffusions have been performed at lower temperatures, this work proceeds in attempting to lower, rather than raise, the Cd diffusion temperature to fabricate solar cells that require less emitter thinning for a shallow p-n junction. Some of the Cd solar cell fabrication work was done at 550°C instead.

Zn Diffusion Temperatures

Meanwhile, for Zn, since Faur's work started at a temperature of 500°C and other work has demonstrated successful diffusion and post-diffusion anneals at 500°C, 500°C was used as a starting point for the Zn diffusion temperature [34] [147]. Since 500°C was the lower end of reported Zn diffusions, however, this work increases the diffusion temperatures beyond 500°C. It turns out, as will be later discussed,

that 500°C Zn diffusions do not work when the native oxide layer is left on as a protective diffusion cap. This necessitates the use of higher diffusion temperatures for Zn, though the temperatures are still lower than the Cd diffusion temperatures.

Time Optimization

There is a tradeoff between low and high diffusion times. Since shallow p-n junctions are desired, a lower diffusion time is preferable to achieve as shallow a p-n junction as possible without needing to thin the emitter post-diffusion. This is because thinning is usually achieved via acid etching, which can damage the surface, so the shallower the p-n junction can be from just the diffusion process, the better. A lower diffusion time also subjects the sample to less surface damage from the diffusion process itself.

However, the diffusion time cannot be lowered too much because it takes time for the system to achieve the desired doping temperature and dopant pressures when evaporated, and the process needs to be performed at those consistent pressures and temperature for long enough to achieve process consistency. Thus, there is a limit to the extent to which diffusion depth can be shortened by reducing the diffusion time.

Cd Diffusion Times

Previous work on Cd diffusions used diffusion times ranging from 5 min to 64 hrs [99] [31]. There was a focus on times ranging from 30 to 60 min, particularly at 560°C and 650°C [99] [31]. Additionally, other work reported a 60 min Cd diffusion at 575°C, which is close to the 560°C starting diffusion temperature chosen for Cd diffusions [141]. The Hall measurements reported in Section 4.4 of this thesis suggest that diffusion durations of 40 minutes and above are needed to obtain sufficient doping across the surface to properly measure a desired emitter doping concentration. Thus, this work started with a 1 hr diffusion time for Cd diffusions, and then attempts to lower the diffusion temperatures to achieve shallower p-n junctions.

Zn Diffusion Times

The Zn diffusion work reporting the post-diffusion anneals to electrically activate the Zn dopants used 15 min furnace times for both the diffusions and post-diffusion anneals starting at 500°C, so 15 min diffusion and anneal times were used as starting points here. It became clear as the diffusions were performed that longer diffusion

times were needed, so diffusion times were increased beyond the 15 min starting point.

Note on Post-Diffusion Cooldown

Post diffusion, the furnaces were turned off and allowed to cool down naturally, but the samples were not extracted from the furnace until the temperature had cooled down to room temperature, and the forming gas was only switched to N₂ once the furnace temperature had cooled down to at least 250°C, if not lower. Thus, the diffusion time was in practice technically longer than the reported times for the particular temperature, and the furnace was cooling down during this extra time. Thus, the higher the temperature, the longer the actual diffusion time technically was. This is another reason why being able to use a longer diffusion time while achieving sufficiently shallow junctions for functioning devices is important — it improves the process consistency since a larger fraction of the process time is actually operated at the desired, consistent temperature.

Note Regarding Surface Impacts on Optimization Parameters

Later sections will elaborate on these effects in greater detail. However, the surface layer on top of the InP substrate, or lack thereof in the case of samples with the native oxide removed and no deliberately-grown cap layer, greatly affect the diffusion temperature and time needed to achieve diffusions of a particular depth. They also likely affect the diffusion profile shape as well. This work demonstrates that the native oxide acts as a stopping layer that results in shallower diffusions than surfaces with the native oxide removed. This means that the latter would require lower diffusion temperatures and times to achieve a particular diffusion depth. This is important to keep in mind when performing diffusions and fabricating solar cells, since the diffusion depth and profile shape will affect the resulting solar cell performance and even future fabrication steps, such as mesa etch time and amount of acid exposure via mesa etching and emitter thinning, if implemented.

4.6 Cell Characterization Results

The diffusion runs in this subsection were performed at 550°C for 1 hr. After diffusion, standard photolithography is used for defining contacts and mesa isolation on the front. The cells measure 3 mm on each side. A 20% by weight iodic acid in water etch was initially used because it can controllably etch InP and is non-volatile, unlike HCl. This was later reduced to 10% to leave leeway to avoid the formation

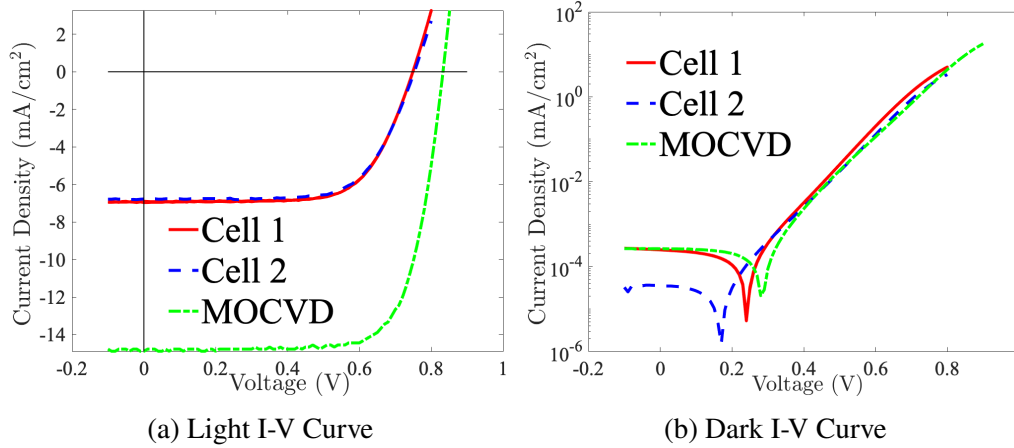


Figure 4.5: I-V curves of two of the diffusion-doped solar cells along with the MOCVD-grown cell. The diffusion for Cell 1 was etched in a 100:1 $\text{H}_2\text{O}:\text{HCl}$ solution to remove surface oxide, while the diffusion for Cell 2 was thinned 500 nm.

of "cigar-shaped hillocks" that would form with too high a concentration of iodic acid [135]. This feature of iodic acid prevents off-target etching [135]. Some of the cells exhibited visible oxidation during diffusion, particularly during Cd diffusions. Etching them with a 100:1 water:hydrochloric acid ($\text{H}_2\text{O}:\text{HCl}$) solution removed visible surface damage. After initial fabrication, some of the cells' emitters were thinned by etching the surface away with the iodic acid in an attempt to improve the short-circuit current density (J_{SC}).

Then, a bottom contact of 50 nm nickel and 50 nm silver was deposited on the acid-etched undoped side while a metal stack of Ag-Zn-Ag, with each layer being 50 nm, is patterned on the p^+ -doped top surface by liftoff before being annealed at 375°C for 5 minutes.

Cd-Doped Cells

Fig. 4.5 shows the dark and light I-V curves of two of the fabricated diffusion-doped solar cells, along with the curves of the MOCVD-grown epitaxial cells for comparison. Table 4.2 summarizes key solar cell parameters obtained from the light and dark I-V curves of the cells in question.

Table 4.3 reports parameters from the QE fits and the Hall measurements. It reports both L_n and L_p for all three cells. Note that L_n represents the diffusion length in the p^+ emitters of the diffusion-doped cells but the diffusion length in the p-type base for the MOCVD cell, while L_p represents the diffusion length in the undoped base of the diffusion-doped cell but the n^+ emitter of the MOCVD cell. The values that

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF(%)	J_0 (mA/cm ²)	n
Cell 1	3.53	6.90	749	68.2	$8.23 * 10^{-7}$	1.88
Cell 2	3.46	6.78	753.2	67.8	$1.11 * 10^{-6}$	1.97
MOCVD	9.08	14.92	832.8	73.1	$1.39 * 10^{-6}$	2.14

Table 4.2: Figures of merit comparisons for the two diffusion-doped cells plus the MOCVD cell. This table reports the efficiencies, short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF), as well as the dark J-V parameters J_0 and n .

represent minority carrier diffusion lengths in the respective emitters are indicated in red and bolded in Table 4.3.

Parameters	Cell 1	Cell 2	MOCVD
$N_{emitter}$	$1.5 * 10^{18} \text{ cm}^{-3}$	$6 * 10^{17} \text{ cm}^{-3}$	10^{18} cm^{-3}
IQE Emitter Width	$0.914 \mu\text{m}$	$0.990 \mu\text{m}$	$0.05 \mu\text{m}$
Hall Emitter Width	$0.275 \mu\text{m}$	$2.32 \mu\text{m}$	$0.05 \mu\text{m}$
SRV (cm/s)	$7.08 * 10^6$	$1.03 * 10^7$	$9.77 * 10^6$
L_n	0.653 μm	0.831 μm	$1.36 \mu\text{m}$
L_p	$1.87 \mu\text{m}$	$1.86 \mu\text{m}$	3.30 μm
% Efficiency	3.53	3.46	9.08

Table 4.3: Extracted parameters from I-V, QE, and Hall measurements. $N_{emitter}$ refers to the doping concentration in the emitter layer (p^+ for Cells 1 and 2, n^+ for the MOCVD cell).

The emitter doping concentrations for Cell 1 and Cell 2 were estimated from mobility measurements using Hall measurements of InP chips that were diffused in the same run as the respective solar cells and we assume constant carrier concentration with depth in the diffused layer. [56]. The table also includes estimated emitter widths from both quantum efficiency (QE) fits and the Hall measurements as well as the minority carrier diffusion lengths.

These preliminary results suggest several things. First, the work has demonstrated a proof-of-concept for successful fabrication of low-cost, diffusion-doped, InP solar cells. The FFs for both of the diffusion-doped cells are a bit less than that of the MOCVD device, which suggests higher series and shunt resistances in the diffusion-doped cells compared to the MOCVD cells. The dark J-V curves give further insight into the resistance behavior. They taper off a little more for the diffusion-doped cells than the MOCVD reference cell, suggesting higher series resistance. However, the lack of s-shaped curving at lower voltages suggests that all of the solar cells have limited shunt resistance. Table 4.2 also includes the diode ideality factors n and the

dark current density J_0 from the dark curves. This suggests that the recombination mechanisms are similar in all cells, suggesting improving the J_{SC} of the diffusion-doped cells to more closely match the J_{SC} of the MOCVD cell will result in much higher efficiencies. Cell 1 does have a slightly lower n than Cell 2, which in turn has a slightly lower n than the MOCVD reference cell. This suggests that recombination from majority carriers plays more of a role in Cell 2 than in Cell 1.

In Cell 2, the majority carrier diffusion length, L_p is less than the minority carrier diffusion length L_n , while in Cell 1, the minority carrier diffusion length L_n was less than the majority carrier diffusion length L_p , so the fitted values for these diffusion lengths makes sense with the diode ideality factors n [49]. Notably, for the MOCVD reference cell, the majority carrier diffusion length in the emitter is actually L_n , which is shorter than L_p , and the MOCVD cell has a higher n . This phenomenon may be related to the thinner emitter region in Cell 2, which has had the top 500 nm etched away.

Further work is needed to fabricate the cells more consistently and improve the recombination mechanisms at play. Reducing oxidation during the fabrication process will eliminate the need for the surface etching that's performed to rehabilitate the surface. However, etching for potential emitter thinning may still be desired. The diffusion-doped device's J_{SC} is less than half of the MOCVD cell's J_{SC} . This makes sense for Cell 1 because the p-n junction is much deeper into the device than it is in the MOCVD-grown cell, but it is notable that thinning the emitter in Cell 2 did not improve the J_{SC} . This may be because the surface emitter doping concentration is lower, based on the Hall measurements, for Cell 2 than for Cell 1. Given that the top 500 nm of the surface were etched away, it is not surprising that the carrier concentration may be lower. It suggests that future work on emitter thinning should start with less emitter thinning — perhaps 100 nm or even 50 nm.

The fitted emitter width from the QE for Cell 2 was similar to that of Cell 1, while the estimated emitter width from the Hall measurement was much larger for Cell 2 than for Cell 1, suggesting that without the surface oxidation, the diffusion itself may have been deeper into the surface than for Cell 1. Further work is needed to obtain precise diffusion profiles and determine the depth of the p-n junction via methods such as secondary ion mass spectroscopy (SIMS) or spreading resistance measurements to resolve this discrepancy and constrain the QE fits to obtain truer values for the other parameters such as L_n . In addition, the V_{OC} of both cells is significantly lower than that of the MOCVD-grown cells, indicating that the former can benefit from further

work in trying different diffusion parameters such as duration and temperature for improved surface quality as well as passivation. Device yield improvement during the diffusion doping process is also needed to avoid surface oxidation effects.

Figure 4.6 presents the internal quantum efficiency (IQE) fits of the two diffusion-doped cells as well as the MOCVD-grown cell. First, the fitting for the diffusion-

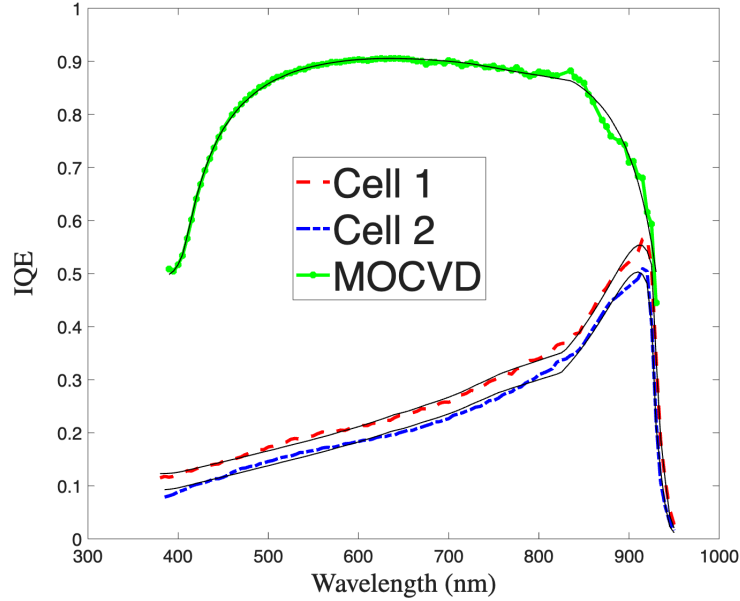


Figure 4.6: IQE measurements of the diffusion-doped cells and the previously-fabricated epitaxial cell. The fits are plotted in the thin black lines to illustrate the quality of the fit upon which the parameters were based.

doped cells, which were simple p-n junction cells, were more in line with the model from Sze et. al. than the MOCVD cells [121]. For the diffusion-doped cells, $|d\lambda| < 3.5$, which represents the wavelength shift for the laser / detector system, as expected, while c ranged from 0.996 to 1.02. Conversely, for the pre-ARC MOCVD cell, $|d\lambda| = 10.3$, and for the post-ARC model, $c = 1.07$. This provides support for the hypothesis that the amount of empirical tweaking to the model needed for the MOCVD cells, coming from the stretch factor c and the wavelength shift $|d\lambda|$, was due to the heterostructure composition rather than measurement error or the like.

The fitted SRV for Cell 2, which had been exposed to acid long enough to be thinned 500 nm, had a higher SRV than Cell 1, which had only been subject to a 100:1 $\text{H}_2\text{O}:\text{HCl}$ solution to remove the surface oxidation. All cells have high SRVs in comparison with the values for InP in the literature, indicating that investigating passivation paths and minimizing acid-induced damage can help improve surface quality, and from there yield better device efficiencies through higher V_{OCs} . The

fitted emitter widths for the two cells are around $1.0\ \mu\text{m}$, even though Cell 2 underwent a thinning of the top 500 nm of the surface to make the emitter shallower and improve the collection of shorter-wavelength photons. This suggests that the diffusion may have gone deeper into the wafer for Cell 2 without the surface oxidation. The MOCVD-grown structure had a known emitter width of 50 nm. Further work needs to be done to determine the p-n junction depth experimentally and the tradeoff between emitter thinning and device efficiency.

Table 4.4 lists the parameter ranges for the QE model fitting for Cells 1 and 2 and the MOCVD cell:

Parameters	Cell 1	Cell 2	MOCVD
c	0.91-1.02	0.91-1.02	0.99-1.04
W_e	0.01-2	0.01-2	0.03-0.08
L_n	0.01-5	0.01-5	0.001-5
L_p	0.01-20	0.01-20	0.1-20
W_d	0.1-0.4	0.1-0.4	0.13-0.14
K_p	0.01-1000	0.01-1000	0.1-1000
K_q	0.01-1000	0.01-1000	0.1-1000
$ d\lambda $	3.5	3.5	10.5

Table 4.4: Parameter ranges for the IQE model in Size to fit the IQE curves for the diffusion-doped and MOCVD cells.

Reducing Diffusion Doping Temperature

Cd diffusions at 540°C were attempted. However, since valid Hall measurements were not obtained for the diffusion run obtained, the work chose to focus on 550°C and 560°C diffusions.

Reducing Diffusion Doping Time

From here, the Cd diffusion time was reduced from 60 minutes to 35 minutes. This resulted in higher-efficiency cells.

Figure 4.7 compares the performance of Cd-diffused cells with durations of 1 hr and 35 minutes. It is unclear whether the 1 hr diffusion was performed at a temperature of 550°C or 560°C , because I switched between the two temperatures. It could be at 550°C because that was the diffusion temperature dialed in for the 1 hr diffusion time, and because the resulting J_{SC} was higher than the previous batch of 1 hr 550°C diffusions. This would be unlikely if a higher diffusion temperature was used since

that would result in a thicker emitter layer and a p-n junction further from the surface, which would lead to fewer carriers being collected at the surface.

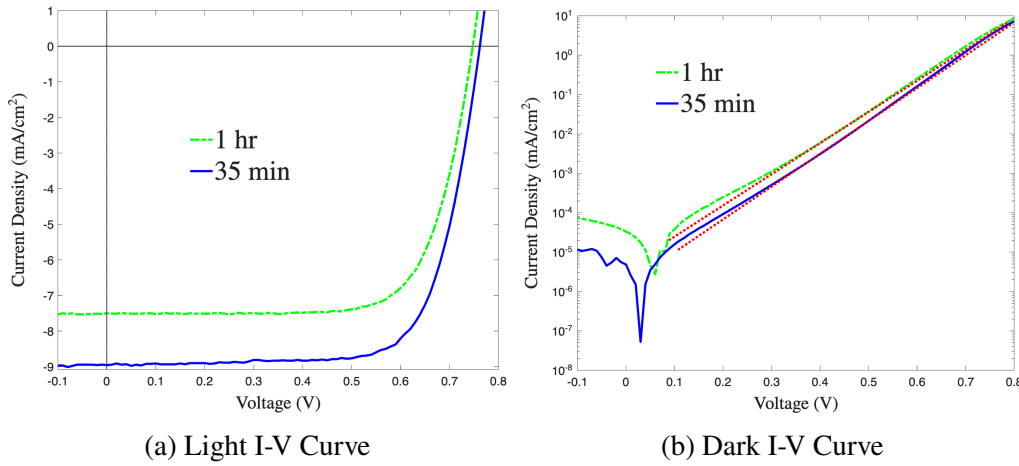


Figure 4.7: I-V curves of Cd-doped cells diffused for 1 hr at 550°C and 35 min at 560°C.

Table 4.5 compares performance parameters for the two cells. Reducing the diffusion

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF	n	J_0 (mA/cm ²)
1 hr	4.08	7.50	747.8	72.7%	2.16	5.17×10^{-6}
35 min	4.94	8.96	762.3	72.4%	2.02	1.74×10^{-6}

Table 4.5: Figures of merit comparisons for two Cd-doped cells. The 1 hr doping was likely at 550°C, while the 35 min doping was at 560°C.

time notably improved almost all aspects of device performance despite the higher diffusion temperature used. Notably, the J_{SC} exhibited a 19.4% increase and the V_{OC} exhibited a 1.94% increase. The FF is almost the same, which results in a 21.4% increase in the final device efficiency, from 4.08% to 4.94%. Both the higher J_{SC} and V_{OC} make sense in light of a likely shallower junction. The lack of meaningful change in the FF suggests that the series and shunt resistances are effectively the same. This is confirmed by the dark J-V curves, which have a straight slope from $V = 0.2V$ onwards. The slope of the 1-hr diffusion's log dark J-V curve, however, is visibly less than that of the 35-minute diffusion, and tapers a little more at high voltages as well. Since the slope is inversely proportional to n , this is confirmed by the 1 hr diffusion cell's higher diode ideality factor n . This suggests that the 1-hr diffusion yielded a higher device series resistance than the 35-minute diffusion. This also makes sense with the current moving through less semiconductor material if the p-n junction is shallower. The overall dark current levels are higher for the 1-hr

diffusion cell than the 35-min diffusion cell, which is reflected in their respective J_0 values. This suggests that the shorter diffusion results in better material quality leading to less recombination, since J_0 reflects the amount of recombination in the device. This is because the source of the dark current J_0 is thermally-generated carriers in a device that is not illuminated. A higher J_0 reflects more trap states, which lead to easier thermal generation of charge carriers since some of those carriers come from the trap states instead of the semiconductor's valence band, so the excitation energy is lower.

Figure 4.8 plots the IQE curves of the 1-hr and 35-min Cd-diffused cells. Table 4.6 lists the parameters extracted from the IQE fits. The N_{emitter} was interpolated from Hall measurements of the surfaces of other chips diffused in the same diffusion run [56].

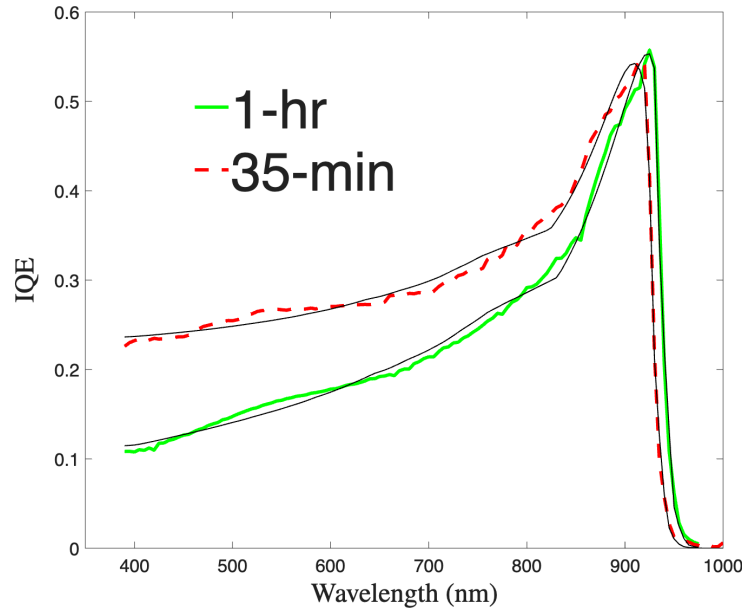


Figure 4.8: IQE measurements of the diffusion-doped cells and the previously-fabricated epitaxial cell. The fits are plotted in the thin red lines to illustrate the quality of the fit upon which the parameters were based.

Despite the fitted depletion width running up against the limits of $0.1 \mu\text{m}$, the allowed W_d range was restricted from $0.1\text{-}0.4 \mu\text{m}$ for all of the diffusion-doped cells because based on the doping range of $10^{16}\text{-}10^{18}$ generally present for these cells, this is the physically-sensible range of depletion widths possible [119]. The stretch factor c was 1.08 for the 35-min diffusion, and 0.959 for the 1-hr cell. This was outside of the $0.99\text{-}1.01$ range expected, which is surprising since c is supposed to be a minor stretch factor. The $d\lambda$ shift for the EQE laser-detector system was -2.61

Parameters	1-hr	35-min
$N_{\text{emitter}} \text{ (cm}^{-3}\text{)}$	$> 10^{19}$	$1.5 * 10^{18}$
IQE Emitter Width	$0.867 \mu\text{m}$	$1.09 \mu\text{m}$
Hall Emitter Width	$0.938 \mu\text{m}$	$0.167 \mu\text{m}$
SRV (cm/s)	$4.08 * 10^6$	$5.54 * 10^5$
$L_n \text{ (}\mu\text{m)}$	0.432	0.541
$L_p \text{ (}\mu\text{m)}$	3.66	1.42

Table 4.6: Extracted parameters from QE and Hall measurements for the Cd-diffused cells. The 1-hr cell was likely diffusion doped at 550°C while the 35-min cell was diffusion doped at 560°C. N_{emitter} refers to the doping concentration estimated from Hall mobility measurements.

nm, which was within the 3.5 nm limit expected based on the offset in the EQE software and residual error. Fitting the data for the 35-minute diffusion required constraining the emitter width range from 0.9-2 μm , otherwise the fitting algorithm diverged or fit parameters "pressed up" against the defined limits (e.g. determining an emitter width of 0.8 μm when the lower limit is set to 0.8 μm).

The IQE curves and their fits illustrate that reducing the diffusion time resulted in greater carrier collection across the visible spectrum, with the most notable improvement at the shorter wavelengths. This further suggests that the diffusion depth was shallower in the 35-minute diffusion even at 560°C than the 1-hr diffusion likely at 550°C. However, the fitted emitter width of the 35-minute diffusion is larger than that of the 1-hr diffusion, which does not match what is expected based on other data about these devices, such as the IQE itself and the cell performance. This means that more higher-energy photons were able to reach the p-n junction, get absorbed, and be collected at the surface in the 35-minute diffusion than in the 1-hr diffusion.

However, even the 35-minute doping IQE profile exhibits the same triangular shape as the 1-hr doping IQE profile, which is very different from the broadband IQE curve of the MOCVD cell. The p-n junction is likely still too deep. Emitter thinning may still improve the I-V curve, although previous sections' results demonstrate that the thinning cannot be too extreme — it is likely in the 100 nm or less range, especially for the shallower diffusion doping profile that likely resulted in the 35-minute diffusion. Additionally, the diffusion doping profile takes the shape of an error function instead of a constant throughout the entire layer. This means that emitter thinning will reduce the surface doping concentration, potentially increasing the surface resistance, reducing the effectiveness of the built-in electric field that

helps improve carrier collection, and increasing the dark saturation current, thereby decreasing V_{OC} . Thus, care must be taken when emitter thinning.

The IQE profile also shows that carrier collection needs to be improved across the entire visible + near-infrared spectrum, not just the shorter wavelengths. Further temperature and time adjustments may also help improve the device's short-wavelength carrier collection. Surface texturing, like with the TiO_2 pyramids, or using ARCs can also help improve the device's IQE as evidenced by simulation results of pyramidally-textured cells in Figure 2.11 and the IQE curves in 3.5.

Table 4.7 lists the parameter ranges for the model fits for the 1 hr and 35 min dopings.

Parameters	1 hr	35 min
c	0.95-1.05	0.99-1.08
W_e	0.7-2	0.9-2
L_n	0.1-5	0.1-5
L_p	0.1-20	0.6-5
W_d	0.1-0.4	0.1-0.4
K_p	0.01-1000	0.1-1000
K_q	0.01-1000	0.1-1000
$ d\lambda $	4.5	3.5

Table 4.7: Parameter ranges for the IQE model in Sze to fit the IQE curves for the 1 hr and 35 min diffusions.

Emitter Thinning Attempts

To compare apples to apples and attempt to investigate the same solar cell before and after thinning, several fabricated cells were thinned by 100 nm with 20% by weight iodic acid after initial measurements. Figure 4.9 illustrates the resulting light and dark J-V curves. Table 4.8 compares performance parameters for the pre-thinned versus post-thinned cells.

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF	n	J_0 (mA/cm ²)
Pre-Thinned	4.08	7.50	747.8	72.7%	2.16	$5.17 \cdot 10^{-6}$
Post-Thinned	1.83	6.71	746.2	36.5%	2.65	$1.82 \cdot 10^{-5}$

Table 4.8: Figures of merit comparisons for a 1 hr, 550°C Cd-doped cell before and after 100 nm thinning with iodic acid.

The J_{SC} and V_{OC} were slightly reduced, with the J_{SC} exhibiting a more severe proportional decrease than the V_{OC} . However, the FF dropped severely. This indicates much higher devices resistances. The dark J-V curves confirm this, given

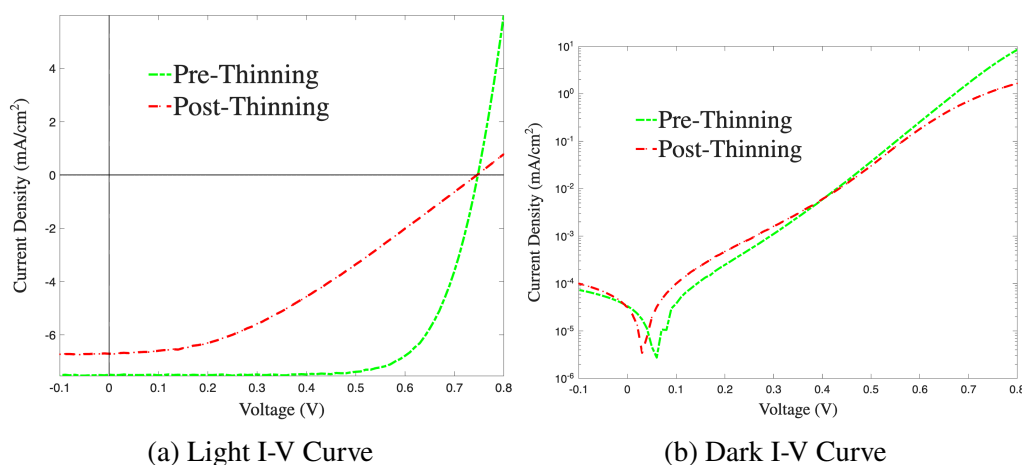


Figure 4.9: I-V curves of Cd-doped cells diffused for 1 hr, likely at 550°C, before and after 100 nm of thinning with iodic acid.

that the post-thinning dark J-V curve has more of an "S" shape, indicating higher shunt and series resistances than the pre-thinning cell. This is likely due to the acid destroying the top contact. Further studies, therefore, are needed to isolate the impacts of emitter thinning and its effect on device performance.

Figure 4.10 illustrates the QE measurements and fits before and after the thinning. Table 4.9 reports the parameters for the QE fits. Note that the Hall measurement-

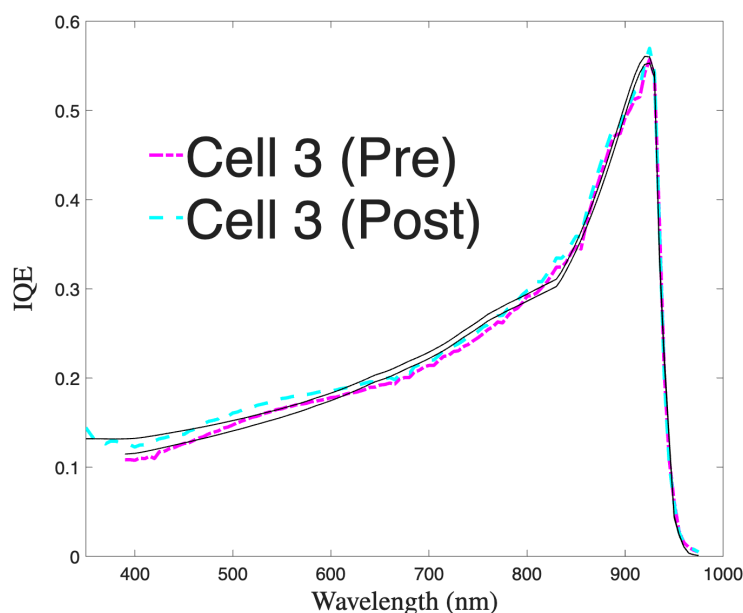


Figure 4.10: IQE measurements of a diffusion-doped cell before and after thinning. The fits are plotted in the thin black lines to illustrate the quality of the fit upon which the parameters were based.

dependent quantities, such as the emitter concentration and Hall emitter width, are not repeated because Hall measurements are unable to be taken on a sample once it has been turned into a solar cell due to the mesa etching and the top metal contacts. The fit seems to imply 17 nm of thinning, which is less than the 100 nm expected.

Parameters	Pre-Thinning	Post-Thinning
IQE Emitter Width	0.867 μm	0.866 μm
SRV (cm/s)	$4.08 * 10^6$	$2.40 * 10^6$
L_n (μm)	0.432	0.391
L_p (μm)	3.66	3.14

Table 4.9: Extracted parameters from QE and Hall measurements for a Cd-diffused cell before and after thinning.

The surface quality seems to be improved based on the SRV, which would make sense if the very top of the surface is damaged from the diffusion doping and the etching removes that damaged part. However, the thinning seems to have reduced the carrier diffusion lengths in both the doped p region and the undoped substrate. The shorter hole diffusion length in the undoped substrate does not make sense since the thinning should only affect the p-type surface unless the p layer were completely etched away. However, if these fitted values are to be believed, then the QE curves in Figure 4.10 imply that the improved SRV outweighs the reduced carrier diffusion lengths. Though the IQE improvement is marginal from thinning, it at least shows that the carrier collection is not worsened, and further suggests that the performance reduction is due to top contact damage rather than overthinning or sample surface damage due to acid etching.

Table 4.10 lists the parameter ranges for the model fits for the pre-thinned and post-thinned cells.

Diffusions With and Without InP's Native Oxide

Since removing the native oxide provided the possibility of lower diffusion temperatures, which could allow for some combination of a shallower p-n junction depth and longer diffusion times for better uniformity and control, fabrication attempts were made after removing the native oxide with a 4:1:100 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution for 2 minutes [134]. However, this resulted in diffusions so deep that even the 30-minute mesa etch with iodic acid did not suffice to completely mesa etch the chip. This was noted by I-V curves that did not flatten for negative voltages. Additionally, the efficiencies were less than 4.8% despite the "extra" current from

Parameters	Pre-Thinning	Post-Thinning
c	0.95-1.05	0.99-1.02
W_e	0.7-2	0.7-2
L_n	0.1-5	0.1-5
L_p	0.1-20	0.1-10
W_d	0.1-0.4	0.1-0.4
K_p	0.01-1000	0.01-1000
K_q	0.01-1000	0.01-1000
$ d\lambda $	4.5	4.7

Table 4.10: Parameter ranges for the IQE model in Sze to fit the IQE curves for the cell before and after 100 nm of thinning.

neighboring cells due to incomplete mesa etching, suggesting that there would not be meaningful performance gains from removing the native oxide. This is because the resulting depth of the p-n junction is more than 1950 nm based on the etch time and rate of even a 10% weight iodic acid mixture. This requires a mesa etch so long that it removes the protective photoresist. Additionally, the iodic acid powder settles and the water it was mixed in evaporates, which may increase recombination. Even reducing the diffusion time to 20 minutes for a 560°C diffusion and thinning it 100 nm did not result in a fully mesa-etched cell. Thus, the native oxide was kept for Cd cell fabrication, and diffusion temperatures at or above 550°C used.

Figure 4.11 illustrates the dark and light J-V curves for some of these cells to illustrate the potential, or lack thereof, of performing diffusions with the oxide removed. Table 4.11 compares performance parameters for the cells.

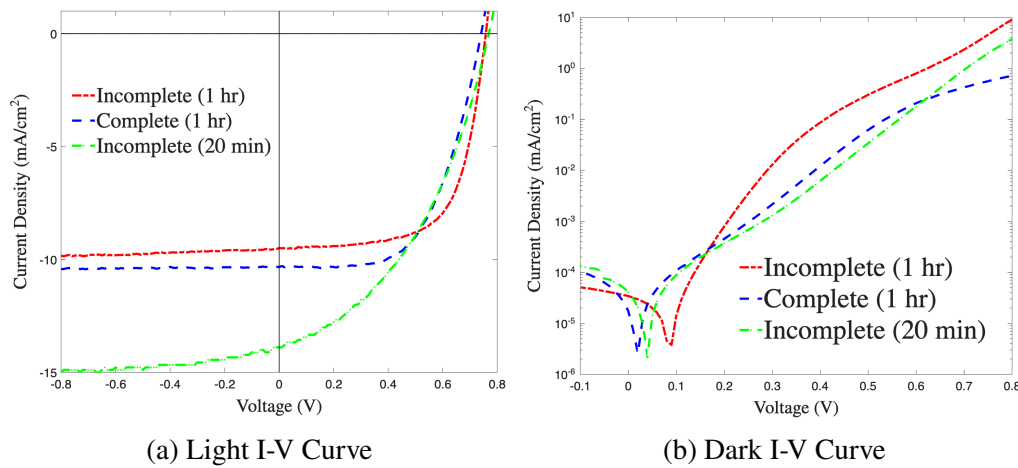


Figure 4.11: I-V curves of Cd-doped cells diffused with the native oxide removed. Diffusions of 1 hr, likely at 550°C, and 20 minutes at 560°C are included for comparison. The cell doped for 20 minute was also thinned by 100 nm.

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF	n	J_0 (mA/cm ²)
Incomplete (1 hr)	4.78	9.50	758.2	66.3%	-	$4.03 * 10^{-6}$
Complete (1 hr)	4.50	10.33	741.2	58.8%	2.41	$1.89 * 10^{-5}$
Incomplete (20 min)	3.29	13.91	769.4	41.8%	2.65	$1.16 * 10^{-5}$

Table 4.11: Figures of merit comparisons for 1 hr 550°C Cd-doped cells and a 20 min 560° cell. The 1 hr cell results were included before and after completing the mesa etch, while the 20 min cell had also been thinned 100 nm with iodic acid.

It must be emphasized that the percent efficiencies of the devices are not reflective of "true" device performance given the incomplete mesa etches. The 1-hr diffused cells were also damaged a bit by a diluted HCl acid that was attempted to achieve the mesa etching for these deeper diffusions, which likely harms the FF as well. However, these numbers highlight that removing the native oxides does not provide an immediate benefit in efficiency in comparison with the increased fabrication burden and yield challenges that result. The J_{SC} of the cell with the complete mesa etch in Table 4.11 is 37.7% better than the cell fabricated with the same diffusion conditions but with the native oxide intact as reported in Table 4.5. However, the V_{OC} is lower, dropping from 747.8 mV to 741.2 mV. This results in an overall higher efficiency for the two specific devices compared. However, the fabrication challenges that result from the oxide removal — which include the associated difficulty with keeping the photoresist intact during the longer mesa etch process and the resulting lower device yield — might not make this step worthwhile unless the mesa etch challenge can be overcome. The 35-min diffusion with the native oxide intact had a higher V_{OC} and a more reliable mesa etch process, but the J_{SC} is 13.3% lower.

A 20 minute Cd diffusion at 560°C was attempted, likely with the native oxide removed given the incomplete mesa etch. Although this is uncertain, it would make sense to have tried removing the native oxide with such a short diffusion time. The J_{SC} is 84.6% of the J_{SC} of the MOCVD cell, which is admirably close, and the V_{OC} is also higher than even the 35-min Cd diffusion with the native oxide intact. This set the stage for a potentially much higher device efficiency. However, the very low FF of 41.8% suggests high device resistance. The dark J-V curve shows that the 20-minute diffusion has a lower series resistance than the 1-hr diffusion, although the higher diode ideality factor suggests that there may be other recombination mechanisms going on, such as Auger recombination [49]. However, given that emitter thinning and a shorter diffusion time should result in a shallower junction and a lower surface carrier concentration, it is not obvious what the recombination

mechanisms at play would be. If the device resistances are due to surface contact issues, then a transparent top contact may help improve the surface conductivity to improve the FF.

Removing the native oxide does result in major improvements in both the possible achievable J_{SC} and V_{OC} values, which can result in higher-efficiency devices. However, in practice, the increased fabrication challenge due to the need for longer mesa etches and increased exposure to acids hurt device yield and introduce increased device resistance and recombination, which lowers the practical payoff of this step unless longer or faster mesa etches can be achieved in a robust manner. The J_0 is higher for the sample with the complete mesa etch than for the one with an incomplete etch, which makes sense given the greater acid exposure. It illustrates that the increased acid exposure does increase the recombination of the device, despite the photoresist. n was not calculated for the incomplete mesa etch because of the curve of the dark J-V graph, while the other dark J-V curves have a large voltage range in which the log graph is straight. One method could include identifying a more robust photoresist for the mesa etch or performing mesa isolation without acids, such as via laser ablation [113].

Figure 4.12 plots the IQE for the 1 hr and 20 min diffusions, with the previous native-oxide-intact 35 min Cd diffusion included for comparison. The IQE results

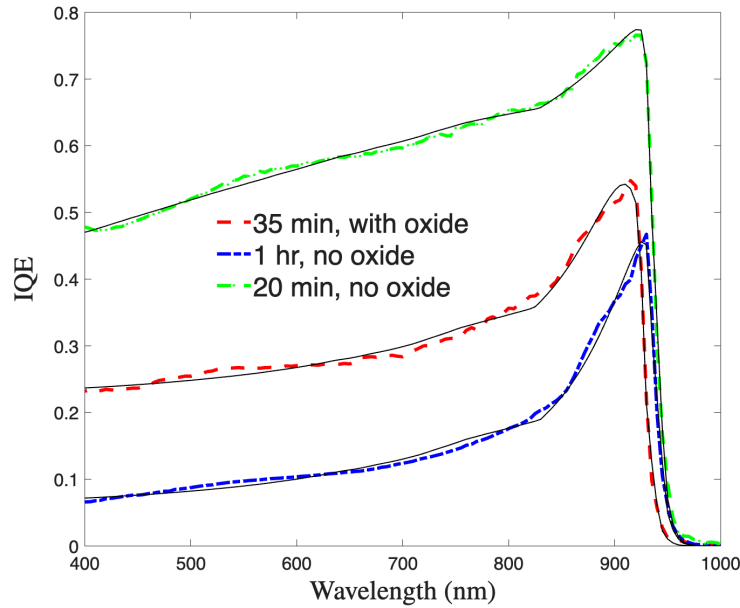


Figure 4.12: IQE measurements of diffusions with the native oxide removed. Diffusion durations of 1 hr and 20 min were included. The 35 min Cd diffusion with the native oxide intact was included for comparison.

should be taken with a grain of salt because the mesa etch was incomplete, so charges from neighboring cells are likely being collected. However, it suggests that a shorter diffusion time or otherwise shallower emitter can help the IQE approach that of the MOCVD reference cell. It also shows that a shorter diffusion time with the native oxide intact is preferable to a longer diffusion time without the oxide, but that if a mesa etch can be completed for a quick diffusion without the native oxide, carrier carrier collection may be improved.

Table 4.12 lists the extracted emitter widths, SRVs, L_n , and L_p for all three of those cells.

Parameters	1-hr	20-min	35-min
$N_{\text{emitter}} \text{ (cm}^{-3}\text{)}$	$\sim 1.7 * 10^{18}$	-	$1.5 * 10^{18}$
IQE Emitter Width	$1.18 \mu\text{m}$	$0.660 \mu\text{m}$	$1.09 \mu\text{m}$
Hall Emitter Width	$0.671 \mu\text{m}$	-	$0.167 \mu\text{m}$
SRV (cm/s)	$3.67 * 10^6$	$1.93 * 10^6$	$5.54 * 10^5$
$L_n \text{ (}\mu\text{m)}$	0.472	24.1	0.541
$L_p \text{ (}\mu\text{m)}$	3.15	8.01	1.42

Table 4.12: Extracted parameters from QE and Hall measurements for the Cd-diffused cells. The 1-hr cell was likely diffusion doped at 550°C while the 20-min and 35-min cells were diffusion doped at 560°C . N_{emitter} refers to the doping concentration estimated from Hall mobility measurements. Hall measurements were not taken for the 20-min diffusion.

Hall measurements were not taken for the 20-min diffusions, so the surface emitter doping concentration cannot be estimated for that sample. The model fit confirms that the 20-min diffusion has a shallower emitter than the 1-hr diffusion. The IQE fits do incorrectly suggest, however, that removing the oxide somehow results in shallower emitter widths than leaving the native oxide intact for a 35-min diffusion, which is known to be false given the larger mesa etch time required. The Hall emitter width estimate suggests the contrary, which would be more in line with what is expected empirically.

The fitted SRV values suggest that the 20-min diffusion yields a slightly better surface quality than the 1-hr diffusion. However, the difference in fitted values is minor, and could be a reflection of the individual diffusion run. It is still notable that, within the bounds of error for lab-scale diffusions, a 20-minute diffusion does not yield a notably superior surface quality as measured by the SRV. In fact, the

35-min diffusion with the native oxide intact seems to yield the best surface quality given the notably lower SRV. However, the electron diffusion length L_n is notably longer for the 20-min diffusion than for the 1-hr diffusion, which intuitively makes sense given that reduced diffusion time would result in less sample damage beneath the surface. It is surprising, however, that 35-min diffusion with the native oxide intact did not yield a significantly better L_n than the 1-hr diffusion without the oxide, and that the L_p was actually the worst for that sample. Perhaps it is a reflection of the individual diffusion run for that sample. The L_p was higher for the 20-minute diffusion than the 1-hr diffusion, which is what would be expected.

Table 4.13 lists the parameter ranges used for the IQE fits for the 1 hr and 20 min diffusions. The lower values of c necessary for converging fits where the c value did

Parameters	1-hr	20-min
c	0.95-1.05	0.91-1.01
W_e	0.7-2	0.5-2
L_n	0.1-5	1-25
L_p	0.1-20	1-10
W_d	0.1-0.4	0.1-0.4
K_p	0.01-1000	0.01-1000
K_q	0.01-1000	0.01-1000
$ d\lambda $	4.5	3.5

Table 4.13: Parameter ranges for the IQE model in Sze to fit the IQE curves for 1-hr and 20-min diffusions with the native oxide removed. The 1-hr diffusion was likely carried out at 550°C while the 20-min diffusion was carried out at 560°C.

not run right up against a user-defined limit are notable because the IQE seems to be lower than would be expected given the fitted model parameters and associated physical device characteristics. $c \approx 0.92$ for the 20-min diffusion, which is smaller than the $c \approx 0.96$ for the 1-hr diffusion. Meanwhile, Table 4.7 shows that the IQE response for the 35-min diffusion is greater than would be expected given the device parameters. The emitter width ranges are larger for the 20-min diffusion than the 1-hr diffusion while the L_n and L_p ranges for the 20-min diffusion have a higher minimum value, as expected given the longer diffusion lengths that would result from shorter diffusions and less damage.

SIMS Measurement Attempts

SIMS measurements were attempted to concretely measure the diffusion depth of the devices. Figure 4.13 illustrates the measured SIMS profile. The sample was

diffused at 550°C for 1 hr. However, the predicted profile depth, based on the

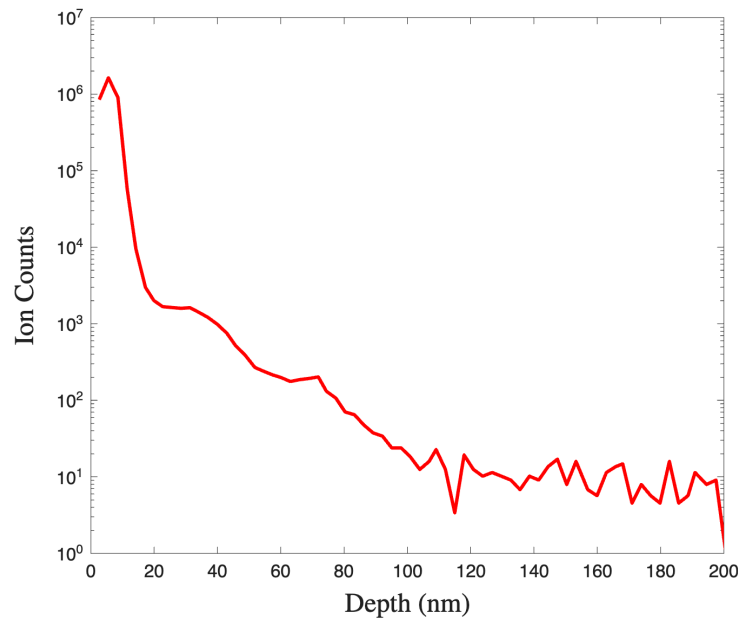


Figure 4.13: SIMS measurement of a sample doped with Cd for 1 hr at 550°C.

measurement time and resulting crater depth as measured by profilometry, looks to be around 140 nm. This was much shallower than expected through both IQE fits and necessary etch times for complete mesa etches. This is in part because while extensive calibrations exist for GaAs SIMS, such extensive calibrations do not exist for InP. Given that, further SIMS measurements will be left to future work.

What is noteworthy, however, is the qualitative observation that the doping concentration drops off rapidly from the surface compared to literature doping profiles. This suggests that the tradeoff between leaving the native oxide intact versus removing it before doping is in the ability to obtain a flat, relatively-abrupt doping profile. This means that thinning the surface will result in a notably lower surface carrier concentration. This makes for a less effective emitter and potentially greater contact resistance with the metal. This result illustrates the risk of diffusions with the native oxide layer intact. Shallower diffusion profiles come with limited upside from emitter thinning in this case.

Future work would benefit from measuring diffusion profiles from diffusions with the native oxide layer removed to confirm the profile shape obtained in the lab setup here. From there, it may be worth making cells from samples diffused without the native oxide layer followed by significantly more aggressive emitter thinning to compensate for the deeper diffusion profile.

4.7 Zn-Doped Cells

Next, Zn doping was attempted, including the post-diffusion annealing step to ensure adequate electrical activation.

Initial Zn Doping and Cell Fabrication Attempts

The substrates that would be doped with Zn were also cleaned with the procedure outlined by Sun et. al. to remove the surface oxide layer and allow for easier diffusion at lower temperatures, since Zn diffusions in particular seem to exhibit higher diffusion depths [134] [141]. However, given that the oxide layer seemed to act as a stopping layer to help achieve shallower p-n junctions in Cd-doped cells, future work will investigate this effect for Zn-doped cells as well. Fabricating Zn-doped cells also required a post-diffusion anneal to electrically activate all the Zn dopants. This was done by removing the Zn_3P_2 powder, placing the samples in an open-air quartz boat, and annealing them for 35 minutes at 520° . Table 4.14 summarizes the diffusion and anneal temperatures and times for the Cd and Zn doped solar cells. Fig. 4.14 shows the dark and light I-V curves of the Cd and

Source	Diffusion Temp / Time	Anneal Temp / Time
Cd_3P_2	560° / 35 min	N/A
Zn_3P_2	530° / 60 min	520° / 35 min

Table 4.14: Summary of diffusion and anneal parameters. The Cd-doped cells with Cd_3P_2 as the diffusion source were not annealed after diffusion, while the Zn-doped cells with Zn_3P_2 as the diffusion source were annealed.

Zn-doped cells, along with the curves of the MOCVD-grown epitaxial cells for comparison. Table 4.15 summarizes key solar cell parameters obtained from the light and dark I-V curves of the cells in question. Table 4.16 reports the device

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF	n	J_0 (mA/cm ²)
Cd	4.94	8.96	762.3	72.4%	2.02	$1.74 * 10^{-6}$
Zn	1.88	3.86	738.0	66.1%	2.00	$2.89 * 10^{-6}$
MOCVD	9.08	14.92	832.8	73.1%	2.14	$1.39 * 10^{-6}$

Table 4.15: Figures of merit comparisons for Cd and Zn-doped cells, as well as an MOCVD cell for comparison.

parameters extracted from IQE model fits.

The emitter doping concentration for the Cd-doped cells was estimated from mobility values using Hall measurements obtained before cell fabrication, and we assume

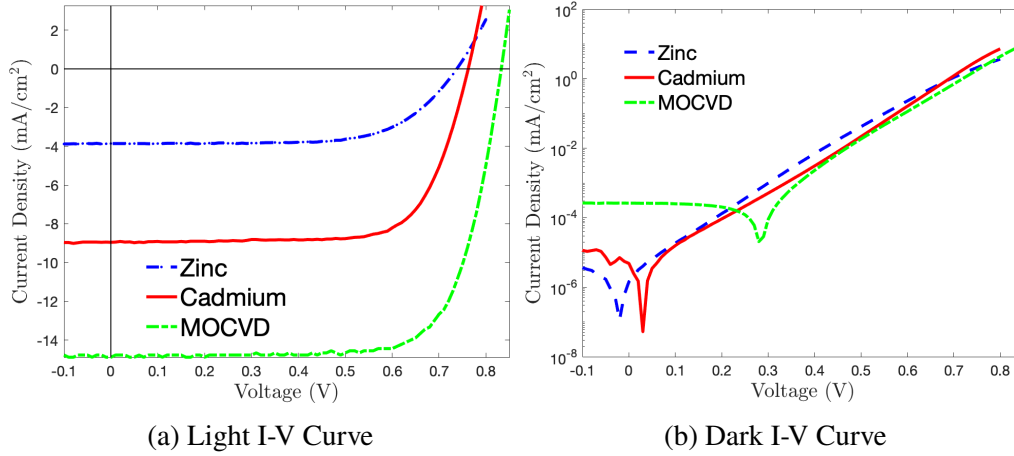


Figure 4.14: I-V curves of two of the Cd and Zn-doped solar cells along with the MOCVD-grown cell.

Parameters	Cd	Zn	MOCVD
N_{emitter}	$1.5 * 10^{18}$	N/A	10^{18} cm^{-3}
IQE Emitter Width	$1.10 \mu\text{m}$	$2.00 \mu\text{m}$	$0.05 \mu\text{m}$
SRV (cm/s)	$9.40 * 10^5$	$2.05 * 10^7$	$9.76 * 10^6$
L_n	$0.614 \mu\text{m}$	$9.02 \mu\text{m}$	$1.36 \mu\text{m}$
L_p	$0.614 \mu\text{m}$	$1.05 \mu\text{m}$	$3.30 \mu\text{m}$

Table 4.16: Extracted parameters from I-V, QE, and Hall measurements. N_{emitter} refers to the doping concentration in the emitter layer (p^+ for the diffusion-doped cells, n^+ for the MOCVD cell). The table reports L_n and L_p .

constant carrier concentration with depth in the diffused layer. [56]. Hall measurements were attempted for the Zn-doped samples but the measurements did not make sense and did not correspond to device performance. The Hall measurements suggested that the samples were not doped, but that was not the case. The table also includes estimated emitter widths as well as the minority carrier diffusion lengths in the emitters from QE fits.

These preliminary results suggest several things. First, we have demonstrated a proof-of-concept for successful fabrication of low-cost, Zn-doped InP solar cells as well as an improvement in Cd-doped solar cell performance metrics with a higher diffusion temperature and lower diffusion time than previously reported. The fill factor of the improved Cd-doped cell is comparable to that of the MOCVD device, and the diode ideality factors n and the dark current density J_0 of both diffusion-doped cells are also comparable to the MOCVD cell. This suggests that the recombination mechanisms are similar, suggesting improving the J_{SC} of the diffusion-doped cells

will result in much higher efficiencies. Further work is needed to fabricate the cells more consistently and improve the recombination mechanisms at play. The Cd-doped device's J_{SC} is less than half of the MOCVD cell's J_{SC} , and the Zn-doped device's J_{SC} is even smaller. This makes sense because the p-n junctions are much deeper into the device for the diffusion-doped cells than in the MOCVD-grown cell, and the Zn diffusions were deeper than the Cd diffusions based on the required times for the mesa etches. Since most of the carrier generation occurs at the p-n junction, this means they would be further from the contacts, making carrier collection more difficult. Further work is needed to obtain precise diffusion profiles and determine the depth of the p-n junction via methods such as secondary ion mass spectroscopy (SIMS) to determine the diffusion depths and constrain the QE fits to obtain truer values for the other parameters such as L_n . In addition, the V_{OC} of both cells is lower than that of the MOCVD-grown cells. We can further optimize diffusion parameters such as duration and temperature for improved surface quality and passivation. It is worth noting that no anti-reflection coating (ARC) was used for these devices, which means that as much as 45% of the short-wavelength light was reflected from the device surfaces [16]. Well-optimized ARCs should improve the J_{SC} 's of these devices.

Table 4.17 lists the parameter ranges used for the IQE fits for the 35-min Cd and the 1-hr Zn diffusion.

Parameters	Cd	Zn
c	0.99-1.08	1.11-1.22
W_e	0.9-2	2-4
L_n	0.1-5	1-10
L_p	0.6-5	0.9-10
W_d	0.1-0.4	0.1-0.4
K_p	0.1-1000	0.1-1000
K_q	0.1-1000	0.1-1000
$ d\lambda $	3.5	3.5

Table 4.17: Parameter ranges for the IQE model in Sze to fit the IQE curves for 1-hr and 20-min diffusions with the native oxide removed. The 1-hr diffusion was likely carried out at 550°C while the 20-min diffusion was carried out at 560°C.

Fig. 4.15 presents the internal quantum efficiency (IQE) fits of the diffusion-doped cells as well as the MOCVD-grown cell. A handful of noisy data points were removed from the MOCVD EQE measurements to improve the fits. Fewer than 10 points out of more than 100 were removed. Fitting the Zn cell IQE was much

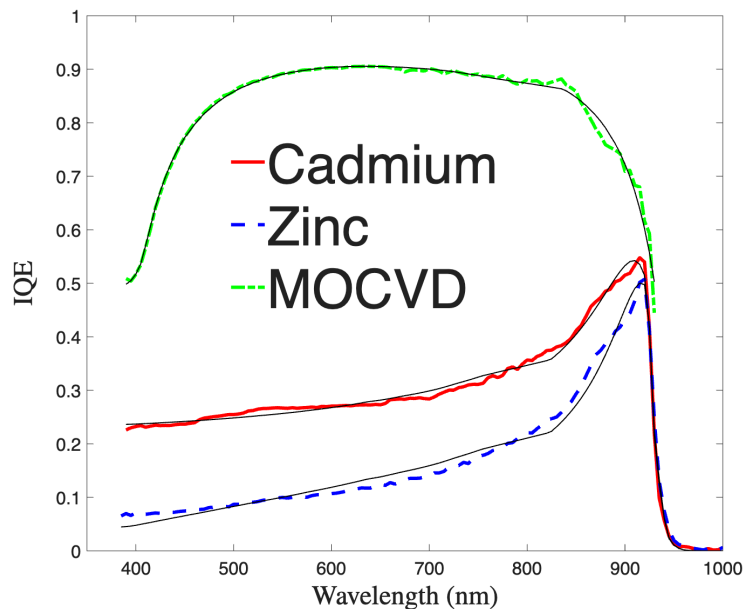


Figure 4.15: IQE measurements of the 35-min Cd and 1-hr Zn diffusion-doped cells and the previously-fabricated epitaxial cell. The fits are plotted in the thin black lines to illustrate the quality of the fit upon which the parameters were based.

more challenging than fitting the Cd cells' IQEs. The range of c values had to be changed, and the permitted emitter widths and diffusion lengths were larger. The need for larger diffusion lengths and wider ranges was surprising given the inferior performance and IQE curves of the Zn cells. It is likely that something about the diffusion profile of Zn makes these cells more challenging to model and perhaps makes the basic Sze IQE model break down for Zn. Thus, the fitted parameter values are less reliable and were found to be much more sensitive to parameter range tweaking during the fits. It is included here for completion, but will not be included in comparisons of future Zn cells. However, examining the IQE curves can still tell us useful information about the cells.

The graphs illustrate that carriers generated near the surface of the diffusion-doped cells are not efficiently collected. The data is fitted to the quantum efficiency expression given in Sze to obtain parameters such as the surface recombination velocity (SRV) and the emitter width, reported in Table 4.3 [121]. The Zn-doped cell had a lower overall IQE than the Cd-doped cell, which makes sense given the deeper p-n junction because more of the short-wavelength light would be absorbed by the emitter rather than the depletion region than in the Cd-doped cell. Both exhibit significantly less short-wavelength absorption than the MOCVD counterparts. Further work is needed to establish a relationship between emitter depth and

short-wavelength carrier transport in the device.

The fitted SRV for the Cd-doped cell was lower than that of the Zn-doped and MOCVD-grown cells, but all were within the same order of magnitude. All cells have high SRVs in comparison with the values for InP in the literature, indicating that investigating passivation paths and minimizing acid-induced damage can help improve surface quality, and from there yield better device efficiencies through higher V_{OCs} . We used the mesa etch-informed knowledge of the deeper diffusion depth of the Zn-doped cell to constrain the emitter widths to above $2\text{ }\mu\text{m}$ for the Zn-doped cell and below $2\text{ }\mu\text{m}$ for the Cd-doped cell. The MOCVD-grown structure had a known emitter width of 50 nm. Further work needs to be done to determine the p-n junction depth experimentally and the tradeoff between emitter thinning and device efficiency.

Zn Doping with InP Native Oxide as a Stopping Layer

Since the Cd-doped cells were found to perform better when diffusions were done with the InP native oxide left as a stopping layer, Zn diffusions with the InP native oxide intact were also performed. It was found that with the native oxide as a stopping layer, increasing the temperature to 540°C and maintaining a duration of 1 hr did not suffice to observe Zn doping. A 2-hr doping was needed. The anneal time was reduced to 20 minutes. Hall measurements were unable to be properly read — the corner contact resistances were not ohmic — so an accurate reading of the surface carrier concentration was not obtained. However, improved solar cells were able to be fabricated, particularly after thinning. Notably, however, the 30-minute mesa etch with the 10% iodic acid, corresponding to a 65 nm/min etch rate, was not sufficient for a complete mesa etch, which suggests that the emitter depth is greater than $1.8\text{ }\mu\text{m}$. See the Appendix for more mesa etch-related troubleshooting tips, particularly for long mesa etch times with iodic acid.

Table 4.18 reiterates the parameters with and without the oxide layer tested for Zn diffusion thus far. The anneals were both performed at 520°C

Diffusion Temp / Time	Anneal Time	Oxide
$540^{\circ} / 2\text{ hrs}$	20 min	Yes
$530^{\circ} / 1\text{ hr}$	35 min	No

Table 4.18: Summary of diffusion and anneal parameters. The anneals are all performed at 520°C .

Performance Improvement from Emitter Thinning

The cell that was not thinned did not exhibit a complete mesa etch. However, the cell that was thinned 100 nm exhibited a completed mesa etch, so its results will be presented. Figure 4.16 presents the J-V light and dark curves of this thinned 540°C cell, along with the 35-min 560°C Cd cell and the first Zn cell for comparison. Table 4.19 presents the figures of merit for these three cells.

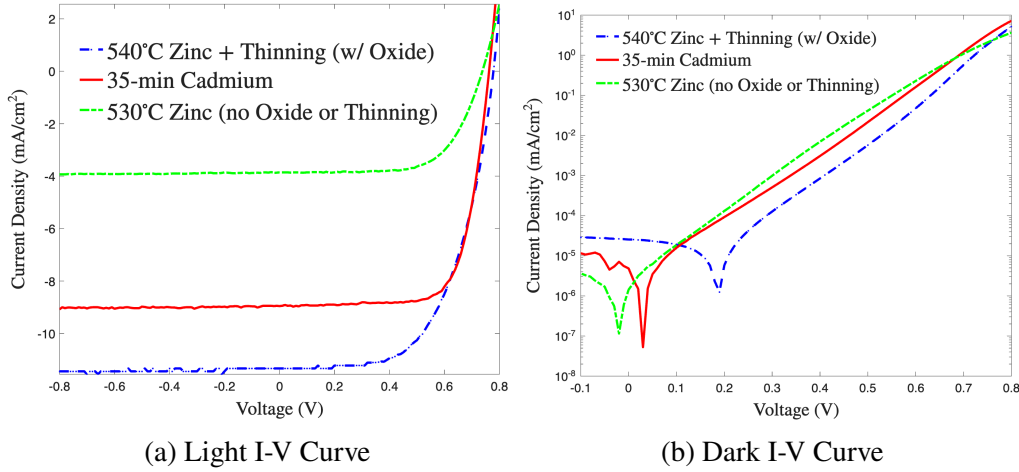


Figure 4.16: I-V curves of the 540°C Zn-doped cell with 100 nm thinning, compared to an unthinned 530°C Zn cell and a 35-min 560°C unthinned Cd cell.

Cell	% Eff	J_{SC} (mA/cm ²)	V_{OC} (mV)	FF	n	J_0 (mA/cm ²)
Zn (540°C)	3.85	11.33	778.1	59.4%	1.93	$1.62 * 10^{-7}$
Zn (530°C)	1.88	3.86	738.0	66.1%	2.00	$2.89 * 10^{-6}$
Cd	4.94	8.96	762.3	72.4%	2.02	$1.74 * 10^{-6}$

Table 4.19: Figures of merit for the 540°C Zn-doped cells that were thinned 100 nm. The figures of merit for the 530°C Zn-doped unthinned cell and the 560°C 35-min Cd-doped unthinned cell are provided for comparison.

Frustratingly, though the J_{SC} and V_{OC} were both improved drastically by doping with Zn for 2 hours at 540°C with the oxide layer intact compared to both the 35-min Cd cell at 560°C with the oxide and the 530°C 1 hr Zn doping with no oxide layer, the efficiency was still worse than that of the Cd-doped cell. This is because the FF was much lower — 59.4% for the 540°C Zn-doped cell as opposed to 72.4% for the Cd-doped cell and even 66.1% for the 530°C Zn-doped cell. However, the dark saturation current density J_0 was lower for this cell than for the other cells, which suggests lower recombination. This is backed up by the higher V_{OC} achieved by this

device. The low FF despite the high V_{OC} and J_0 suggests a high series resistance from the overall device, which could be because of the following reasons:

- High metal contact resistance, either from the metal stack itself or the metal-semiconductor surface.
- High resistance within the device, such as the emitter-base junction.

Since thinning removes the heaviest-doped portion of the doping profile, the surface of a thinned cell has a lower doping than that of an unthinned cell. Given how rapidly the doping concentration drops off in samples doped with the native oxide layer intact, this could mean high resistance between the emitter and metal contact. This is the likely cause of the low FF because the J_{SC} is much higher than for the other cells, so the lower surface emitter concentration is not hurting the carrier collection in the device. A lower-doped emitter could also mean high lateral resistance, which can be countered with a TCO layer on top, such as ITO, under the metal contacts. Future work can try the following to address this low FF:

- Diffusion after native oxide removal followed by aggressive emitter thinning;
- Different thicknesses for the Zn, Au, and Ag layers, along with varying anneal temperatures and times, for the ohmic contact to the p-InP surface emitter;
- TCO layer on top of the emitter and below the top metal grid contacts;
- Increase the Zn post-diffusion anneal time to potentially electrically activate more of the Zn;
- Further tune diffusion temperatures and times to alter the diffusion profile.

Figure 4.17 plots the IQE plots of the 1-hr and 2-hr Zn diffusion-doped cells, along with the 35-min Cd-doped cell for comparison. Even the 1-hr Zn diffusion doped cell was challenging to fit and get to converge to physically-sensible values without hitting the limits of the permitted range of c and $|d\lambda|$. Thus, the fitted parameters of the 2-hr Zn diffusion-doped cell are not provided.

Despite the difficulty in fitting, the IQE plots alone illustrate the extent of improvement achieved by pairing a stopping layer, via keeping the native oxide in this case, with a longer Zn diffusion and emitter thinning. The stopping layer likely helped the

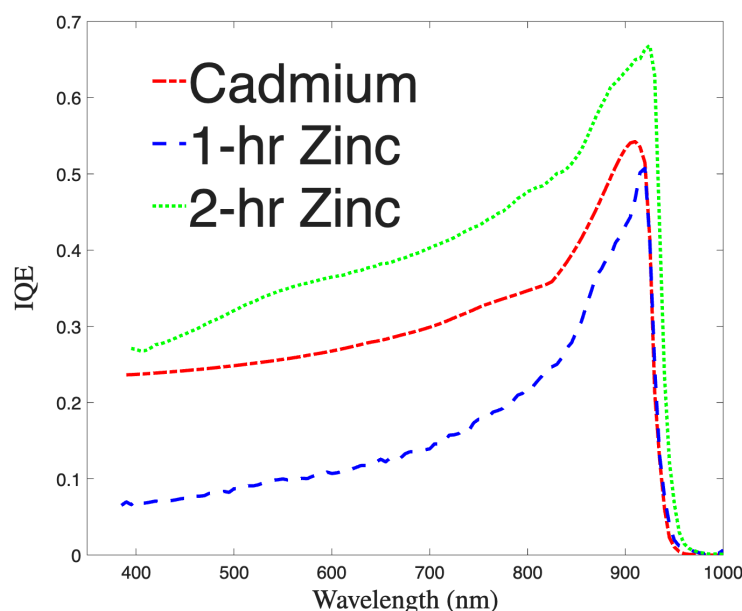


Figure 4.17: IQE measurements of the 35-min Cd and 1-hr and 2-hr Zn diffusion-doped cells.

junction be shallower even with the longer diffusion time than for the 1-hr oxide-less diffusion. Combined with emitter thinning, this greatly improved the short wavelength charge carrier capture. Its IQE was better than even the 35-min Cd cell, which makes sense given the higher J_{SC} the 2-hr Zn cell was able to achieve. This boost was seen across all wavelengths shorter than the bandgap.

Comparing Best V_{OC} s

Though incomplete mesa etches result in a higher J_{SC} than reality, they result in lower or equivalent V_{OC} , reflecting that of the worst cell. The V_{OC} of a chip with an incomplete mesa etch does not add those of the component cells, so the best V_{OC} s at different doping conditions can be compared. Table 4.20 lists the best V_{OC} s recorded thus far for the different cells fabricated.

Cell	V_{OC} (mV)
35-min Cd (560°C)	769.2
20-min Cd (560°C, No Thinning)	771.0
20-min Cd (560°C, 100 nm Thinning)	769.4
2-hr Zn (540°C, No Thinning)	776.4
2-hr Zn (540°C, 100 nm Thinning)	778.1

Table 4.20: Best V_{OC} for the cells fabricated thus far. The Zn cells reported in this table had the native oxide intact during diffusion.

The V_{OC} of the 20-min Cd cell did not improve after 100 nm emitter thinning, but rather slightly declined. The V_{OC} of that cell after 100 nm emitter thinning was actually on par with the 35-min Cd doping. Meanwhile, thinning the Zn cell slightly improved the device's V_{OC} . This may suggest a difference in the shape of the Zn versus Cd diffusion profiles. However, further tests would be needed to confirm this is a real phenomenon and not just a one-off due to the low yield and uneven inconsistent dopings in these processes.

However, the V_{OC} of the Zn-doped cells is consistently higher than the Cd-doped cells, which suggests that optimizing the Zn diffusion and post-diffusion anneal parameters can yield more efficient solar cells. This will be especially true if the low FF issue can be solved. This also has the advantage of being able to use longer diffusion times, likely leading to more controllable and consistent diffusions because minor deviations in diffusion time would likely have less relative impact on the final device for a 2-hr Zn diffusion than a 35-min Cd diffusion.

4.8 Conclusion

This work on InP diffusion doping using Cd and Zn-based dopants establishes a solid starting point for future work to optimize InP diffusion-doped cells. It used a leaky-tube diffusion approach to balance the advantages of open-tube and closed-tube diffusions. It then investigated Cd and Zn diffusions using Cd_3P_2 and Zn_3P_2 powders, both with and without native oxide layers.

Below are the parameters for the best Cd and Zn-doped solar cells achieved in the work thus far:

- Cd (4.94% efficiency): 35 min diffusion at 560°C with the native oxide layer intact;
- Zn (3.85% efficiency): 2 hr diffusion at 540°C with the native oxide layer intact.

And the SIMS profile demonstrated that, at least with the native oxide intact, the Cd dopant concentration dropped off abruptly beyond the surface, which may limit the effectiveness of emitter thinning.

Based on the findings thus far, future work could benefit from the following directions to improve cell performance:

- Depositing a TCO layer such as ITO between the doped InP surface and the grid metal contacts to improve the FF for the following cells to optimize the cells' performances:
 - Thinned 2-hr 540°C Zn-doped cell with the native oxide intact;
 - Thinned 20-min 560°C Cd-doped cell with native oxide removed;
 - Thinned cells more broadly, most likely.
- Attempting to fabricate more cells without the native oxide layers and compensating with more aggressive emitter thinning to maintain a higher surface doping concentration even after thinning.
- Further increasing the Zn post-diffusion anneal times to see if greater electrical zinc activation is achieved, which can also improve performance post-thinning.
- Removing the native oxide and trying other cap layers, such as a P-rich cap layer similar to the ones alluded to earlier in this chapter from the literature.
- Laser ablation for mesa isolation of such deep junctions to bypass altogether the surface damage-related challenges of acid-based chemical mesa etching.

Thoroughly understanding the performances of these devices upon making these changes will likely require some combination of the following measurements, with the high-priority ones bolded:

- **Light and dark J-V curves;**
- **EQE measurements;**
- **SIMS measurements** to at least qualitatively determine the diffusion profile;
- **Hall measurements** of thinned samples to accurately determine the carrier concentration at different depths and construct a diffusion profile that way;
- Reflection measurements for the surfaces to accurately determine the IQE;
- Wavelength-dependent absorption coefficient measurements for the diffused InP sample.

Beyond these initial optimization directions, the following work needs to be undertaken to achieve scalable, low-cost InP diffusion-doped cells:

- Radiation hardness testing of p^+n diffusion-doped InP cells as is, both for optimized Cd and Zn-doped cells
 - Electron irradiation
 - Proton irradiation.
- Spalling p^+n Cd-doped and Zn-doped InP wafers
 - Handling spalled samples tends to require glass slides and tape, which makes it impractical to dope samples after spalling, and since doping modifies the surface, it will save time to optimize spalling parameters according to the surface of a doped sample from the get-go.
 - InP wafers can be (100) or (110). (100) wafers yield corrugated surfaces after spalling, while (110) wafers yield flat surfaces after spalling [72]. Both have potential benefits and drawbacks, but this thesis work was done on (100). There may be process differences when moving from (100) to (110) due to the modified crystal orientation and its impact on dopant motion through the crystal as well as the spalling morphology and necessary film thickness to get intact spalled samples for corrugated versus flat films.
- Attempting diffusion doping AFTER spalling
 - Previous literature results achieved InP film thicknesses of $15\text{ }\mu\text{m}$ [44]. This is thicker than the diffusion depths of Cd and Zn in InP at the temperatures and diffusion times run in this work. This work also handled spalled samples by attaching an InP film with a Ni stressor layer onto Ni foil. A quick search on Perplexity suggests that Ni can be put in a tube furnace with forming gas flowing through it at temperatures of 600°C , so it MAY be possible for a clever researcher to figure out how to diffusion dope a spalled InP film.
 - This would solve the problem of needing to flip over the spalled film AND removing the Ni adequately before depositing Au-Ag-Zn grid top contacts and allow the Ni stressor layer used for the spalling to double as the bottom contact to undoped InP.
 - The researchers in [44] did face problems with spalled film warping, which complicated post-spalling fabrication steps, particularly at elevated temperatures. This could also pose a problem in the post-spalling

diffusion doping, since warping could make the doping non-uniform across the surface, which would in turn result in inconsistent device fabrication and lower device yield across fabrication runs.

- Fabricating solar cells from spalled p^+n Cd and Zn-doped cells
 - The work of Andrew Nyholm elaborates more on spalled solar cell fabrication, which will likely involve removing the Ni layer used for spalling the InP film and flipping the film over to deposit grid contacts on the doped surface and perform the mesa etch.
 - Handling the spalled sample for the remaining contact deposition and mesa etch steps will be a challenge, and will involve tape and care. This will be especially true if dealing with corrugated spalled surfaces for (100) InP.
 - This would look different if successful post-spall diffusion is achieved — then, all that would be needed are grid top contacts and a mesa isolation.
- Radiation hardness testing of spalled p^+n diffusion-doped solar cells, both for optimized Cd and Zn-doped cells
 - It could be worth comparing the radiation hardness of corrugated spalled (100) InP solar cells with flat spalled (110) InP solar cells, if both can be fabricated successfully, since the surface texturing may improve radiation hardness just like NWs did.
 - Investigating both electron and proton irradiation would be ideal if possible.
- Wafer-scale spalling and solar cell fabrication
 - This will require a new photolithography mask for the mesa etch and grid contacts where the pattern is big enough to accommodate the wafer.
- Actual orbital flight data for any or all of the cells above.

Ideally, there would be multiple people working on these different attempts. Especially with the post-diffusion cool-downs of the furnaces needed, having one person try to execute this in a linear fashion leads to very long times before any feedback can even be obtained on whether a given diffusion run yields sufficiently good fabricated baseline cells to even perform any follow-up modifications, such as emitter thinning

or ARCs, to attempt and improve the cells. With the device yield of this process having been low, this can be particularly frustrating. Having one student do all this alone from the ground up might very well crush their soul and kill their spirit.

Chapter 5

CONCLUSION

5.1 Summary

This thesis explored multiple approaches to achieving sustainable, scalable, low-cost space solar power. Space solar cells require not only sufficiently high power-conversion efficiency but also intrinsic radiation hardness to reduce shielding weight and the resulting launch costs.

This need for radiation hardness inspired the initial exploration of NW solar cells. The previously-demonstrated radiation hardness of NW solar cells, combined with the promise of scalability via nanoimprint lithography, inspired the investigation of this pathway despite the challenges with nanolithography-based fabrication. Simulation results illustrated the potential for NW cells to achieve similar efficiencies as their planar counterparts, which would have promising ramifications for NW solar cells for space that would last longer without a sacrifice in overall lifetime performance from start to finish. However, after experiencing first-hand the difficulty of consistent NW fabrication and the long process times involved with InP etching due to the toxic gases that need to be cleared out before and after etching, this work concludes that NW solar cells are not a desirable pathway to focus on if low cost and scalability are priorities.

Then, after fabricating MOCVD-grown planar solar cells to establish a reference baseline for comparison, this thesis explored diffusion-doped cells using Cd and Zn-based dopants. Both had their benefits and drawbacks related to safety, electrical properties, and more, so cells were fabricated using both dopants. The work thus far has achieved better device efficiencies with Cd cells, but Zn-doped cells, both before and after thinning, were able to achieve better V_{OC} than Cd-doped cells after thinning. There is a chance its J_{SC} could be better too, especially after thinning, if the mesa etch of even the 20-min Cd-doped cell were complete.

5.2 Future Directions

Detailed future work ideas for MOCVD-grown and diffusion-doped thin-film cells were outlined in Sections 3.8 and 4.8. However, given all the challenges described in the thesis with diffusion doping, many of which have not been fully resolved and can

create problems further along when spalling is introduced, **serious consideration should be given to ESC cells** such as the ones in [165] and [90] for fabricating spalled thin-film InP solar cells. Though such cells are more sensitive to surface quality and stoichiometry challenges that may arise from the deposition process, it provides the following advantages:

- Bypasses the need to optimize diffusion doping parameters — there are likely more folks around who have deposited at least TiO_2 , even if not Ta_2O_5 , compared to the folks who have done diffusion doping on InP in particular. This difference matters, as discussed in Section 4.1. **NOTE: This includes avoiding the painful, seemingly-infinite rabbit hole of comparing diffusions with and without the native oxide!**
- Heterojunction fabrication is quicker than diffusion doping — If you can book the ALD and an ITO sputterer back-to-back, the total process for depositing a ~ 10 nm TiO_2 layer and a ~ 60 nm ITO layer would take around 4 hours. In contrast, because of the furnace cool-down period, necessary, a Cd diffusion would take ~ 6 hrs while a Zn diffusion + post-anneal would take around twice as long (~ 12 hrs).
- This process is also less dangerous and less prone to clumsiness-induced user error from lack of dexterity than diffusion doping, which involves carefully carting around pumped-out quartzware, loading and unloading long tubes without cracking them or injuring yourself, inserting quartzware adequately centered into the furnace without burning yourself or inhaling toxic Cd fumes, and so on.
- Due to the lower surface recombination in InP compared to GaAs [94], and the fact that ALD-deposited TiO_2 and Ta_2O_5 have been used to make InP ESC solar cells in 3.8 and 4.8, the ESC deposition process is likely more substrate-agnostic than diffusion doping to begin with. Moreover, any differences due to different surface properties would likely work in favor of InP rather than against it, as is the case in diffusion doping.
- Eliminates the need for emitter thinning, which avoids all the hassle around etching the surface and the associated surface damage.

- Allows for short mesa etches to electrically isolate neighboring cells on a substrate, rather than the long mesa etches needed for deep diffusion-doped junctions. This further reduces performance loss due to surface damage.
- Allows for Zn-based p-InP Ohmic contact to be deposited before the ESC deposition, rather than afterwards, even if spalled film handling complexities are introduced. This is important because the Zn-based contact HAS to be deposited AFTER the InP is doped, and the contact anneal needed to achieve ohmicity likely makes the Zn diffuse deeper into the substrate and makes the p-n junction deeper. Using an ESC-based approach bypasses this challenge altogether.

Moreover, spalled heretofunction cells have already been demonstrated in the literature [44], so there is a quicker, better-established pathway to fabricating sufficiently high-efficiency thin-film cells that can then undergo radiation hardness testing to actually evaluate their performance for space.

Challenges with this approach would include:

- Ensuring TiO_2 (the likely choice, since Ta_2O_5 is less common) is deposited well via ALD and the interface between it and the InP surface is high-quality
 - Jared Sisler, who is currently in charge of the ALD, said that it achieves high-quality films pretty easily without painstaking optimization.
- Successfully executing ITO deposition such that the TiO_2 -InP interface remains high quality and the ITO is sufficiently conductive and transparent.
 - The author cannot speak to how challenging this will be in practice, although there should be people who can help out with ITO deposition. At the very least, someone in the KNI — Alex Wertheim as of the writing of this thesis — should be able to help out with ITO deposition in the KNI sputterer, although that sputterer does deposit other materials as well, which can cause contamination.
 - As of the writing of this thesis, Prof. Atwater's lab has a dedicated ITO sputterer, but this may change over time, though seemingly mostly for TiO_2 sputtering. As of the writing of this thesis, Holland, Julie, and Mina are looking to sputter ITO.

- Executing successful ALD on corrugated spalled InP may prove to be a challenge, if that side of the spalled (100) sample is chosen as the top side with the ESC.
 - Jared did also say that ALD is pretty conformal, but of course actual execution is left to the user. The author cannot comment on this from personal experience.

Additionally, general challenges for spalled cells include:

- Film warpage, which will affect post-processing handling and steps such as contact deposition, mesa isolation, and potentially diffusion doping / ESC and TCO deposition, depending on the process workflow chosen.
- Process "order of operations," especially if removing the Ni stressor layer is required
 - If diffusion doping, then grid top contacts would need to be deposited on the doped emitter, which would be covered with a Ni stressor layer for spalling. Those contacts would also need to be annealed, which would likely make the p-n junction penetrate deeper.
 - If fabricating heterojunctions, the workflow is already laid out in [44], with the caveat that now the cell has a p-type base instead of an undoped or n-type base. However, execution would be a challenge, and as of the writing of this thesis, no one is actively working on this.

Future researchers working on thin-film InP solar cells for space have multiple options and directions of exploration based on their judgments and hypotheses about the promise of different options. This work aimed to document in detail the progress and pitfalls of NW, MOCVD, and diffusion-doped cells.

Two further pieces of unsolicited advice include:

- Try to get as clear a sense as possible about the challenges and pitfalls encountered in the past or that could be encountered in the future.

This work attempts to do some of that, including in the troubleshooting tips outlined in Appendix B and the brainstorming around heterojunction ESC solar cells laid out earlier in this section. It can help save time by proactively

adapting accordingly and mentally set expectations to do so. But it is worth undergoing this exercise proactively before diving into new experimental procedures as well.

Papers may or may not include this information — very few do in practice — but theses are more likely to thoroughly document such obstacles and pitfalls. AI tools such as Perplexity, Gemini, or ChatGPT can help both brainstorm ideas "itself" and locate hard-to-find theses, conference papers, and more that might contain the relevant information needed.

- When given freedom over the overall direction of inquiry, such as diffusion doping versus heterojunction ESC cells, do not underestimate the importance of picking a direction whose day-to-day work and obstacles are more in line with your strengths, preferences, and working style.

Diffusion doping and ESC heterojunction fabrication, for instance, involve different equipment, different process workflows with their own pros and cons, and so on. Similarly, InP and Si have drastically different dry etch times in the cleanroom for identical structures because of the toxic gases involved in InP etching, increasing cleanroom time from 1 hr for 1.6 μm Si NWs to 4 hrs for 1.6 μm InP NWs. Such factors can drastically affect your quality of life and day-to-day satisfaction in your research endeavors.

Try to ask people who use similar tools about their workflows and what they like or dislike about them to get a sense of what you are getting yourself into. Likewise, AI tools might be able to help answer some of these questions and at least get a better sense of what to expect than going in completely blind, especially if embarking upon a procedure for which you cannot find an in-person source to show you the ropes.

This work serves as a thorough documentation of the progress and pitfalls towards sustainable, scalable, low-cost InP-based space solar power. It includes an honest detailing of nitty-gritty, "quotidian" simulation and fabrication challenges that the author hopes future researchers can learn from in order to anticipate and avoid unnecessary frustration and make quicker progress. This thesis serves as the next-best alternative to the author personally delivering this information to future researchers in need, and does its part in ameliorating the often-clunky knowledge transfer around practical research execution challenges. The author hopes it is useful for at least one future researcher working on anything even tangentially related to this work.

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20over, whereas%20CSS%20is%20limited%20to%20bottom%20Dup%
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Appendix A

DETAILED EXPERIMENTAL PROCEDURES

A.1 Solar Cell Fabrication

Solar cell fabrication involves depositing bottom contacts across the entire surface and grid top contacts on the top surface. Defining the geometry of the grid top contacts requires photolithography, after which metal is deposited and the photoresist lifted off. Defining several cells on a substrate that are electrically separated from each other requires mesa etching.

Before undergoing mesa isolation and grid contact deposition, a charge separation junction is needed (e.g. p-n junction, ESC heterojunction). In the case of an ESC heterojunction, or if an ARC is used, the mesa isolation and grid contact deposition should occur after depositing the ESC layer followed by the TCO layer. For instance, ITO can be etched using stock HBr or $\text{H}_2\text{O}:\text{HCl}(37\text{wt}\%):\text{HNO}_3(70\text{wt}\%)$ at a 1:1:0.16 ratio by volume [66].

Photolithography Procedure

Below are the steps outlined for the photolithography process before the mesa etch, with minor deviations from the process sheet [82]:

1. Spin-coat photoresist onto the diced InP chip or the InP wafer. AZ nLoF 2020 was used for most of the photolithography in this thesis.
2. Bake the spin-coated sample on a hot plate pre-heated to 110°C for 1 minute.
3. Expose the baked sample to UV light using a mask aligner. The exact exposure time would depend on the desired exposure dose, but for practical purposes, a 1 minute exposure suffices. An MJB 3 Mask Aligner by SUSS Micro Tec (formerly Karl Suss).
4. Bake the exposed sample on a hot plate pre-heated to 110°C for 1 minute.
NOTE: This step is NECESSARY, NOT OPTIONAL!
5. Develop the sample in a metal-ion-free, tetramethylammonium hydroxide-based developers like MF-319 or Resist Developer RD6 by placing the samples in a dish and submerging them in the developer. Start with a development

time of 1 minute. Development can be crisper and more thorough if the user agitates the sample a bit, either by gently moving the dish back and forth on the fumehood tabletop surface or gripping the sample with tweezers and moving it vigorously within the developer.

6. For good measure to remove developer film on the surface, hold the sample with tweezers under running water to ensure the photoresist developer is fully rinsed off.

Mesa Etching

Wet chemical etching was used to perform mesa isolation for the MOCVD and diffusion-doped solar cells because it was the most accessible method given the equipment available for lab-scale solar cells. The wet chemical mesa etch procedure involves photolithography to define the pattern, exposure to acid to react the patterned InP, and then photoresist removal. Different acid mixtures are needed to etch different materials.

Figure A.1 illustrates the mask used to mesa etch square cells that measure 3 mm on each side:

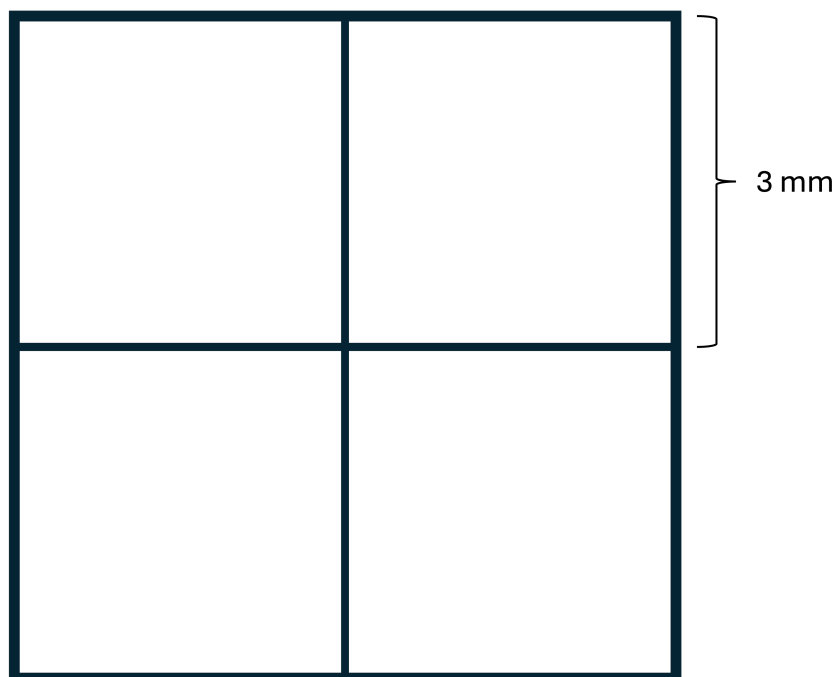


Figure A.1: Schematic of a photolithography mask used to mesa etch square solar cells measuring 3 mm on each side.

The black outline represents the portion of the surface that was exposed during the

lithography step to be etched away by acid.

Grid Contact Deposition

Grid contacts are deposited on the front surface of the cell, the surface that will be facing the sun. The goal is to use enough metal for electricity to conduct well throughout the device while covering as little of the semiconductor surface to maximize the effective area exposed to the sun.

The grid contact deposition starts with the photolithography process outlined in Appendix A.1, but with the mask pattern illustrated in Figure A.2 instead of Figure A.1.

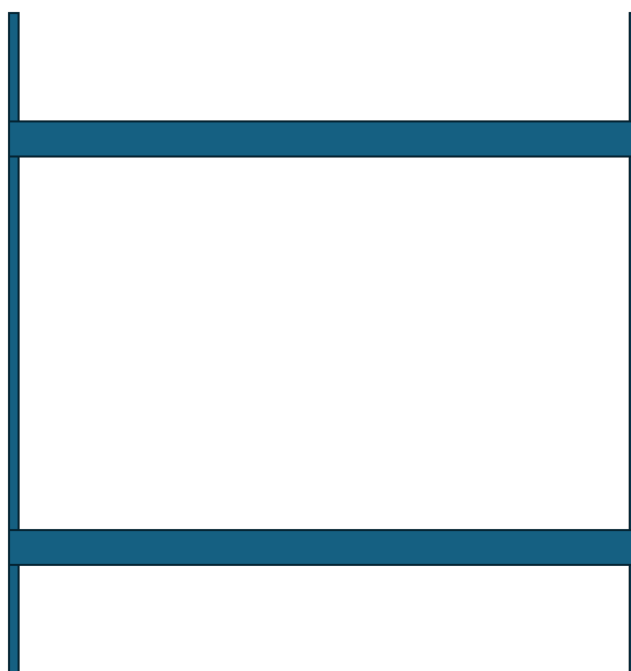


Figure A.2: Schematic of a photolithography mask used to deposit grid contacts on square solar cells measuring 3 mm on each side.

For the MOCVD cells, the ohmic top contact is Ni-Ag, which adheres to InP in a relatively fuss-free manner. Since Ni-Ag adheres well to InP, Remover PG or acetone work well within a relatively brief amount of time. For top contacts that do not adhere as well, such as the Ag/Zn-based contacts to p^+ -InP in the diffusion-doped cells, the cells are often left in DMSO overnight. When an Au adhesion layer was needed, as was the case for the diffusion-doped p^+n cells with Au-Ag-Zn-Ag grid contacts, then the Au and Ag layers before Zn were deposited in the e-beam evaporator before moving the samples to the thermal evaporator to deposit the Zn

and top Ag layer.

Bottom Contact Deposition

Depositing bottom contacts is more straightforward, since the aim is to cover as much of the bottom surface as possible.

The thermal evaporator was used whenever Zn was needed. In practice, Zn and Ag were deposited sequentially in the thermal evaporator for convenience. The e-beam evaporator was also used to deposit Ni-Ag contacts to the undoped InP.

A.2 Defining Macroscopic Patterns: Marker Lithography

For macroscopic patterning of a surface, such as defining the contact dots for a Hall measurement, "marker lithography" can be a convenient alternative to attempting to selectively cover the sample using tape or strips of paper.

The process has overlap with the standard photolithography, but there are some key differences. In this work, negative photoresist (AZ nLoF 2020 in particular) and a black ***water-soluble*** marker (uni POSCA PC-5M in particular) were used. After spin-coating the sample with photoresist and the initial bake, the marker was used to define the desired pattern (such as the four dots or squares for Hall measurement contacts). The sample was then exposed to the U-V light, but afterwards the sample was gently wiped with water (hence the need for water solubility) before the post-exposure bake to prevent the marker pattern from solidifying onto the photoresist and potentially chemically reacting in a way that would make developing difficult.

Credits go to Philip Jahelka for coming up with this idea.

A.3 NW Fabrication

Much of the NW fabrication procedure was detailed in [37]. This work focused on a Cr hard mask for the array of circles that defined the NWs via ICP-RIE etching due to superior etch selectivity and greater fabrication ease.

In practice, the author was struggling to achieve well-defined circles with radii less than 50 nm, and sometimes even larger circles were not well-defined somewhere along the way from e-beam lithography to the final Cr hard mask achieved. The author recommends investigating the post-e-beam-lithography array under an optical microscope after soaking it in the developer solution to confirm that this step went smoothly. If so, then care must be taken when depositing Cr, and perhaps more importantly, removing the e-beam resist after the Cr deposition. Slow Cr deposition

rates and careful treatment when performing lift-off, such as by not oversonicating or shaking the samples too vigorously, may help achieve better results.

The author did not pursue NW fabrication enough to debug the issues with achieving tapered cones. Definitely ask the cleanroom staff and user community for help! As of the writing of this thesis, Wen-Hui (Sophia) Cheng's recipe (and mine, which I just duplicated from her) are available in the ICP-RIE etcher in the KNI.

Reader beware that, at least in the KNI, the whole process will take over 3 hrs because of the gas clearing procedure needed for the gases used to etch InP, despite the etch itself taking 3 minutes. If you were working with Si, it would have been 1 hr total. Just a little note about the effect of material choice on quality-of-life.

A.4 Diffusion Doping

Diffusion doping was briefly discussed in Chapter 4. However, this section will describe the procedure in further detail. To begin, be sure to have your own furnace diffusion tubes and quartz vials, if diffusion tubes do not currently exist for Cd_3P_2 and Zn_3P_2 .

Also, before starting any of the sample preparation and loading steps, the tube furnace should be turned on and pre-heated to the desired temperature.

Vial and Furnace Tube Preparation

Material and Shape

The small dopant source vial, as well as the large vial to hold both the dopant source vial and the substrates, are made of quartz. For the work done here, they were custom commissioned by the campus glass shop, currently run by Nathan Hart. Figure A.3 illustrates the vials in question.

Blocking the Outer Vial with Quartz Wool

The outer vial should be blocked at the nose with tightly-packed quartz wool, as pictured in Figure A.3, to allow for the dopant vapor pressure to build up and actually dope the sample rather than simply escape. However, the inner vial should be left unblocked so that the evaporated dopant source can actually reach the substrates.

The quartz wool should be inserted into the outer vial nozzle AFTER the first RCA clean. However, to save quartz wool, the outer vial cap was generally not RCA

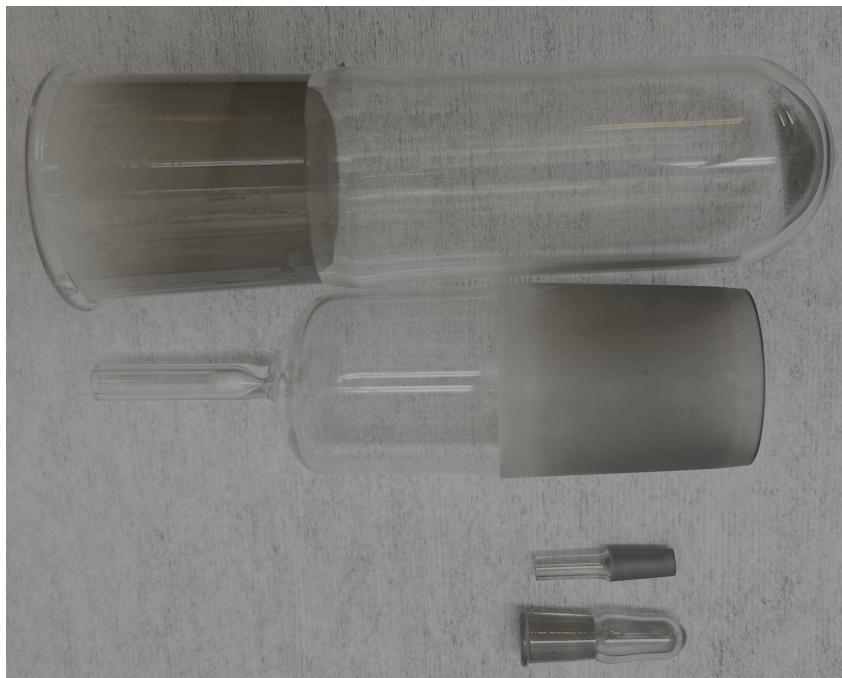


Figure A.3: Inner and outer quartz vials for diffusion doping. The top two larger pieces are for the outer vial to load the inner vial with the dopant source and the substrate chips. The bottom two smaller pieces are for the inner vial to load the dopant source powder (Cd_3P_2 or Zn_3P_2 for this work).

cleaned in between diffusion runs, or at most was wiped with a Texwipe dipped in RCA solution.

Decontaminating the Vials and Tube: RCA Clean and Tube Bake

RCA Clean

After commissioning the vials before first use, and in between uses, an RCA clean should be performed on all the quartz vial pieces using the procedure outlined in [4]. This is especially important for Cd diffusions, where Cd residue has been observed at the bottom of the outer quartz vial. Such residue has not been observed with Zn diffusions, and extensive tests had not been run to confirm whether the RCA clean makes a tangible difference in improving diffusion quality. However, given how many things already go wrong in the process with achieving consistent, high-yield, quality diffusions, the author recommends erring on the safe side. The RCA clean DOES remove the Cd residue while acetone / RCA alone do not. Step 2 of the RCA clean, with the HCl and H_2O_2 , seems to be the step that visibly removes the Cd residue, so chances are that is the relevant step for addressing that residue. However, after initially commissioning the glass vials, before which they

have been handled with bare hands, and if the vials are accidentally touched with bare fingers or if any organic residue ends up on the vials, Step 1 should absolutely be performed to remove that organic residue. Even if only the outside is touched, the high temperatures from the diffusion process will absolutely cause the organic contamination to seep through the quartz vials and ruin the diffusions.

Because the quartz tube was also handled with bare fingers, ideally it too needs to be decontaminated. The author is unsure of the best way to accomplish this, although she has attempted to wipe the tube with a Texwipe soaked in RCA cleaning solutions using one of the long rods used to load the furnaces with samples.

High-Temperature Quartz Bake

After the fact, however, she discovered that baking the tubes at 1000°C seems to do the trick. This was EL2 anneal temperature used for GaAs diffusion-doped solar cell fabrication. Since quartz wool could handle temperatures up to $1050\text{--}1150^{\circ}\text{C}$, one could also simply avoid the RCA clean step and bake the quartz vials instead.

Loading Samples in the Vials

Figure A.4 shows the outer vial and inner vial assembled separately:

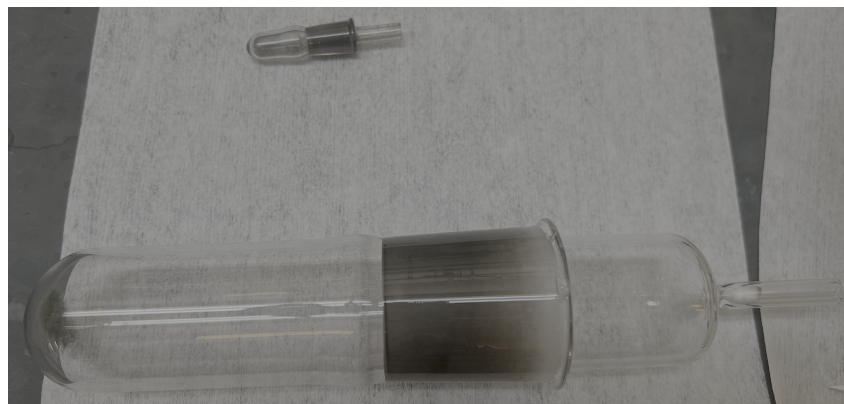


Figure A.4: Inner and outer quartz vials, assembled. The glossy part of the glass should be facing out, while the ground joints should be plugged into each other.

The dopant powder would be loaded into the small vial before plugging it as pictured in Figure A.4. However, the full loading is as pictured in Figure A.5.

It was desirable to maximize the distance between the samples and the dopant source in order to reduce the effect of sample distance on the resulting doping concentration and profile and ensure consistent doping across all chips to the best extent possible. However, the author wanted to dope at least 6 chips in one diffusion run, and that was

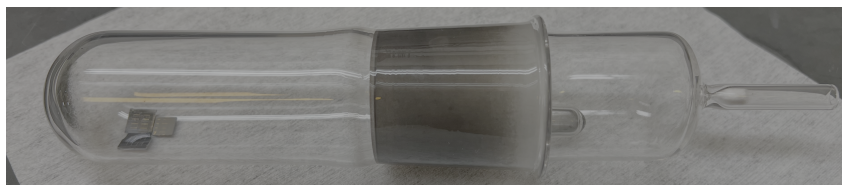


Figure A.5: Loaded samples and dopant source. The dopant vial is loaded such that the quartz bottom faces the outer vial nozzle while the hole for the evaporated dopant to escape is facing the samples. The samples are loaded as close to the bottom of the outer vial as possible.

too many to load in the outer vial cap and handle adequately without jostling. Thus, the chips were loaded as close to the bottom of the outer quartz vial as possible. The dopant vial is loaded such that the quartz bottom faces the outer vial nozzle while the hole for the evaporated dopant to escape is facing the samples. However, to avoid quartz wool oddly getting stuck on the dopant and / or sample, the small dopant vial was kept a little distant from the nozzle with the quartz wool. Currently dopant powder is not loaded in the setup pictured in Figure A.5, but for the diffusion run it should be.

Pump-Purging the Vial with Forming Gas

To prevent sample oxidation during the doping process, the loaded vial must have the atmospheric air pumped out of it and replaced with forming gas. This process is called pump-purging. The apparatus used to perform this process is shown in Figure A.6.

Using this set-up, pump-purging is accomplished by using a vacuum pump to pump out the air from the metal drum with the loaded vial placed inside it and the lid sealed on top of it, followed by allowing forming gas to enter the metal drum. At the time of this thesis writing, Phil had created an Arduino setup to help automate this process. For the size of the vials here, 10 pump-purge cycles were needed to sufficiently evacuate the air from the vials and replace them with forming gas. With the automated setup, this process takes around 20 minutes.

While this process takes place, one should switch the gas flowing through the tube furnace from N_2 to forming gas to ensure that the tube in the furnace has only forming gas flowing through it by the time the samples are ready to load into the furnace. Care must be taken not to open the filter until the N_2 has been switched to forming gas to avoid contaminating the filter. The gas flow rate was also adjusted to 2 sccm. Additionally, as of the writing of this thesis, there is a filter attached to the

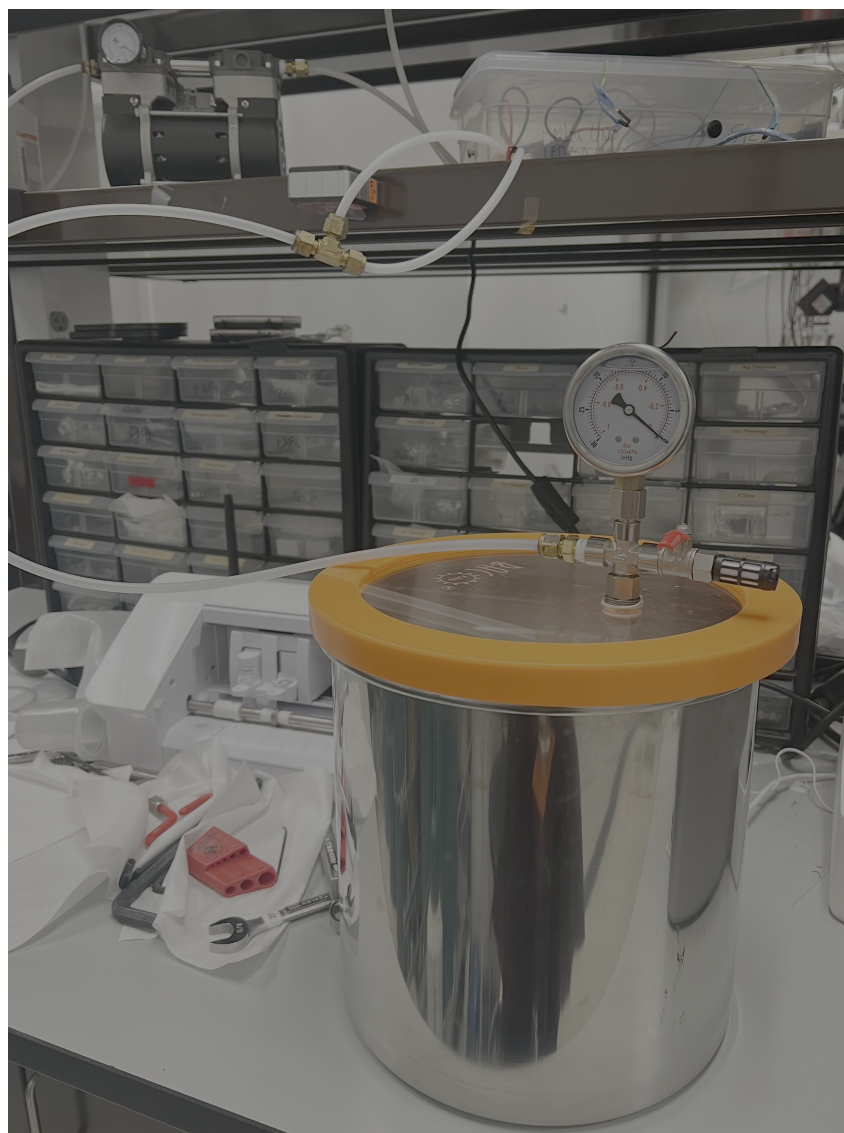


Figure A.6: Pump-purge system. It illustrates the drum in which the loaded vial is placed as well as the vacuum pump in the top left corner with the dial indicating the extent of vacuum. It also shows the Arduino system that helps automate this pump-purge process in the top right corner inside the plastic box, as well as the pipes hooking up the vacuum pump, Arduino system, metal drum, and the forming gas tank (not pictured).

top furnace, and the fittings should be opened and switched such that the forming gas flows through the filter before reaching the tube in the furnace. If the lab setup that was used at the time of this thesis is still in use, hopefully someone in the lab group can demonstrate this.

Diffusion Doping in the Tube Furnace

Afterwards, the loaded vial must be carefully transported and loaded into the tube furnace, which should be pre-heated to the desired temperature and have filtered forming gas running through it. The tube furnaces used are pictured in Figure A.7



Figure A.7: Tube furnaces used for diffusion doping. The gas lines going to the top furnace currently have a filter attached, while the bottom furnace does not.

A quartz rod is used to push the pump-purged vial into the furnace, as close to centered as possible. Then, the cap is put back on and the furnace is left to operate for the desired diffusion time. After that time has elapsed, the furnace should be shut off but the samples untouched until the furnace has cooled down. The gas lines should keep flowing filtered forming gas until the temperature has cooled down to at least 250°C, at which point it can be switched to N₂ and the filter closed.

If a post-diffusion anneal needs to be done, as for Zn doping, then once the furnace is cooled down and the samples can be unloaded, the samples should be taken out of the quartz vial, placed in a quartz open-air boat, and the process in Section A.4 should be repeated, but this time with the samples in the open-air boat with no dopant source rather than the pump-purged quartz vials with a dopant source.

Appendix B

SIMULATION AND EXPERIMENTAL TROUBLESHOOTING

B.1 Lumerical Meshing

One major factor affecting simulation results is meshing size in Lumerical. There is a balance between achieving more accurate results with a smaller mesh size and simulation speed. If the mesh size is too small, the simulation can take a day or even more to run, which is quite impractical. However, if the mesh size is not small enough, then the structure might not be resolved enough to accurately capture the device's properties and performance. For a solar cell, the light intensity attenuates as the light travels down the device, so less and less light is available to be absorbed and converted into captured charge carriers. If the mesh is not refined enough, the decay will not be accurately captured, and this will affect the field, generation rate, and J_{SC} calculations.

The default mesh settings are generally fine starting points. For my nanostructured simulations, such as the NWs, the simulations with default mesh settings would generally finish running under 10 minutes. The mesh refinement can be adjusted either universally in Lumerical's settings or in selected portions of the simulation via user-defined mesh override regions [15] [14] [13].

It is possible to define mesh override regions anywhere within the FDTD region, including over the monitors, within the vacuum outside of the materials, and over the plane wave source. It could be useful to define mesh override regions for the monitors if calculating reflection, transmission, or absorption, or to refine the mesh for the plane wave source to obtain more refined spatial resolution for the light source. In practice, refining the mesh for the top portion of the NW is helpful for reflection and absorption calculations, as well as for the entire solar generation region, which in these simulations covered the entire InP region but nothing else. It can also be helpful to define a refined mesh for the top portion of the InP structure — whether the NW or the planar films both with and without the textured pyramids — because the generation rate changes so rapidly in the top portion. This is more true for the NWs and textured films, since the nanostructuring introduces nonlinearities that may be worth refining in the simulations. The electric field and generation rate figures in Chapter 2 illustrate the extent to which the chosen mesh settings

resolve the circular x-y cross sections and the x-z trapezoidal cross-sections for the NWs, for instance. They also show how well the generation rates for the x-y textured pyramidal cross sections are resolved. It can be helpful to play around with the mesh sizing to investigate the tradeoffs between the desired results — such as electric fields, generation rates, and calculated J_{SC} — and the simulation times.

For all the simulations run, the FDTD's global mesh settings were set to an "auto non-uniform" mesh type with "conformal variant 0" chosen as the mesh refinement type. The top region of the FDTD, which encompassed the reflection monitor, had a mesh override region with the z mesh overridden and set to a maximum of $0.01\ \mu\text{m}$ or $0.022\ \mu\text{m}$. The entire solar generation region has a maximum z mesh step of $0.0025\ \mu\text{m}$ for the entire InP structure in both the NW and thin-film cells. Best practice would probably be to set the maximum mesh step size as some fraction of the top NW radius.

Pro tip: It is possible to define parameter values for different objects in the simulation by scripting them in the Setup of the model object. This allows easy parameter changes and defining parameter values as functions of other parameter values. For instance, doing this would allow the user to set the maximum mesh size as a function of the NW radius.

B.2 Using the AM0 Spectrum

To use the AM0 spectrum, start with a "solar generation rate" analysis group (can be found from one of Lumerical's example solar cell simulations such as in the following Lumerical examples in [10], [12], [9], [8], [11], [7], or as an analysis group option that can be inserted from within the "optoelectronics" category. Then, download the AM0 spectrum and save it as a .mat file and put it in the same directory as the Lumerical FDTD simulation file. Then, in the Analysis script for the solar generation rate object, include the line "matlabload('AM0.mat');". The variables representing the wavelength and spectrum will be whatever those column titles are in the .mat file.

B.3 Wafer Handling

Dealing with MOCVD Wafers

The MOCVD wafers were double-side polished, so the back side was marked by lightly scratching it with a diamond scribe.

If one loses track, during the dicing process, of which side is the front versus the

back, it is helpful to remember that HCl etches InP but not InAlAs (at a meaningful rate), one can chip off a portion and drop some HCl acid onto the suspected back side. Since the InAlAs layer is close to the front side, only $\sim 2 \mu\text{m}$ below the surface, the front side would stop reacting with the HCl much faster than the back side.

B.4 Diffusion Doping

Vial Sizes

The initial tube and cuvette used were so small, and it was difficult to keep the Cd_3P_2 powder away from the InP chips during handling. Thus, initial diffusions were inconsistent from diffusion run to run. Moreover, the sample surfaces would exhibit permanent discoloration if the Cd_3P_2 powder came in contact with the InP chips during diffusion runs.

To address this issue, custom quartz vials were commissioned from Nathan at the campus glass shop. The outer vial was much larger, and came with a cap that had a small hole to make it easier to seal with quartz wool and keep the wool in place. The small inner vial that contained the dopant powder also came with a cap with a small hole, which made it easier to keep the powder contained within and separate from the substrate while still allowing the heated dopant vapor to escape the small vial and occupy the larger vial during the doping process. Using a larger vial also allowed for two chips to be placed next to each other at a given distance rather than only one and meant that there was a smaller fractional difference in the distance between the chips and dopant source, resulting in more consistent diffusions when multiple chips were placed in the vial in a single diffusion run.

Pump-Purge

The number of pump-purge cycles needed will depend on the size of the vial. When the quartz test tubes were used, three pump-purge cycles sufficed. When the larger vials were used, ten pump-purge cycles were needed to sufficiently pump the air out of the vials and replace it with forming gas. Phil built an Arduino system that helped automate this process. However, care is still necessary when handling the samples post pump-purge to minimize exposure to air after the pump-purge cycles and before loading them into the furnace.

Since the pump-purge setup and the furnace are in different rooms, and require opening and closing heavy doors to get from one setup to the other, this can be a challenge. Assistance is recommended, although it was possible to achieve dif-

fusions that were not visibly oxidized even without it. Keeping the vials in the pump-purge drum and carrying the drum can help minimize exposure to air, but at the cost of carrying and handling a big, heavy drum that, depending on your arm length, can be cumbersome and result in the vial rolling around and jostling the samples. Taking the vial out of the drum and blocking the outer hole plugged with quartz wool using a finger to further block air can help keep the vial more stable and prevent rolling, but there may be more air exposure, especially if one is trying to open doors without assistance.

If a different-sized vial is used, adjustment to the number of pump-purge cycles may be needed.

Furnace Loading and Operation for Diffusion Doping

The author has generally found it easier if the tube is loaded as pictured in the top furnace in Figure A.7, with the nozzle end of the tube itself being attached to the circular metal fitting, rather than the cap as pictured in the bottom furnace. However, earlier tubes had thinner quartz walls on the nozzles, which made them prone to breaking and cracking until the nozzle got too close to the overall tube and could no longer be properly sealed when the metal circular fitting was attempted to be screwed on. Later commissioned tubes had thicker walls, which ameliorated this challenge. However, sometimes it was preferred to screw the cap to the metal fitting instead of the main tube. This author found, though, that the cap was harder to push on and pull off when the tube was set up as pictured in the bottom furnace of Figure A.7.

Acid Etching: Back Side

After diffusion doping, all of the surfaces are doped, so the back needs to be etched to remove the doped layer and have a p-n junction rather than a p-n-p junction. However, the acid risks damaging the front side of the sample unless the front is protected, particularly if HCl is used to etch the back given how volatile it is. To avoid or limit this effect, deposit a layer of photoresist on the front of the whole sample and bake it to harden the photoresist without any photolithography. Then, etch the back. The photoresist will help protect the surface against acid damage that can result from exposing the sample to even HCl fumes, even if the acid does not leak onto the front side. The fumes from undiluted HCl have eaten even through the baked photoresist on the front, however, when attempting to etch the backside. Thus, if using HCl, it should be diluted at least somewhat to prevent surface damage.

The downside of using iodic acid instead of HCl is that iodic acid comes as a powder that needs to be dissolved using a stirbar, and it has a much lower etch rate than HCl — a 20% by weight iodic acid etch has an etch rate of around 80 nm / min and increasing the concentration does not much increase the etch rate but results in surface roughness. Since the diffusion depth seems to be around 2 μm at least, the required etch time to fully remove the doped layer on the back side is on the order of 30 minutes, during which time iodic acid particles precipitate onto the surface and are difficult to remove even with sonication in acetone or IPA. Meanwhile, a 1:1 $\text{H}_2\text{O}:\text{HCl}$ acid mixture has an etch rate of 100 nm / min, there is no particle precipitation like with iodic acid, and its ratio can be adjusted easily to increase the etch rate. However, this comes at the cost of an increasingly aggressive etch that can damage the front of the sample.

Redeeming Oxidized Samples

Cd-doped samples were especially prone to visible signs of oxidation via brownish or rainbow-colored discoloration if the system was not pump-purged sufficiently or if it is exposed to anything but filtered forming gas at elevated temperatures over 250°C for too long. Etching the samples with a 100:1 $\text{H}_2\text{O}:\text{HCl}$ solution would remove the visible discoloration, and working solar cells were able to be fabricated from such treated samples.

B.5 Etching

There were a surprising number of challenges with etching, especially when transitioning from the MOCVD-grown cells with shallower p-n junctions to diffusion-doped cells with deeper p-n junctions. Diffusion-doped cells also require investigation of emitter thinning to create shallower p-n junctions, which makes etching challenges even more pressing to address for those samples.

Impact of Etch Depth on Etchant Choice

When mesa etching InP solar cells, the most important thing to consider is the depth of the p-n junction. The mesa etch must reach past the p-n junction to properly electrically isolate adjacent solar cells. For the MOCVD cells, the p-n junction is 80 nm below the surface, which made an $\text{HCl}:\text{H}_2\text{O}$ etchant easy and functional [89]. Even so, it is important to strike a balance between etchant aggressiveness and etch time. It may take some trial and error to determine what etchant compositions etch the sample in a reasonable amount of time while not etching away the photoresist

layer. If the etchant is too aggressive or it is left on the sample too long, it can etch the photoresist and then ruin the sample.

HCl-Based Etchant

For the MOCVD samples, a 1:1 HCl:H₂O etchant, which etched InP at ~100 nm / min, was sufficiently effective. A 3-minute etch for good measure was sufficient to etch through the p-n junction for these samples without wearing out the photoresist. For the diffusion-doped cells, however, with p-n junctions on the order of ~1 μ m, however, HCl-based etchants were too aggressive. Etchants with higher HCl concentration had lower etch times but were difficult to control and eroded the photoresist, but the 1:1 etchant took too long to etch through the p-n junction, which also eroded the photoresist.

Iodic Acid for Longer Etches

Diffusion-doped InP cells were etched with iodic acid. This had a lower etch rate — 65 nm / min for a 10% weight iodic acid etchant, and 80 nm / min for a 20% weight iodic acid etchant — but it causes less damage to the photoresist than HCl-based etches [135]. Iodic acid does not dissolve very readily in water. Thus, for best results, mix the etchant by weighing out the appropriate ratio of iodic acid powder and water and using a magnetic stirrer to fully stir and dissolve the iodic acid powder. For the diffusion-doped cells, etch times of 30 minutes with 10%-weight iodic acid tended to be needed to etch the cells. This was true for even those cells that were fabricated with the native InP oxide left on the surface during diffusion as a stopping layer, which helped yield shallower p-n junctions than those formed in diffusion runs with the native oxide removed.

B.6 Ohmic Contacts

Ohmic contacts are essential in achieving a proper I-V curve and achieving excellent figures of merit such as J_{SC} , V_{OC} , and FF. However, the intrinsic properties of InP, particularly p-InP, as well as material and lab limitations, can lead to unexpected challenges even in such a "basic" step. The following subsections detail some of these challenges.

Challenges with Finding Tools to Deposit Zinc

Note: since Zn has a much higher vapor pressure than many other metals during deposition, tool managers might be strict about allowing Zn deposition. Prof. Atwater's lab has a thermal evaporator dedicated to high vapor pressure materials

such as Zn and organics. This can create challenges in finding a tool to deposit Zn. Because the thermal evaporator was used to deposit Zn, and it could only handle 2 materials at once, additional challenges arose when Au was introduced into the ohmic contact to the p-InP diffusion doped layer because the Au and bottom layer of Ag were deposited in the e-beam evaporator and then the samples had to be unloaded and reloaded into the thermal evaporator to deposit the Zn and the second Ag layer on top.

Necessity of Anneals: Minimizing High-Temperature Exposure

Because of how thin the top n-type window and emitter layers are in the MOCVD layers, top contacts deposited on the emitter side of the device risk penetrating the device too deep during such a long anneal time at this temperature, which is why it was important to investigate whether anneals were necessary to achieve ohmic contacts, particularly for the Ni-Ag metal stack chosen for the top contacts in these cells. For the diffusion-doped cells investigated, the diffusion of the Ag-Zn contacts was not a major concern because of the apparent thickness of the p-doped emitter. However, it would be a major concern if the emitter is made thinner, either via a more optimized diffusion process or emitter thinning. Unfortunately, Ag-Zn contacts are not ohmic to p-InP without this anneal. The literature suggests that temperatures of at least 350°C are needed to achieve ohmic contact to p-InP [68]. Additionally, because the literature did not always provide % weight for the various metals used, particularly Zn and Ni, the work stuck to equal thicknesses of each layer (50 nm each). For instance, the Ag-Zn-Ag stack was 50 nm Ag, 50 nm Zn, and then another 50 nm Ag. However, this translates to around 25% weight Zn instead of 5% often used in some papers [129]. Previous work also shows that, all else equal, reducing the % weight of Zn from 20% to 1% reduced the anneal time from 17 minutes to 1 minute at a temperature of 440° while also reducing specific contact resistivity [30]. While it is not certain that this trend would persist at lower temperatures, it is an argument in favor of reducing the thickness of Zn layers in devices for future work. Since this paper was an obscure conference paper that was only located after the start of thesis writing, this insight was not able to be incorporated into the TLM measurements and devices made in this work. However, future work can further investigate the ideal Ag-Zn proportions in p-type ohmic contacts and their effects on anneal temperature and time.

Anneal Environment: Glovebox versus Furnace

To avoid oxidation, anneals needed to be performed in an inert atmosphere. Many of the anneals in this work were performed in a glovebox filled with N_2 . However, the hot plate was moved to a different glovebox between the work performed on MOCVD wafers and that performed on diffusion-doped wafers. This seemed to have altered the effectiveness of the anneals, perhaps in part because aluminum foil was expected to be used to cover the hot plate. Additionally, maneuvering centimeter-sized chips with tweezers in a glovebox was difficult, and it was difficult to remove the samples quickly enough without damaging the gloves. Furnace anneals were also attempted, with forming gas (95% N_2 , 5% H_2), but optimizing the anneal time was challenging because the sample would take more time to reach the desired temperature in a large furnace resting on a glass slider, relying on the surrounding hot gas to heat the sample up, compared to being placed on a pre-heated hot plate. Attempting to anneal the samples without overshooting the anneal time and ruining the solar cells was a challenge that remained unresolved after initial attempts incrementing the anneal times in 5-15 min increments from anneal times of 15 minutes onwards. Thus, the work reverted back to the hot plate glovebox anneals, despite their imperfection. However, obtaining a rapid thermal annealer for future work would likely help achieve better anneals, especially if anneal temperatures higher than $400^\circ C$ are needed for sufficiently-low specific contact resistivities. Other work has annealed Au-Zn contacts for 40 minutes at $400^\circ C$ in forming gas in a tube furnace [44].

B.7 Metal Adhesion Issues: Ag on InP

For the diffusion-doped cells, the ohmic top contact was initially Ag-Zn-Ag. Ag-Zn-Ag adhered adequately enough to the back surface, which is covered in its entirety. However, the grid front contacts are much thinner, and effective liftoff often required sonication, which often removed the top contacts with it. To mitigate this issue, a thin Au layer of 1-10 nm was deposited before depositing the Ag-Zn-Ag stack. Lift-off was performed by leaving the cells in DMSO overnight. However, because the diffusion-doped cell is a p-on-n cell, exposing the solar cells immersed in DMSO overnight to laboratory light creates a photoelectrochemical effect where the holes generated in the n-InP migrate to the surface and etch away the surface and top contacts with it, and the need to leave the samples overnight provides plenty of time for this reaction to occur. Therefore, it is important to cover the samples to prevent light exposure during this liftoff process, at least not overnight exposure.

B.8 Measurements

This section details the challenges faced in measuring devices.

Hall Measurements

Hall measurements involve measuring the voltage that results when a magnetic field is applied to a sample with current flowing through it, and the moving charges are pushed to one side and build up [93]. The sign of the voltage dictates the carrier type — n or p — while the magnitude indicates the mobility. There were a few challenges that arose during Hall measurements.

Undesired Carrier Type Reading

It is important to pay attention to the carrier type reading, since sometimes the carrier type is the opposite of what is expected. For instance, some Hall measurements of the diffusion-doped samples registered 0 p-type counts and, say, 10 n-type counts, even though the sample surface is expected to be p-type. Other times, the sample registers both p and n-type counts.

Confirm that the magnet is oriented as directed by the tool and the arrow stickers on the magnet and setup, and take full Hall measurements rather than FastHall measurements for good measure. If the measurements still indicate the wrong doping type, this suggests that the doping did not occur as expected, or at least that the doping is not consistent across the whole surface.

Contact Check

The LakeShore Cryotronics HMS-TT M91 FastHall measurement system used in this work can perform a contact check before the rest of the measurements. If the contact check is linked to the rest of the measurements, it "permits the M91 to automatically determine the best excitation and ranging parameters for the measurement conditions, and then use these inputs for subsequent resistivity and FastHall™ commands" [70]. Many times, the contact check will not pass. However, if the R^2 value is sufficiently high ($R^2 > 0.99$), measurements are still worth taking. However, if the contacts are not of good quality, or if the sample resistivity is high and contact is not ohmic, then the R^2 values can be quite low ($R^2 < 0.85$), and then the measurements are likely not reliable.

Alternatives to Zn Deposition for Hall Measurement Corner Contacts

When the thermal evaporator was not working or Zn depositions were not working well, then the author attempted to melt In dots onto the corners of the samples as a simpler way to achieve contact for Hall measurements because a labmate had success with this method for their samples. However, with InP, it seems using In dots messes with the ability of the Hall apparatus to accurately read the surface charge type and concentration. Therefore, do not try this at home, kids.

B.9 Depositions

Thermal Evaporator Depositions

Issues were encountered when the boats got contaminated with other materials deposited in the thermal evaporator. Best practice would be to get your own thermal evaporation boats for your depositions and unload them when you are not using the evaporator to avoid contamination from other users' runs.

E-Beam Evaporation

Different metals will have different ideal deposition conditions — including deposition rates, beam sweep pattern, etc. — to achieve smooth evaporation runs with minimal metal splattering while achieving quick enough depositions to be time-efficient. Ni in particular was recommended to be deposited at $0.2 \text{ \AA/s}$, although rates up to $0.5 \text{ \AA/s}$ were achieved without notable splattering. Check deposition logs or ask other users for more details.

Appendix C

OTHER NOTES

C.1 Identifying Appropriate Deposition Tools

NOTE: These deposition tools operate in vacuum, and Zn has a high vapor pressure, so users should check before doing any depositions once Zn has been deposited. Some tools, such as the e-beam evaporator, have been okay with the relatively small amount of Zn used on the samples, especially if there is a layer of metal like Ag on top of it. However, others, like the Atwater ALD, are not okay with any Zn-coated materials being in the tool. While n-on-p cells may face fewer challenges with this restriction by depositing the Zn later, since Zn is part of the back contact, this is a greater challenge with p-on-n cells because the contacts need to either directly touch the surface or touch a conductive layer, like ITO. This can limit the ARC possibilities. TiO_2 , which is used as an ESC for InP solar cells like those presented in [166], would make a bad top contact for a p-on-n InP cell precisely because it selects electrons and rejects holes, which is the opposite of what is desired in a solar cell.

ITO

As of the writing of this thesis, there was a sputterer in the Atwater lab that was dedicated to ITO. Continuous film thicknesses can start at 5 nm. ITO can also be deposited in the KNI sputterer as of the writing of this thesis, but films may not be sufficiently pure because the KNI sputterer is used for a variety of materials besides ITO.

TiO_2

TiO_2 can be deposited in the e-beam evaporator. However, because of the crystalline form the source comes in, the deposition is not as controlled as metal deposition. Ellipsometry seemed to indicate major discrepancies in the desired versus actual film thicknesses, on the order of 10 nm for films that are 50-60 nm thick. However, since many people adjust the tooling factor using ellipsometry measurements, care needs to be taken regardless, and it is important to use AFM on a separate sample if possible to get measurements of the actual thicknesses. This is especially important for an ARC, whose effectiveness is very sensitive to the film thickness. Ti_3O_5 was used as a

source to deposit titanium oxide instead of TiO_2 , and limited measurements showed that AFM revealed a difference of ~ 2 nm between the intended and measured thicknesses, but ellipsometry for Ti_3O_5 revealed a 20 nm difference in potential thicknesses. The fitted film thickness ranged from 57-77 nm for a film that was intended to be 60 nm depending on the choice of angles measured.

TiO_2 can also be deposited by ALD, but that is a much slower method, and in practice depositing films thicker than 10 nm is undesirable. ALD, at least in the lab, should be for films thinner than 10 nm, which makes them unsuitable for depositing TiO_2 as a predominant component of an ARC. At best, it is suitable as an ESC, if ever trying to fabricate a junction-less InP cell such as demonstrated in [165].

TiO_2 can also be sputtered in the KNI, but contamination would be an issue, just like with ITO. Additionally, with the KNI in general, it can be difficult to get time on the tool, and it is important to use the tool often enough to remember how to use it so that retraining is unneeded. TiO_2 was never sputtered on the samples fabricated for this thesis. Just as with the other methods, thicknesses would need to be calibrated by measurement with AFM or ellipsometry.

SiO_2

SiO_2 can also be deposited in the e-beam evaporator. Similar issues around thickness calibration existed. Ellipsometry seemed to indicate major discrepancies in the desired versus actual film thicknesses, on the order of 20 nm for films that are ~ 100 nm thick. However, limited AFM measurements suggested that, at least for the samples measured, there was a difference of ~ 4 nm between the intended and measured thicknesses. Again, since many people adjust the tooling factor using ellipsometry measurements, care needs to be taken regardless. It is important to use AFM on a separate sample if possible to get measurements of the actual thicknesses. This is especially important for an ARC, whose effectiveness is very sensitive to the film thickness.

SiO_2 can be sputtered in the KNI dielectric sputterer using either a SiO_2 target or a Si target with reactive sputtering using O_2 gas. The former is more straightforward, but it results in a lower deposition rate and greater optical absorption, which is non-ideal for an ARC [52]. The latter requires sufficient O_2 flow to ensure the formation of stoichiometric SiO_2 . If a well-defined, well-calibrated recipe is not being used, that must be done by depositing and measuring the layer thickness. It can also be deposited in the PECVD tool in the KNI, although the KNI PECVD was not used

to fabricate the samples in the thesis.

Zn

Because Zn has a higher vapor pressure than other materials, it risks contaminating other depositions, and is thus not allowed in many deposition tools in the labs, such as the e-beam evaporators in both the Atwater lab and the KNI. As of this thesis, the thermal evaporator in the Atwater lab, affectionately known as the "dirty thermal" because of the permission to deposit high vapor pressure materials such as Zn and organics, was the only tool where Zn could be deposited. This caused delays when the thermal evaporator was not working or when there were delays in ordering new, uncontaminated boats due to the lack of alternatives.

Ag

Ag is pretty straightforward to deposit in the Atwater e-beam evaporator. However, near the end of the work underlying this thesis, the evaporator often malfunctioned, which caused delays. Ag can also be evaporated or sputtered in the KNI, but again, that requires KNI access, which entails a membership, as well as cleanroom trainings and either an incredibly sharp memory and competence with the KNI tools specifically or sufficient usage to keep memory fresh.