Development of Biocompatible Parylene Neurocages for Action Potential Stimulation and Recording

Thesis by

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Acknowledgements

I would like to dedicate this thesis to my parents and my sister, Michelle. For their unwavering support and assistance in so many ways over the years, I am extremely grateful.

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Abstract

Neurons, and the neural networks they form, are at the heart of our biological and cognitive functions. Traditional *in vitro* techniques for studying neural networks use two-dimensional multi-electrode arrays. While furthering the study of neural networks, the inherent mobility of the neurons and the lack of specificity between neurons and electrodes can limit the use of these arrays. Initial work, the neuro-well, eliminated these problems by physically trapping individual neurons in wells. While neural networks were formed and action potentials recorded with arrays of neuro-wells, the bulk micromachining techniques required a complex fabrication process, with limited scalability and a low yield, thus inhibiting their further development.

Parylene neurocages counteract these difficulties by using surface micromachined structures to trap neurons in close proximity to electrodes, without inhibiting their growth. The use of surface micromachining techniques minimizes the fabrication and scaling complexities, improving the device yield. The neurocages can be fabricated on either glass or silicon substrates, with a variety of electrical insulation materials, including Parylene and silicon-nitride. Parylene is a biocompatible polymer that is non-toxic, extremely inert, and resistant to moisture and most chemicals. Its conformal deposition makes it easy to fabricate 3D structures like the neurocage. Parylene is transparent, allowing the neurons to be easily seen.

Individual neurons are placed into the neurocages, either manually with a pressure-driven micropipette or automatically with a laser tweezers system. The neurocages have openings to allow the neurites to extend out of the neurocages and form synaptic connections with their neighboring neurons. Each neurocage has its own electrode, which is platinized to increase its capacitance. Successful growth of neural networks has been achieved using arrays of neurocages with Parylene and silicon-nitride insulation on both silicon and glass substrates. These neurocages have a long-term cell survival rate of ~ 50% after 3 weeks and have proven 99% effective in trapping neurons. The neurons inside the neurocages have been successfully stimulated, with both current and voltage pulses. Action potentials, both spontaneous and resulting from a current stimulus, have been recorded from neurons comprising the neural networks.

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CHAPTER 1
Neurons and Neural Networks

Neurons are at the heart of our biological and cognitive functions. The human brain consists of networks of more than 100 billion interconnected nerve cells. These neural networks control our perceptions, actions, emotions, and our ability to learn. Thus, neurons, and the neural networks they form, have been the subjects of intense study over the last several decades. Unfortunately, due to the location of these neural networks and their immense complexity, it is very difficult to study these networks *in vivo*. Therefore, the most common techniques for studying neural networks are *in vitro* techniques.

1.1 Neurons

A typical neuron can be divided into four separate regions: cell body, dendrites, axon, and presynaptic terminals. The cell body is the metabolic center for the neuron, processing proteins and nutrients. Dendrites and the axon are the processes of the neuron. The dendrites branch out from the cell body and receive incoming signals from other neurons. The axon extends out from the cell body and transmits electrical signals to other neurons. These electrical signals are called action potentials and are rapid, transient, all-or-none impulses. They have typical amplitudes of 100 mV with durations

of about 1 ms. Action potentials are the method by which the brain receives, analyzes, and conveys information. As all neurons conduct action potentials in the same manner, the information conveyed by the action potential is determined by the pathway to the brain and not the signal itself. Finally, the presynaptic terminals are at the ends of the axon and transmit the action potentials to the dendrites of the next neurons in the network.

There are two basic principles of neural organization, put forth by Ramón y Cajal [1]. The first is called the principle of dynamic polarization. This principle states that the electrical signals in the neurons flow in only one direction, from the dendrites to the cell body to the axon and finally to the presynaptic terminals. The second is the principle of connectional specificity. According to this principle, neurons do not indiscriminately form random neural networks; rather each neuron makes specific connections with only certain other neurons.

Ultimately, we want to study the dynamics of a functioning neural network by measuring the electrical activity of all of the individual neurons within the network. Our goal is to create a non-invasive technique that allows specific stimulation of selected neurons and records the responses of all the other neurons. Then we can map the connections within the neural network and study the plasticity, the changes over time in the connections between the neurons. There are two standard electrophysiological techniques for studying neurons within a neural network: whole-cell patch-clamp and multi-electrode arrays (MEAs).

1.2 Patch-Clamp Recording Technique

The patch-clamp technique developed in 1976 by Erwin Neher and Bert Sakmann involves puncturing the cell membrane with a glass micropipette filled with saline [1]. A metal electrode in contact with the saline in the micropipette allows the membrane current to be recorded. The properties of small to medium sized neural networks can be explored with this technique [2–3].

There are, however, several serious drawbacks to this technique. First, by puncturing the cell membrane, the neuron's responses can be unintentionally altered. The puncturing also leads to imminent neuron death, usually in a matter of hours. This limits the ability of the patch-clamp to obtain repeated recordings over long periods of time. In addition, the death of individual neurons in the neural network will alter the connections and function of the network. Finally, we would like to be able to record from all of the neurons within the neural network. However, the patch-clamp requires the use of large external micromanipulators to hold and manipulate the micropipettes, and given the relatively small area in which the neural network grows, it is virtually impossible to record from more than a few neurons at one time.

1.3 Multi-Electrode Arrays (MEAs)

Multi-electrode arrays (MEAs) are two-dimensional arrays of electrodes on glass or silicon substrates [4–9]. Neurons are cultured on top of the electrode array and neural networks are allowed to form. MEAs are non-invasive and non-lethal, unlike the patch-clamp technique, and are well-suited for long-term experiments. MEAs are ideal for

studying the spontaneous activity of the neural network, as well as recording action potentials when an external source supplies the stimulation pulse. MEAs are the standard method for neural network recording; however, they have two serious weaknesses when studying neural network function. First, the cell bodies and processes (axons and dendrites) are typically quite mobile during the first few weeks of culturing [10–12]. Thus, it is difficult to associate the recorded signals with specific neurons. Second, since the neurons are not confined to the electrodes, recording and stimulation can occur at unknown sites on an unknown, often changing, number of neurons.

As an alternative to the traditional MEA, a patterned MEA was developed [11–14]. The patterned MEA is also a two-dimensional array of electrodes; however, the surface has been patterned. Certain regions surrounding the electrodes are stamped with a neurophilic substance, such as poly-D-lysine which promotes attachment of the neurons to the substrate, while other regions are stamped with a non-adhesive substance, such as polyethylene glycol (PEG) to which neurons will not adhere. Therefore, the neuron growth, and the subsequent neural network formation, is confined to those areas which have been stamped with the neurophilic substance. Thus, even though the neurons are mobile, the area in which they can move has been limited. Unfortunately, despite the restricted neuron growth area, the patterned MEA has the same drawbacks as the traditional MEA. To counteract these difficulties, the neuro-well was developed.

1.4 Neuro-Well

The neuro-well is essentially a two-dimensional electrode array, except around each electrode a small "well" is placed into which a single neuron can be placed [10, 15–17]. Fig. 1-1 shows the basic neuro-well structure. The neuro-well is a bulk-micromachined silicon device. The wells are etched into the silicon and then covered with a silicon-nitride canopy. Individual neurons are placed into the wells, while the silicon-nitride canopy traps the neurons in close proximity to the electrodes. The canopy also contains openings to allow neurite outgrowth. Arrays of neuro-wells permitted the neurites from different neurons to form connections, thereby allowing the neurons to develop neural networks. With these neuro-wells, individual neurons in neural networks could be reliably stimulated and action potentials recorded for long-term studies.

One advantage of the neuro-wells is the one-to-one correspondence between neurons and electrodes. Hence, electrical recordings can be unambiguously associated with a single neuron. Also, by physically trapping the neurons, it is guaranteed that the neuron will always be in close proximity to the same electrode, ensuring it can always be

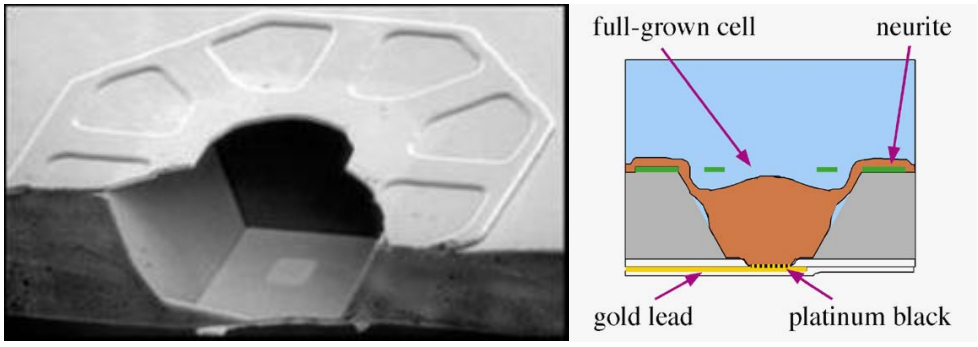


Fig. 1-1. The left image shows a scanning electron micrograph of a cross-section of the neuro-well. The electrode is at the bottom of the well and the silicon-nitride canopy covers it. The right image shows an illustration of a neuron inside the neuro-well, with the neurites extending out through the openings in the silicon-nitride canopy on top.

accessed. The recording and stimulation, like for the MEAs, is non-invasive and non-lethal, allowing individual neurons to be studied for long-term experiments.

Unfortunately, the neuro-wells had several significant drawbacks which limited their continued development. As the neuro-well was a bulk-micromachined device, the fabrication process was incredibly complex and the resulting devices had a very low yield. The complex fabrication process also made it difficult to create large arrays of neuro-wells to study large neural networks. Another serious flaw was that as the neurites grew out through the openings in the canopy on top of the wells, the neuron was pulled away from the bottom of the well, and hence from the electrode. In some cases, the neuron was pulled completely out of the neuro-well. Finally, the neuro-well was opaque, thus limiting the visibility of the cell bodies, making it difficult to ascertain details concerning the health of the neurons until after the neurites had grown out of the wells.

1.5 Neurocage

To counteract the difficulties encountered with the neuro-well, we developed the neurocage (Fig. 1-2), the focus of this thesis. Like the neuro-well, the neurocage traps individual neurons in close proximity to the electrodes, while at the same time allowing neurite outgrowth and neural network formation. The neurocage, unlike the neuro-well, is a surface micromachined device. Thus, the fabrication process is much less complex, resulting in a higher device yield. The use of surface micromachining techniques also makes it easy to fabricate large arrays of neurocages. Unlike the neuro-well, the neurites in the neurocage grow out through openings at the bottom of the cage. Hence, as the

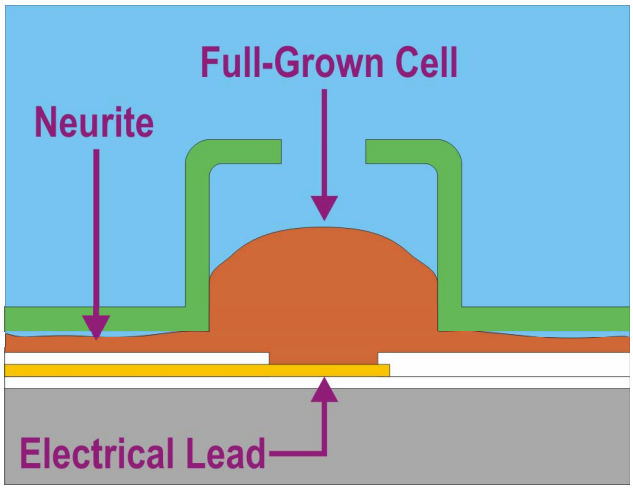


Fig. 1-2. Illustration of a neuron inside the neurocage. The neurites grow out through openings in the bottom of the neurocage, pulling the neuron closer to the electrode. Thus, the neuron remains trapped in close proximity to the electrode.

neurites grow the cell body is actually pulled closer to the electrode, rather than further away. Finally, the use of Parylene, a biocompatible polymer described further in Section 2.2, ensures the neurocage is transparent. Thus, the neuron inside the neurocage can be easily visualized.

Initial neurocage designs achieved some neurite outgrowth, however, the long-term survival rate was very low (< 25%) [18–19]. The continued development of these neurocages presented here, achieves neurite outgrowth and neural network formation, with a long-term survival rate > 50%. In addition, successful action-potential stimulation and recording has been achieved from neural networks formed by neurons in these neurocages.

CHAPTER 2
MEMS Fabrication Technologies

A Micro-Electro-Mechanical System (MEMS) is a fabricated system that contains both electrical and mechanical components. The characteristic dimensions range from a 100 nm to millimeters. MEMS are also called micromachines or microsystems technology (MST). Inspired by the technologies used to create microelectronic devices, MEMS devices serve as bridges connecting the digital world of integrated circuits (IC) with the analog physical world.

MEMS technology is still largely based on techniques borrowed from the semiconductor industry. However, the materials and techniques used in MEMS fabrication are continually evolving to suit the current needs. Although still using the silicon-based devices common to semiconductor fabrication, alternative substrates, such as glass/quartz, ceramics, and polymers, are gaining popularity. This change is motivated by the desire to produce devices that are biocompatible, cheaper, and easier to fabricate.

In general, MEMS technology produces devices that are smaller, better, and cheaper. MEMS devices have significantly smaller footprints than their conventional counterparts. By exploiting phenomena that are better or more efficient with downsizing, MEMS devices are often faster, consume less power, and are more sensitive and selective.

2.1 Fabrication Technologies

Born out of the IC industry, many basic processing techniques for MEMS have been borrowed or adapted from those used to fabricate ICs. Some examples are photolithography, oxidation, diffusion, ion implantation, chemical vapor deposition (CVD), evaporation, sputtering, wet chemical etching, and dry plasma etching [20]. Many microfabrication techniques, such as bulk etching, Deep Reactive-Ion-Etching (DRIE), LIGA (German acronym for x-ray lithography, electroforming, and molding), wafer bonding, electroplating, and 3D-stereo lithography, have been specifically developed for MEMS over the years [21]. More recently, polymer-based MEMS have become popular, resulting in many new techniques suitable for polymers, such as soft lithography [22–24].

To make a complete MEMS device, several basic microfabrication processes are performed sequentially. These basic microfabrication processes can be classified as either bulk micromachining techniques [25] or surface micromachining techniques [26]. As shown in Fig. 2-1, bulk micromachining uses chemical or plasma selective etching of a substrate material, with the help of masking films, to form structures in the substrate. The etching process can be either isotropic, such as HNA (hydrofluoric acid + nitric acid + acetic acid) or XeF_2, or anisotropic, such as potassium hydroxide (KOH), tetra-methyl

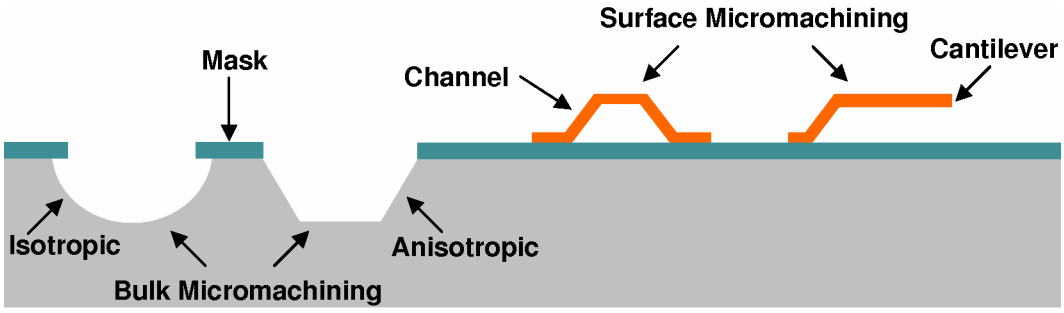


Fig. 2-1. Examples of bulk micromachining and surface micromachining

ammonium hydroxide (TMAH), or DRIE. Surface micromachining, on the other hand, fabricates devices on top of the substrate, usually with the help of sacrificial materials, to form freestanding or even completely released thin-film microstructures, such as micro-channels and micro-cantilevers (Fig. 2-1). Common sacrificial materials used in surface micromachining are photoresist, polyimide, metals, phosphosilicate glass, and polysilicon.

The neurocage is, in general, a surface micromachined MEMS device, although it does utilize some of the bulk micromachining techniques. The basic techniques used in the neurocage fabrication are:

1. Photolithography
2. Oxidation
3. Etching (including both wet chemical and dry plasma etching)
4. Evaporation
5. Chemical Vapor Deposition or CVD (including Plasma-Enhanced CVD or PECVD)

These techniques are described in further detail in the subsequent sections.

2.1.1 Photolithography

Photolithography is the basic tool to fabricate a MEMS device. By creating patterns with photoresist on the substrate, selective regions are then subjected to etching or deposition steps, thus transferring the pattern to the substrate [20–21]. Repeating this procedure of pattern definition followed by etching/deposition with different patterns allows the creation of complex MEMS devices.

There are 3 basic steps to any lithographic process: photoresist application, exposure, and development (Fig. 2-2). The photoresist is a light-sensitive chemical that undergoes a chemical change when exposed to certain wavelengths of light (generally UV light). Conventional photoresists consist of 3 materials: solvent, matrix resin, and photoactive compound (PAC). The solvent keeps the photoresist in a liquid state until it is applied to the wafer and processed. Once the photoresist is spun onto the substrate, the substrate is then soft-baked, during which most of the solvent (approximately 80–90%) is baked out of the photoresist. After removal of the solvent, the matrix resin and the PAC remain. The matrix resin, in the absence of the solvent, provides the photoresist film with its adhesion and etch resistance properties. In other words, the matrix resin ensures the photoresist adheres to the substrate during the subsequent exposure and development steps. In addition, the matrix resin determines the thickness of the photoresist and resists the chemical or plasma etching that follows photoresist development. The last component of conventional photoresists is the PAC. The PAC undergoes a chemical

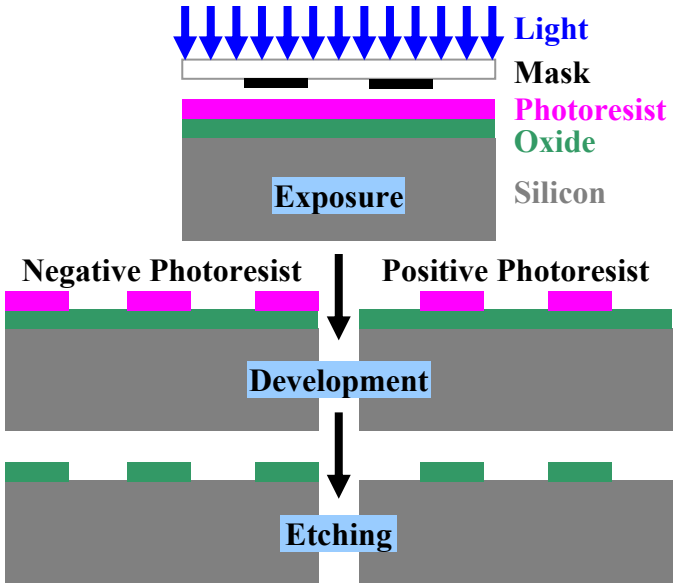


Fig. 2-2. Illustration of the photolithography process for both positive and negative photoresists

reaction in response to exposure to UV light, which then determines the etch rate of the photoresist in developer. In positive photoresists, the PAC, once exposed to UV light, acts as a catalyst, increasing the rate at which the resist will dissolve when placed in the developing solution. In contrast, the PAC in negative photoresists, after exposure to UV light becomes cross-linked and acts as an inhibitor, decreasing the rate at which the resist dissolves when placed in the developing solution.

Once the photoresist is spun on and soft-baked, it is then exposed to UV light through a mask. The mask contains transparent and opaque features that define the pattern to be transferred to the photoresist. The exposure to the UV light activates the PAC, rendering the areas of the photoresist either soluble or insoluble to developing. After exposure, the developer dissolves either the exposed regions of the photoresist (in the case of positive photoresist) or the unexposed regions of the photoresist (in the case of negative photoresist). In both cases, once developing is complete, the features in the mask will have been faithfully replicated in the photoresist. At this point, the exposed substrate can be subjected to a variety of etching or deposition processes. The presence of the photoresist protects the substrate in those regions from the etching or deposition processes. Thus, the features in the masks can be successfully replicated on the substrate.

2.1.2 Oxidation

Silicon dioxide (SiO_2 or oxide) is used in a variety of MEMS applications, including as an insulator for electrodes, mask material for etching processes, and sacrificial material for surface micromachining [20]. There are two main processes for

depositing oxide onto a substrate: thermal oxidation (requires a silicon substrate) and sputtering.

2.1.2.1 Thermal Oxidation

Thermal oxidation involves heating a silicon substrate in an O_2-containing atmosphere [20–21]. Although silicon oxidizes readily in ambient air, even at room temperature, creating native oxide layers approximately 20 Å thick, the elevated temperatures allow thicker layers of oxide to be grown. The high temperature, generally between 600°C and 1250°C, aids in the diffusion of the oxidizing material through the oxide present on the surface to the silicon interface, where it then converts the silicon to oxide. The oxidizing material is either water vapor (wet oxidation) or O_2 gas (dry oxidation). The governing reactions that convert the silicon to oxide are:

$$Si + 2H_2O \rightarrow SiO_2 + H_2 \text{ (Wet Oxidation)}$$

$$Si + O_2 \rightarrow SiO_2 \text{ (Dry Oxidation)}$$

Thermal oxidation is good for growing thin layers of oxide (< 1 μm), which is more than sufficient for most insulating and masking applications. The drawback of thermal oxidation is that the silicon must be free of all metal or polymers, as these materials cannot generally withstand the high temperature and will interfere with the oxidation reaction. This limits the use of thermal oxide as a sacrificial material.

2.1.2.2 Sputtering

Sputtering is a general technique used for the deposition of a wide variety of materials, including oxide, silicon, metals, silicon-nitride, and polysilicon [20–21].

During sputtering, the target (a disc of the material to be deposited) is held at a high negative potential. Positive ions of an inert gas, such as argon or xenon, bombard the target which causes neutral atoms of the target material to be sputtered off. The bombardment, and subsequent sputtering, transfers the momentum of the positive ions to the neutral atoms allowing the neutral atoms to travel to and condense on the substrate.

The use of sputtering to deposit oxide layers does not limit the choice of substrate and sputtered oxide can be deposited on silicon, metal, and polymers. Similar thicknesses are achievable with both sputtered and thermal oxide, although sputtered oxide does not require high temperatures for deposition. Thus, sputtered oxide is ideal for use as a sacrificial material. However, as it often contains impurities, it is less ideal as an insulating material.

2.1.3 Etching

The two main types of etching are wet etching and dry (including plasma) etching [20–21]. Although wet etching is often faster and can provide better selectivity than dry etching, it also requires the use of potentially dangerous acids and solvents. As such, dry etching techniques, requiring only small amounts of chemicals are generally preferred. Some of the other advantages obtained by dry etching are both isotropic and anisotropic etch profiles, directional etching (independent of the crystal orientation of the underlying silicon), high-resolution patterns, and better process control.

2.1.3.1 Wet Etchants

The basic wet etching process involves three fundamental steps. First, the reactants must be transported to the surface. Second, a surface reaction occurs between the reactants and the material to be etched. Finally, the products of the surface reaction must be transported away from the surface. In general, wet etchants contain three key ingredients: an oxidizer, an acid or base to dissolve the oxidized surface, and a diluent in which the reactants and products are transported. Wet etchants can be used to etch silicon, oxide, silicon-nitride, and metals.

Wet etchants can be further classified by the etching profile they produce (Fig. 2–3). Isotropic etchants have the same etch rate in all directions. In other words, the lateral etch rate is the same as the vertical etch rate, and these are independent of the mask or substrate orientation. These etchants will undercut the mask layer if etching continues long enough. For anisotropic etchants, the etch rate depends on the crystal orientation of

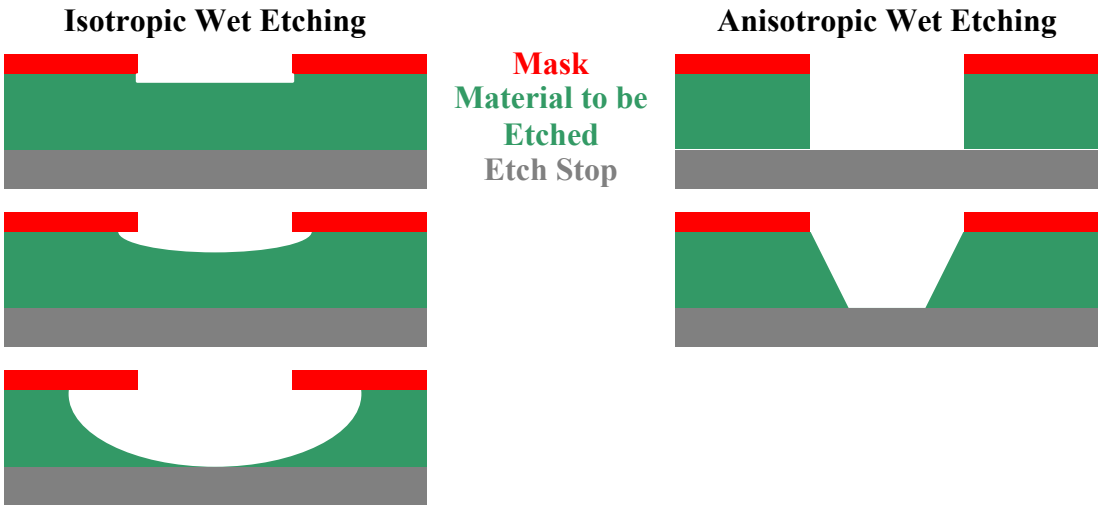


Fig. 2-3. These illustrate the differences between isotropic and anisotropic wet etching. The left image shows a time series for isotropic wet etching. As the vertical etching continues, the masking material is undercut as the etching also continues laterally. The right image shows two possible anisotropic etching profiles. As can be seen, the masking material is not undercut.

the material to be etched. Thus, the lateral etch rate can be significantly larger or smaller depending upon the orientation of the mask to the crystalline axes of the substrate.

2.1.3.2 Dry Etchants

There are two main types of dry etching: non-plasma based and plasma based. Non-plasma-based dry etchants are isotropic and generally limited to etching silicon. These etchants typically are fluorine-containing gases, such as xenon difluoride or bromine trifluoride, that readily etch silicon. The etch rate is easily controlled by the temperature and pressure of the reactants.

Plasma-based dry etching (plasma etching) employs the use of plasma to etch the substrate. Plasma is a partially ionized gas consisting of equal numbers of positively (ions) and negatively (electrons) charged species, as well as a large number of neutral (un-ionized molecules). Ion-electron pairs are constantly created by ionization and destroyed by recombination. Plasma is generated by filling a chamber with the required gases and applying DC or RF energy to a pair of electrodes. The applied energy accelerates the electrons, thereby increasing their kinetic energy. The electrons collide with the neutral gas molecules forming more ions and electrons. Plasma is created when steady state is reached and the ionization rate of the molecules equals the recombination rate. Like wet etchants, plasma etching can be used to etch silicon, oxide, silicon-nitride, and metals. In addition, plasma etching can be used to etch organic films, including photoresist and polymers.

There are four types of plasma etching: physical etching, chemical etching, Reactive-Ion Etching (RIE), and Deep Reactive-Ion Etching (DRIE). Physical etching

(often called sputter etching) is based on the physical bombardment of the substrate with ions. The plasma is used to energize a chemically inert molecule. When this molecule strikes the surface, the substrate atoms are dislodged. Physical etching is highly anisotropic, although it has very low-selectivity, often etching the masking material at the same rate as the underlying substrate. In chemical etching, the plasma is used instead to produce chemically reactive species from the gas. These chemically reactive species diffuse and adsorb to the surface, react with the surface molecules to be etched, and the resulting products are desorbed and diffuse away. This isotropic etching process is similar to the wet etching process. The RIE process is actually a combination of physical and chemical etching. The chemical etching is assisted by the ionic bombardment (physical etching), as the bombardment creates more areas for the chemical reactions to occur. The RIE process, because of the ionic bombardment, is more anisotropic and faster than the chemical etching process, however, it also has much lower selectivity. The DRIE process uses inductively coupled plasma (ICP) technology or microwave electron cyclotron resonance (ECR) to create the plasma [27–29]. This creates a high-density, low-pressure, low-energy plasma, leading to increased etch rates, high selectivity, increased ion directionality (resulting in less side-wall etching), and less damage (caused by ion bombardment). Thus, the DRIE process is highly anisotropic, with very large aspect ratios possible.

2.1.4 Evaporation

A variety of different kinds of films can be deposited by evaporation [20–21]. Both evaporation and sputtering (described in Section 2.1.2.2) are examples of physical

vapor deposition (PVD) in which the material to be deposited is first vaporized from a source and then condensed onto the substrate. Evaporation is one of the oldest techniques for depositing thin films (generally metals). Thermal evaporation is based on the boiling off, or sublimating, of metal onto a substrate. It is generally performed under vacuum to eliminate any potential contaminants (including oxygen which can oxidize the deposition metal) and to increase the mean free path of the molecules boiled off, ensuring the majority of them reach the substrate. The two primary means for heating the deposition material are resistive and electron beam (often called e-beam evaporation). In resistive heating, the metal is contained in a highly resistive container (e.g., a tungsten boat) and a high current is passed through the container heating it and causing the metal to evaporate. In electron beam heating, an electron beam is magnetically focused onto the target metal causing it to locally melt and evaporate.

As mentioned in Section 2.1.2.2, it is possible to deposit metal films using sputtering. Some advantages of using evaporated metal are higher deposition rates, less substrate heating, and fewer impurities, due both to the higher vacuum and the fact that in evaporation a new charge of metal is used for each deposition, as opposed to sputtering where the target is re-used for multiple depositions.

2.1.5 Chemical Vapor Deposition (CVD)

The basic mechanism of chemical vapor deposition (CVD) is that starting material is vaporized and then chemically reacts with the molecules on the surface to create the desired deposited material [20–21]. CVD starts by moving the reactant gases (often diluted with an inert carrier gas) into the main reaction chamber. As the gases

flow through the chamber, the reactant gas transports to the surface. The reactants, now called adatoms, are adsorbed onto the substrate surface. The adatoms migrate to the growth sites where the film-forming reactions take place creating the solid film and gaseous by-products. Once the gaseous by-products are desorbed from the surface, the gas flow through the reaction chamber removes the gaseous by-products. The energy to drive these chemical reactions can be supplied by several different methods: thermal energy, photonic energy, or electrons. There are a variety of different types of CVD classified by the pressure at which the deposition takes place: Atmospheric-Pressure (APCVD), Low-Pressure (LPCVD), and Plasma-Enhanced (PECVD).

In PECVD, plasma is responsible for creating the radicals that eventually form the deposited films. The ion bombardment of the substrate provides the energy required to form the film. APCVD and LPCVD both rely on thermal energy for creating the radicals and forming the film. The main advantages of PECVD are the lower substrate temperature required, in the range of 300°C to 400°C, and the good step coverage. PECVD is ideal for low-temperature insulators, such as silicon-nitride. LPCVD also achieves good step coverage, although the deposition rate is less than that for PECVD. It is ideal for high-temperature oxides, silicon-nitride, and polysilicon. Unfortunately, LPCVD requires substrate temperatures in the range of 550°C to 600°C. APCVD, like PECVD, does not require high temperatures and has a high deposition rate. However, APCVD has poor step coverage.

2.2 Parylene

Parylene (poly-para-xylylene) is the generic name for a family of vapor phase deposited thermoplastic polymers [30]. Fig. 2-4 shows the chemical structures for the three most commonly used types of Parylene: Parylene-N, Parylene-C, and Parylene-D.

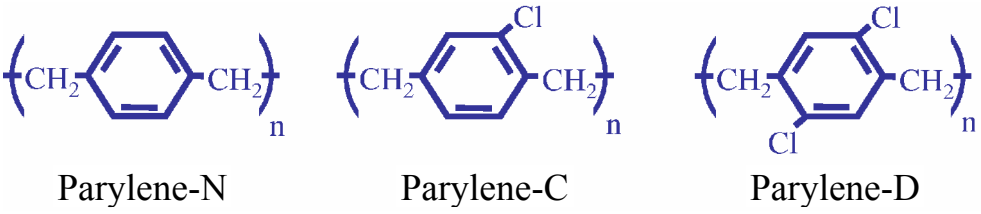


Fig. 2-4. Chemical structures for the three most common types of Parylene

2.2.1 Parylene Deposition

Parylene is deposited at room temperature using CVD [30]. The deposition process and corresponding chemical changes are shown in Fig. 2-5. This figure details the deposition process for Parylene-N; however, the process is identical for all three common types of Parylene, except for some slight differences in pyrolysis temperature and deposition pressure.

To start, Parylene dimer (di-para-xylylene), a stable, granular compound, is placed in the vaporizer and the substrate to be coated in the deposition chamber. The whole system is pumped down to medium vacuum (~ 10 mTorr). The dimer is heated in the vaporizer until it sublimates at about 160°C. The dimer vapor enters the pyrolysis furnace, which is heated to 690°C, where it is cleaved into monomers (para-xylylene). In the room temperature deposition chamber, the monomers reunite on all exposed surfaces as the polymer poly-para-xylylene. The deposition takes place at the molecular level as the monomers are extremely active with a mean free path on the order of 1 mm (under

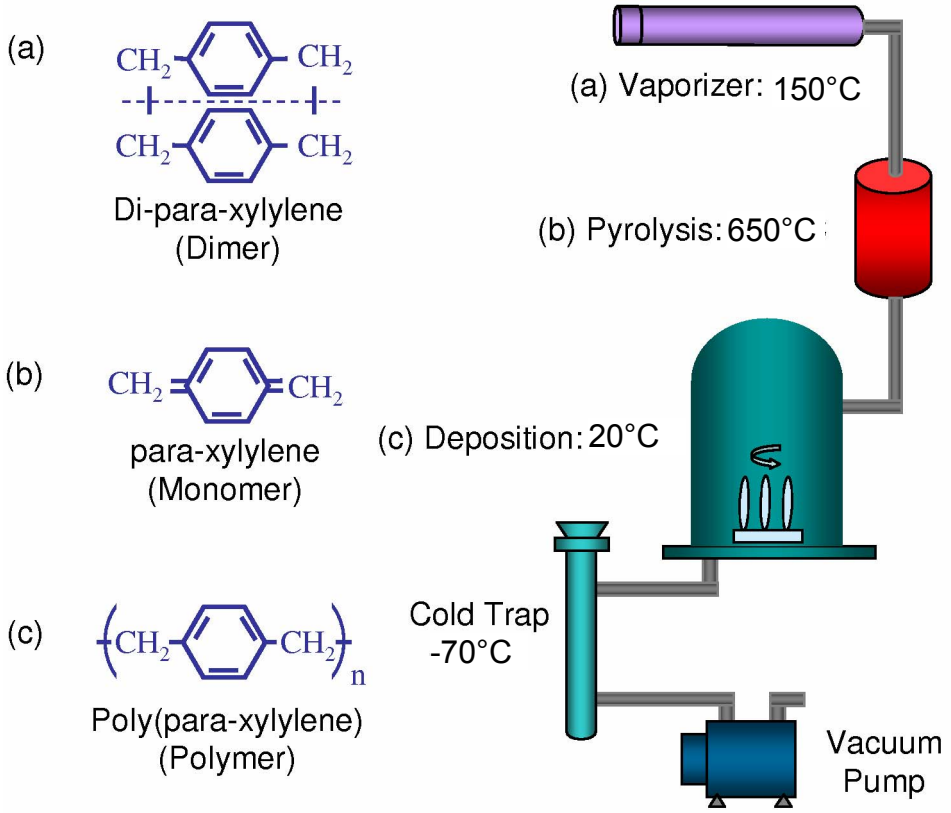


Fig. 2-5. Schematic of the Parylene deposition system and the associated chemicals. This process shows the deposition parameters for Parylene-N. The same procedure is used for the deposition of both Parylene-C and D, with slight changes in deposition pressure and pyrolysis temperature.

the deposition pressure of ~ 100 mTorr). This results in superior penetration power and a high degree of conformability to the surfaces being coated. The temperature of the coated substrate inside the deposition chamber never rises more than a few degrees above room temperature.

The deposited Parylene film is highly conformal and truly pinhole free. Typical coating thicknesses range from one to tens of microns, although they can be as thin as hundreds of angstroms. The coating thickness is controlled by the amount of dimer used. The average deposition rate for Parylene-C is about 5 μm per hour. The deposition rate is

directly proportional to the square of the monomer concentration and inversely proportional to the absolute temperature [30].

2.2.2 Parylene Properties

Parylene is an excellent barrier to gas and moisture. In addition, Parylene is extremely inert to most chemicals and solvents. Based on the manufacturer's study [30], solvents can cause minor swelling in Parylene, causing a 3% maximum increase in film thickness. This swelling is completely reversible, however, after the solvents are removed by vacuum drying. Inorganic reagents, except for oxidizing agents at elevated temperatures, have little effect on Parylene. Parylene is also biocompatible (USP Class VI), which means it is safe for long-term human implants. These properties also make Parylene well-suited for cell culture experiments.

Parylene exhibits impressive mechanical strength and flexibility in thin film coatings. Thus, it can be used to make both rigid structures and flexible actuators.

Parylene is also an excellent electrical insulator [31–36], as well as a good thermal insulator.

Optically, Parylene is transparent in the visible light range. It only absorbs light with wavelengths under 280 nm.

Due to their slightly different chemical structures, the three types of Parylene also differ in properties. Parylene-N has the best penetration characteristics; however, it also has the slowest deposition rate. Parylene-D can withstand higher temperatures than Parylene-C. Parylene-C, though, has a useful combination of electrical and physical properties, plus a very low permeability to moisture and corrosive gases. In addition, the

deposition rate of Parylene-C is faster than the other two types. Therefore, Parylene-C is the choice for most biological and electrical applications, including the neurocage.

Detailed electrical, mechanical, thermal, barrier, optical, and other properties can be found on a Parylene vendor's website [30]. A list of selected properties for Parylene-N, C, and D are shown in Table 2-1.

	Parylene-N	**Parylene-C**	**Parylene-D**
Dielectric Constant (1kHz)	2.65	3.10	2.82
Volume Resistivity (x10^{16} Ω-cm)	14	8.8	12
Young's Modulus (GPa)	2.42	2.76	2.62
Density (g/cm^3)	1.1	1.3	1.4
Melting Temperature (°C)	420	290	380
Glass Transition Temperature (°C)	N/A	80-100	N/A
Thermal Conductivity at 25°C (mW/(cm-K))	1.26	0.84	N/A
Moisture Vapor Transmission at 90%RH, 37°C (g-mil/100in^2-d)	1.5	0.21	0.25
Water Absorption (% after 24 hours)	<0.1	<0.1	<0.1

Table 2-1. Selected properties for Parylene-N, C, and D

CHAPTER 3
Neurocages on Silicon without Electrodes

Neurocages allow individual neurons within a larger neural network to be stimulated and action potentials to be recorded. The "cage" structure counteracts the problems encountered when using multi-electrode arrays in which the lack of neuron-to-electrode specificity and the inherent neuron mobility make it difficult to stimulate and record from single neurons during long-term studies [10–12]. The surface micromachining techniques used in the fabrication of the neurocages eliminate the fabrication difficulties common to other bulk micromachined "cages," such as the neuro-well [10, 15–17].

Three essential elements must be determined to create a functional neurocage, capable of stimulating and recording. First, a proper geometry must be found, one capable of both effectively trapping neurons and allowing neurite outgrowth to form neural networks. Second, suitable materials for fabricating the neurocage must be selected. Finally, a fabrication process to integrate the materials to create the desired geometry must be developed.

3.1 Design Components

The three basic components of the neurocage are the anchors, the tunnels, and the chimney (Fig. 3-1). The anchors ensure the neurocage remains firmly attached to the substrate. The tunnels, while small enough to prevent the neurons from escaping the neurocage, are large enough to permit neurites to extend out of the neurocage and form synaptic connections with neighboring neurons. The chimney, including the loading hole through which the neuron is placed into the neurocage, is the central area in which the neuron lives and grows.

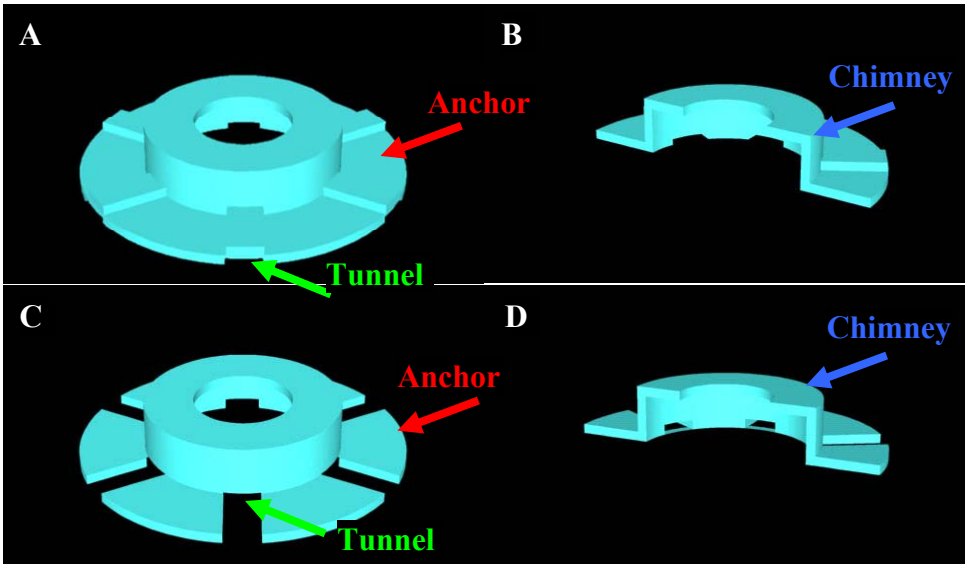


Fig. 3-1. Two different neurocage designs: long tunnels (**A** and **B**) and short tunnels (**C** and **D**). The arrows denote the anchors (red), tunnels (green), and chimneys (blue). (Not drawn to scale)

3.1.1 Anchors

The Parylene-C used to form the neurocage does not adhere well to the silicon substrate. Chemical methods, such as the A-174 Parylene Adhesion Promoter (gamma-Methacryloxypropyltrimethoxy Silane**,** Specialty Coating Systems, Indianapolis, IN),

generally used to improve the adhesion between Parylene-C and the silicon are not effective for the neurocage due to the extremely small area that is in direct contact with the silicon. Hence, the neurocages require a structural method to anchor the Parylene-C to the silicon.

One structural method for creating anchors is to roughen the silicon, using gas-phase etchants, like xenon difluoride (XeF_2) or bromine trifluoride (BrF_3), or wet etchants, such as HNA (a mixture of hydrofluoric, nitric, and acetic acids). This increases the surface area of the silicon to which the Parylene-C will be in contact, without increasing the total area of the neurocage. Other chemical methods can also be used in conjunction with the roughened silicon to further improve the adhesion. Unfortunately, while the roughened silicon improves adhesion, the etchants are isotropic and can produce severe undercut of the neighboring tunnels (Fig. 3-2). This decreases the effective tunnel width through which the neurites can grow. If the tunnels are too narrow, the neurons will not extend through the tunnels and, thus, will not form synaptic

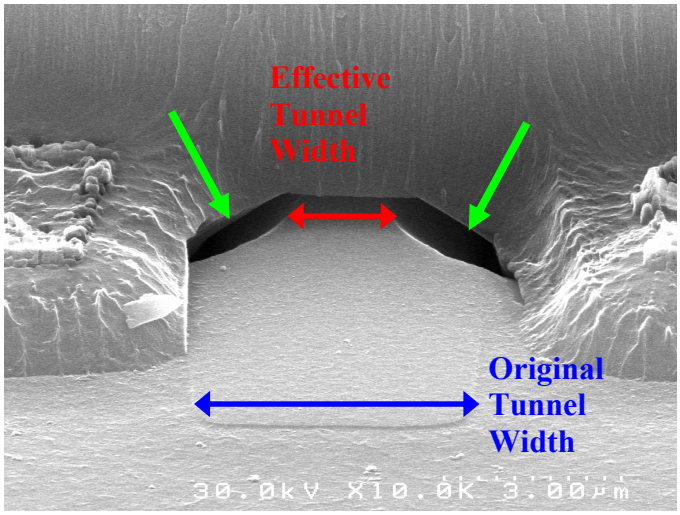


Fig. 3-2. Scanning electron micrograph of a tunnel and anchors etched with XeF_2. The green arrows denote the anchor undercut extending into the tunnels, effectively narrowing the tunnel.

connections with nearby neurons.

An alternative method uses a combination of isotropic and anisotropic etchants to create a locking structure, with virtually no undercut. This process uses Deep-Reactive-Ion Etching (DRIE) to create an inverted mushroom structure that, when filled with Parylene-C, securely anchors the Parylene-C to the silicon (Fig. 3-3) [37]. First, a standard Bosch process [38] is used to create the vertical "mushroom stalk." The Bosch process uses alternating sulfur hexafluoride (SF_6) and fluorocarbon (C_4F_8) plasmas. A short exposure to SF_6 plasma will etch the silicon isotropically. The C_4F_8 plasma then creates a Teflon-like passivation layer on the bottom and sidewalls of the hole. This passivation protects the sidewalls from further etching during the subsequent exposures to SF_6 plasma. The bottom is not protected from etching by the passivation layer since the SF_6 ions are directional in the DRIE and travel vertically down the hole. Thus, the passivation layer at the bottom is quickly etched off by the SF_6 ions, exposing the silicon for etching by the SF_6 plasma. Repeating this alternating etching and passivation process

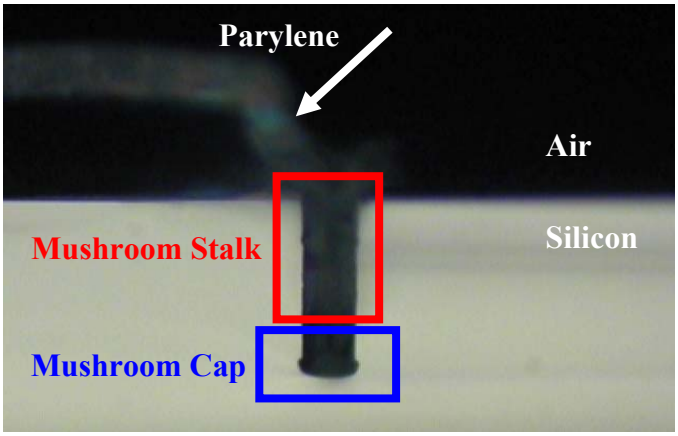


Fig. 3-3. Scanning electron micrograph of an anchor etched into silicon and filled in with Parylene-C. The red outlines the anisotropically etched mushroom stalk and the blue outlines the isotropically etched mushroom cap.

yields a highly anisotropic structure that forms the mushroom stalk. Next, a longer SF_6 plasma etch creates the "mushroom cap." The sidewalls are still protected from etching by this SF_6 plasma etch from the previous C_4F_8 passivation step (the last step in the Bosch process creating the mushroom stalk), so only the bottom is etched isotropically by the SF_6 plasma. Since the Parylene-C deposition is conformal, this inverted mushroom structure will be completely filled by the Parylene-C forming the neurocages. This method, unlike the first method, does not rely on the adhesion of the Parylene-C to the silicon, but rather mechanically locks the Parylene-C to the silicon creating a more robust structure capable of withstanding a variety of chemical and mechanical treatments and increasing the reusability of the neurocages. In addition, the mostly anisotropic etching process virtually eliminates any undercut, ensuring that the tunnels remain the desired width.

Each neurocage has six anchors. The anchors are approximately trapezoidal, with an area of 60 μm^2 or 90 μm^2, for 10 μm or 5 μm wide tunnels, respectively. The anchors and the tunnels are interleaved with one another and separated by 4 μm. The separation allows for slight misalignment of the various layers during fabrication. The anchors are 50–60 μm deep, although the depth of the anchors is not critical, provided the inverted mushroom structure is present.

3.1.2 Tunnels and Chimneys

The neurocages each have six tunnels and one chimney. The size of the neurons used for the experiments dictates the dimensions of the tunnels and chimney. These experiments used embryonic rat neurons, which are approximately 10–15 μm in diameter

when loaded into the neurocages and grow to be approximately 25 μm in diameter. The neurons flatten themselves against the bottom silicon surface as they extend their neurites; hence when full grown, the neurons are more like a thin disc rather than a sphere. Based on this information, the chimney was designed to be 30 μm in diameter and between 4 μm and 15 μm tall. The neurites are cylindrical, approximately 1 μm in diameter, and can grow to be 0.5–1 mm in length. The tunnels must be large enough to allow neurite outgrowth, as well as enable the neuron to sense its neighbors, while at the same time small enough to prevent the neuron from squeezing through the tunnel to escape from the neurocage. Several different combinations of tunnel width and length were explored to best balance these two criteria. The chosen tunnel widths are 5 μm and 10 μm and the tunnel lengths are 4 μm and 25 μm. The desired tunnel height is between 1 μm and 2 μm.

3.1.2.1 Sacrificial Materials

The tunnels and chimneys are formed by patterning sacrificial materials. Once the Parylene-C is deposited and patterned to form the outer neurocage structure, the sacrificial materials are then removed. The most common sacrificial materials are photoresist (both soft-baked and hard-baked), silicon, and metal. The metal used is typically aluminum as it is both relatively inexpensive and easy to deposit and remove. Table 3-1 summarizes the advantages and disadvantages of these materials.

Deposition and patterning of photoresist, both soft-baked and hard-baked, is simple and small structures (less than 1 μm wide) can be easily made. The patterning of

both the silicon and aluminum is relatively simple; however, the deposition is much more complicated, requiring sputtering or evaporation.

	Deposition	**Removal**	**Thickness**	**Usable for Chimneys**	**Usable for Tunnels**
Soft-Baked Photoresist	Easy	Easy	0.5–100 μm	Yes	Yes†
Hard-Baked Photoresist	Easy	Hard*	0.5–100 μm	Yes	Yes
Silicon	Difficult	Hard*	< 1 μm	No	Yes
Aluminum	Difficult	Medium	< 1 μm	No	Yes
* Removal agents may damage other materials and structures present. † Requires chimneys also to be made of soft-baked photoresist. Only limited chimney heights are possible.					

Table 3-1. Advantages and disadvantages of potential sacrificial materials

Soft-baked photoresist can be easily removed with acetone, which will not damage the other materials and structures present. Aluminum is slightly more difficult to remove, as it requires the use of mild acids or bases. Hard-baked photoresist and silicon require harsher chemicals, typically strong acids and strippers, and longer times to ensure complete removal of the sacrificial material. These harsher chemicals may cause damage to the other materials and structures present, especially since long exposures are generally required.

Typical photoresist thicknesses, both soft-baked and hard-baked, are between 0.5 μm and 100 μm. Potential silicon and aluminum thicknesses, however, are limited to less than 1 μm.

The tunnels and chimneys do not need to be made of the same sacrificial material. Soft-baked and hard-baked photoresist can easily be used for the chimneys. Silicon and aluminum cannot be used for the chimneys, as the desired chimney height (4–15 μm) is

greater than the 1 μm limit. All of the sacrificial materials can be used for the tunnels, as the desired tunnel height is 1 μm. If the tunnels are made using hard-baked photoresist, aluminum, or silicon, then either hard-baked or soft-baked photoresist can be used for the chimneys. However, if soft-baked photoresist is used for the tunnels, then it must also be used for the chimneys. In addition, the partial-exposure method, described in Section 3.4.1, must be used, which further constrains the heights and widths of the tunnels and chimneys. In general, the step height created by the partial-exposure method, in this case the height difference between the tunnels and the chimneys, must be smaller than the width of the tunnels. For example, if the tunnel height is 1 μm and the chimney height is 15 μm (a height difference of 14 μm), then the tunnel width must be greater than 14 μm.

3.1.3 Neurocage Arrays

4 x 4 arrays of neurocages, centered within a 440 μm x 440 μm square, were used for the culturing experiments. The use of surface micromachining techniques ensures that larger arrays can be easily fabricated, however, without changing the basic neurocage design or the fabrication process.

3.2 Aluminum Sacrificial Material

3.2.1 Fabrication

The first neurocage fabrication process used thermally evaporated aluminum as the sacrificial material for the tunnels and soft-baked photoresist as the sacrificial material for the chimneys. The tunnels were 5 μm wide, 25 μm long, and 1 μm high.

The chimneys were 30 μm in diameter and 15 μm high. An outline of the fabrication process is shown in Fig. 3-4.

The fabrication process begins by first cleaning the silicon wafer thoroughly in piranha, a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), heated to 120°C, and followed by hydrofluoric acid (HF). These both remove any potential organic or metallic contaminants on the silicon. Next, a thin layer, 0.5 μm, of thermal oxide is grown on the silicon. The silicon wafer is again cleaned in piranha and HF to prepare for the aluminum deposition.

The silicon wafer is baked at 100°C for 10 minutes, to remove remaining water molecules from the surface, and is then treated with hexamethyldisilazane (HMDS) for 2 minutes. The HMDS bonds with the oxide and enhances the adhesion of the photoresist to the oxide [20]. A thin layer of photoresist, less than 0.5 μm thick, is then spun onto the wafer and soft-baked at 100°C for 30 minutes. This layer of photoresist is then completely exposed and a second, thicker layer (4–5 μm) is spun onto the wafer and baked at 100°C for 30 minutes. Next, the photoresist is exposed and developed to create the openings where the aluminum will form the tunnels. The bottom layer of photoresist is used to create an undercut in the photoresist sidewalls, which will ensure a clean lift-off after the metal has been deposited. Using two layers of photoresist eliminates a common problem that can occur when using only one layer of photoresist (Fig. 3-5A). During deposition, the metal completely covers the sidewalls of the photoresist, forming a single continuous layer of metal. The metal lift-off does not occur because there are no openings in the metal to remove the underlying photoresist. When using two layers of

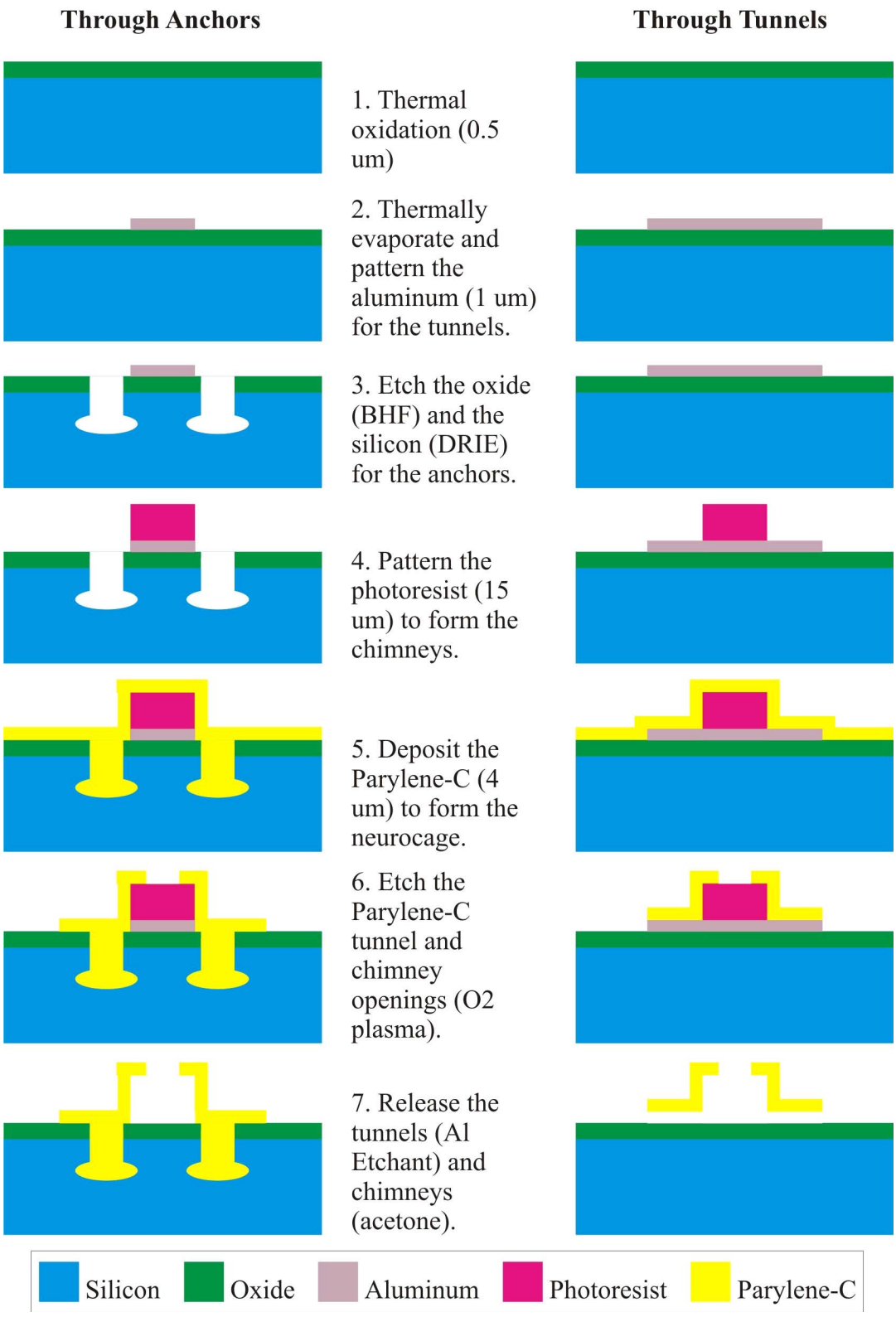


Fig. 3-4. Process flow for the neurocages on silicon with aluminum as the sacrificial material for the tunnels and soft-baked photoresist as the sacrificial material for the chimneys. (Not drawn to scale.)

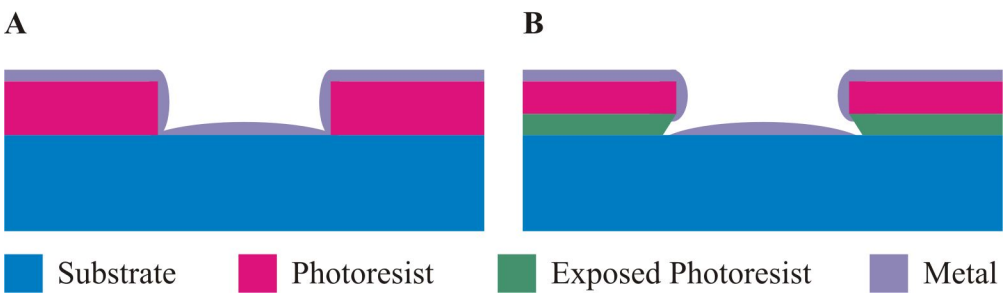


Fig. 3-5. Fig. **A** depicts a common problem when doing metal lift-off with only a single layer of photoresist. The metal lift-off does not occur because there are no openings in the metal to remove the underlying photoresist. Fig. **B** depicts the results when using two layers of photoresist for metal lift-off. The bottom layer of photoresist (in green) is exposed prior to spinning on the top layer of photoresist (in pink). The sidewalls of the bottom layer of photoresist are not coated in metal, due to the undercut, and thus, the underlying photoresist and the unwanted metal on top can be easily removed.

photoresist, the bottom layer is exposed prior to spinning on the top layer of photoresist (Fig 3-5B). When the top layer of photoresist is subsequently exposed, the bottom layer is exposed again (i.e., the bottom layer is over-exposed). Hence, during developing, the bottom layer of photoresist will develop faster and create an undercut structure, similar to the one shown in Fig. 3-5B. During the metal deposition, the metal may cover the sidewalls of the top layer of photoresist, but due to the undercut, it does not cover the sidewalls of the bottom layer of photoresist. Thus, the underlying photoresist, and the unwanted metal on top, can be easily removed during metal lift-off. Following the exposure and development of the two layers of photoresist, the wafer is then treated briefly with oxygen (O_2) plasma and HF to ensure all of the photoresist in the tunnel openings has been removed. The aluminum is thermally evaporated in two consecutive depositions, totaling 1 μm. (The thermal evaporator used during fabrication can accommodate only a limited amount of un-melted aluminum, typically only enough to deposit 0.5 μm.) The photoresist underneath the undesired aluminum is then dissolved in

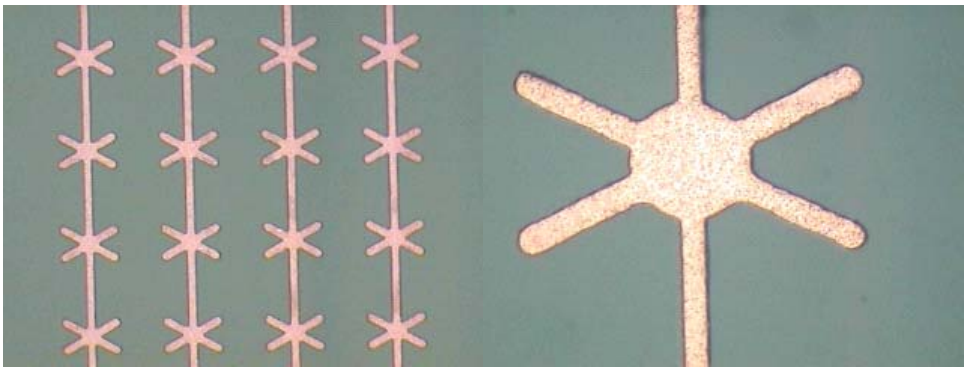


Fig. 3-6. Optical images showing the patterned sacrificial aluminum for the tunnels. The left image shows the tunnels for a 4 x 4 array of neurocages and the right image is a close-up of the tunnels for a single neurocage.

acetone with ultrasonic agitation, leaving only the aluminum for the tunnels on the surface (Fig. 3-6). The resulting tunnels were 0.95 μm (± 0.14 μm) tall.

The silicon wafer is again baked at 100°C for 10 minutes and treated with HMDS for 2 minutes. A single layer of photoresist, less than 2 μm thick, is spun on, soft-baked at 100°C for 30 minutes, and patterned to form the openings for the anchors. A brief O_2 plasma treatment is done to ensure all of the photoresist in the anchor openings has been removed. The anchors are first etched into the oxide using a buffered HF (BHF) solution. Subsequently, the anchors are etched into the silicon using the DRIE process outlined in

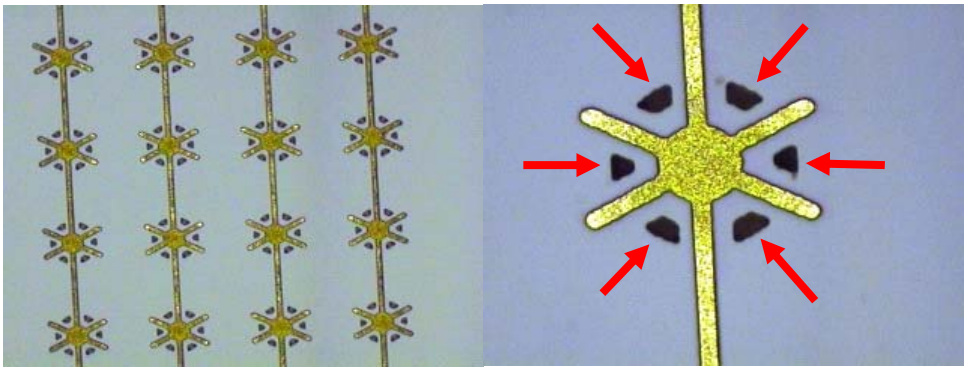


Fig. 3-7. Optical images showing the anchors that have been etched into the silicon, as well as the patterned sacrificial aluminum for the tunnels. The left image shows a 4 x 4 array and the right image is a close-up of a single neurocage (the red arrows point to the 6 anchors).

Section 3.1.1. Finally, the photoresist is stripped in acetone (Fig. 3-7).

After baking the silicon wafer at 100°C for 10 minutes and treating it with HMDS for 2 minutes, the single layer of photoresist (15 μm) is spun on and soft-baked at 100°C for 30 minutes. The photoresist is then exposed and developed to form the chimneys (Fig. 3-8). The resulting chimneys are 15.28 μm (± 0.51 μm) tall. After a brief O_2 plasma treatment to ensure all extraneous photoresist has been removed, a single layer of Parylene-C, approximately 4 μm thick, is deposited, filling the anchors, to form the neurocage.

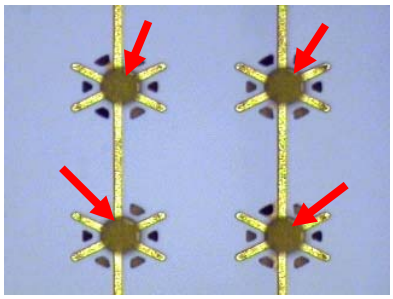


Fig. 3-8. Optical image showing the photoresist chimneys (denoted by the red arrows)

Next, a single layer of photoresist, 15 μm thick, is spun on and soft-baked at 90°C for 40 minutes. Since there is soft-baked photoresist underneath the Parylene-C forming the chimneys, this photoresist is soft-baked at a lower temperature than the previous layers. The photoresist forming the chimneys still contains some solvent (hence, it is soft-baked, not hard-baked) and if baked at too high a temperature the remaining solvent will out-gas, potentially causing the covering Parylene-C to bubble, and the photoresist will become hard-baked, making it more difficult to remove. By soft-baking the top layer of photoresist at a lower temperature, the out-gassing of the chimney photoresist is minimized. The openings for the tunnels and chimneys are then exposed and developed.

O_2 plasma is then used to etch the Parylene-C to form the final neurocage. Once etching is complete, the sacrificial aluminum and photoresist for the tunnels and chimneys are removed in Aluminum Etchant Type A (Transene Company, Danvers, MA) and acetone, respectively. Finally, the resulting chips are cleaned in piranha and HF to prepare them for culturing. Scanning electron micrographs (SEMs) of the final neurocages are shown in Figs. 3-9 and 3-10.

3.2.2 Culturing Results

Once the neurocages have been fabricated and cleaned, they are first sterilized with UV light to prepare them for cell culture. The neurocages are then covered with 95% ethyl alcohol (EtOH). Due to the small openings, many liquids, including water, do not easily penetrate the neurocages. Fortunately, EtOH easily travels through the tunnels and chimneys and reaches the interior of the neurocage. Unfortunately, the EtOH is toxic to neurons, so it is exchanged for water. A 5% PEI (poly-ethylene-imine) solution is then added to improve the cell adhesion to the surface. The PEI is rinsed out of the dish and

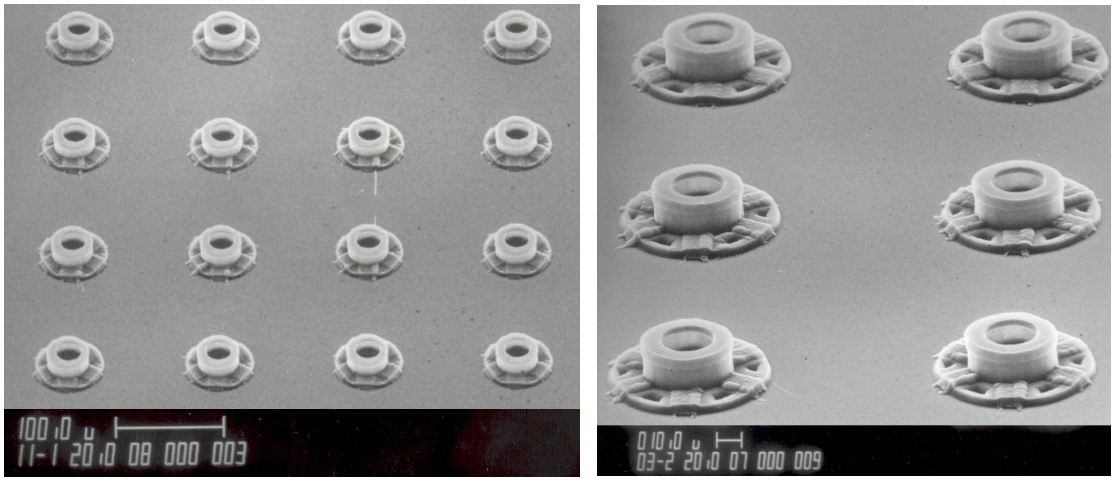


Fig. 3-9. SEMs of neurocage arrays

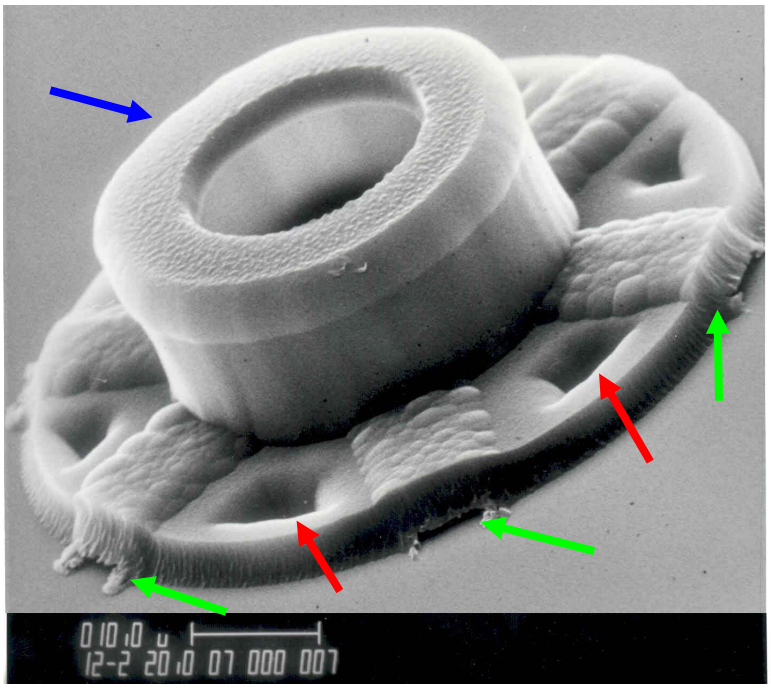


Fig. 3-10. SEM of a single neurocage. The green arrows indicate the tunnels, the red arrows indicate the anchors, and the blue arrow indicates the chimney.

subsequently replaced by neurobasal medium. Embryonic rat neurons (E18) are used for all of the culturing experiments. The neurons are then plated to a density of 30 K/cm^2 on the edges of the chip. Individual neurons are loaded manually into the neurocages with a pressure-driven micropipette. The first signs of neuron growth usually appear within 12–24 hours of loading.

Unfortunately, the survival rate for these neurons was extremely low. Fewer than 25% of the neurons survived for more than 5 days and extended neurites out through the tunnels. The remaining neurons died within 3–4 days. There are two potential reasons for the low neuronal survival rate. First, it is possible that the tunnel sacrificial material was not completely removed. The SEMs (Figs. 3-9 and 3-10) clearly show that the tunnel exits are open and clear of aluminum. However, it is impossible to determine whether the entire length of the tunnel was clear of aluminum using the SEMs. Attempts

were made to put fluorescent dye into a chimney using a micropipette, with the assumption that if the tunnels were clear of aluminum they would fluoresce when the dye entered them. Unfortunately, putting the dye directly into a chimney proved unfeasible, as the dye generally covered the top of the neurocage, including the tops of the tunnels, rendering the results useless. The second possible cause for the low survival rate is that the geometry of the neurocages is not well suited for these neurons. Since some of the neurons did survive, it was decided that the incomplete remove of the tunnel sacrificial material was the most likely cause of the low survival rate. As a result, a different material, hard-baked photoresist, was chosen as the new tunnel sacrificial material.

3.3 Hard-Baked Photoresist Sacrificial Material

3.3.1 Fabrication

With the lack of success of the aluminum tunnels, hard-baked photoresist was then explored as the sacrificial material for the tunnels. The neurocage dimensions remain unchanged. The tunnels are still 5 μm wide, 25 μm long, and 1 μm high. The chimneys are 30 μm in diameter and 15 μm high.

The fabrication process is identical to that that outlined in Fig. 3-4 and detailed in Section 3.2.1, except for the tunnel sacrificial material. Instead of depositing 1 μm of aluminum for the tunnels, a single layer of photoresist is spun on. Once it is exposed and developed, it is hard-baked at 140°C for 30 minutes to remove the remaining solvent. This also makes the photoresist more resistant to further development, ensuring that the tunnels will not be completely developed away when developing the photoresist for the

chimneys. In addition, in the previous process, the anchors were etched after the aluminum for the tunnels was deposited and patterned. In this process, though, the anchors are etched before the photoresist for the tunnels is patterned, to minimize the number of subsequent developing steps to which the tunnel photoresist is subjected.

SEMs of the resulting neurocages are shown in Fig. 3-11. As can be seen, the tunnels are clearly defined, although like the previous neurocages only the tunnel exits are definitively open. The SEMs do not show whether the tunnel entrances inside the chimneys or the tunnel lengths are open. More troubling, however, are the anchors. Fig. 3-11B shows that the Parylene-C filling the anchors is actually lifting out of the anchor holes, causing the neurocage itself to lift off the silicon surface. The most likely cause is

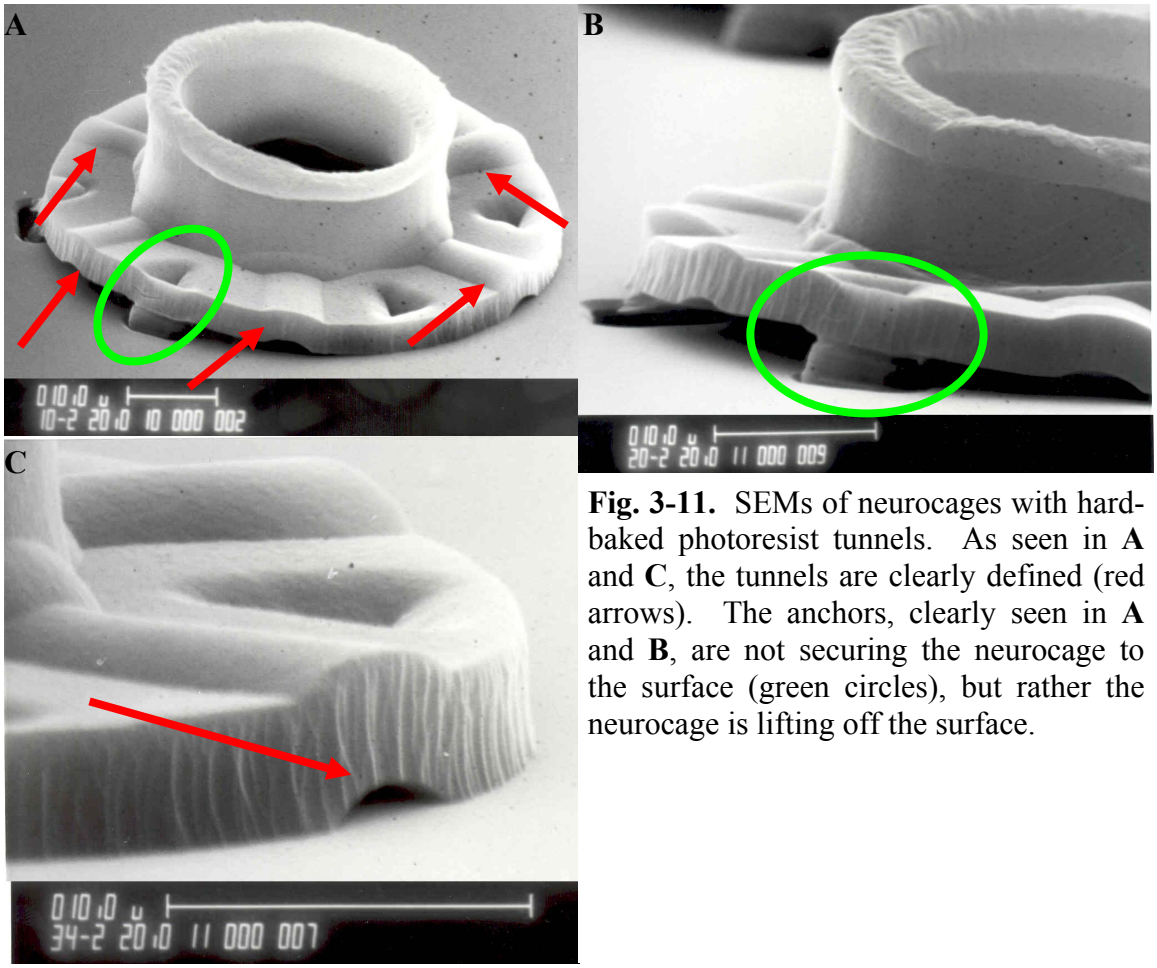


Fig. 3-11. SEMs of neurocages with hard-baked photoresist tunnels. As seen in **A** and **C**, the tunnels are clearly defined (red arrows). The anchors, clearly seen in **A** and **B**, are not securing the neurocage to the surface (green circles), but rather the neurocage is lifting off the surface.

that the anchor holes are not completely free of photoresist. Any photoresist, especially low-viscosity photoresists used for thin layers like the tunnels, that is spun on after the anchor holes are etched can get into the anchor holes themselves. Depending upon the depth of the anchor holes, and the depth to which the photoresist fills the holes, the photoresist may not get exposed and developed away. If the photoresist remains in the bottom mushroom-cap, the resulting anchor hole does not have the desired inverted mushroom structure and is merely a hole in the silicon. This hole does not provide any means for mechanically locking the Parylene-C into place. The best means to ensure the anchor holes remain free of photoresist is to etch them after all of the photoresist has spun on and developed. Due to the anchoring problems with these neurocages, they were not used in culturing experiments. Rather, a new process was developed to counteract the anchoring problems.

3.4 Soft-Baked Photoresist Sacrificial Material

In addition to counteracting the anchoring problems encountered in the previous version, this new process also attempts to eliminate any potential tunnel blockage [39–42]. In the previous versions of the neurocage, although the tunnel exits were clearly free of any sacrificial material, the results were ambiguous for the remaining tunnel length. Two means are incorporated to eliminate this ambiguity. First, a shorter tunnel length, 4 μm (the thickness of the Parylene-C comprising the neurocage) instead of 25 μm, is also used. It is believed that this shorter tunnel will allow a clear view of the entire tunnel length. Second, the sacrificial material for the tunnels is changed to soft-baked

photoresist. Soft-baked photoresist is extremely easy to remove, requiring only acetone. The drawback, however, is its use will limit the chimney dimensions.

3.4.1 Fabrication

With this new fabrication process, several different combinations of tunnel length and width were tried. The tunnel lengths are 25 μm and 4 μm and the tunnel widths are 5 μm and 10 μm. The 25 μm tunnel length is not abandoned completely, as it is unclear whether the 4 μm tunnel length will be sufficient to prevent the neurons from escaping from the neurocage. The new 10 μm tunnel width is tested, on the assumption that the tunnels were too narrow to allow the neurons to extend out and sense their neighbors. The same fabrication process is used for each of the different combinations of tunnel lengths and widths. The chimneys are still 30 μm diameter. However, the use of soft-baked photoresist for the tunnels and the chimneys necessitates the use of the partial-exposure method (described subsequently) which limits the chimney height to only 4 μm, for a given tunnel height between 1 μm and 2 μm. An outline of the fabrication process is shown in Fig. 3-12. (A detailed fabrication process can be found in Appendix I.)

As in the fabrication process described in Section 3.2.1, this process begins by cleaning the silicon wafer with piranha and HF and then growing a thin layer, 0.5 μm, of thermal oxide.

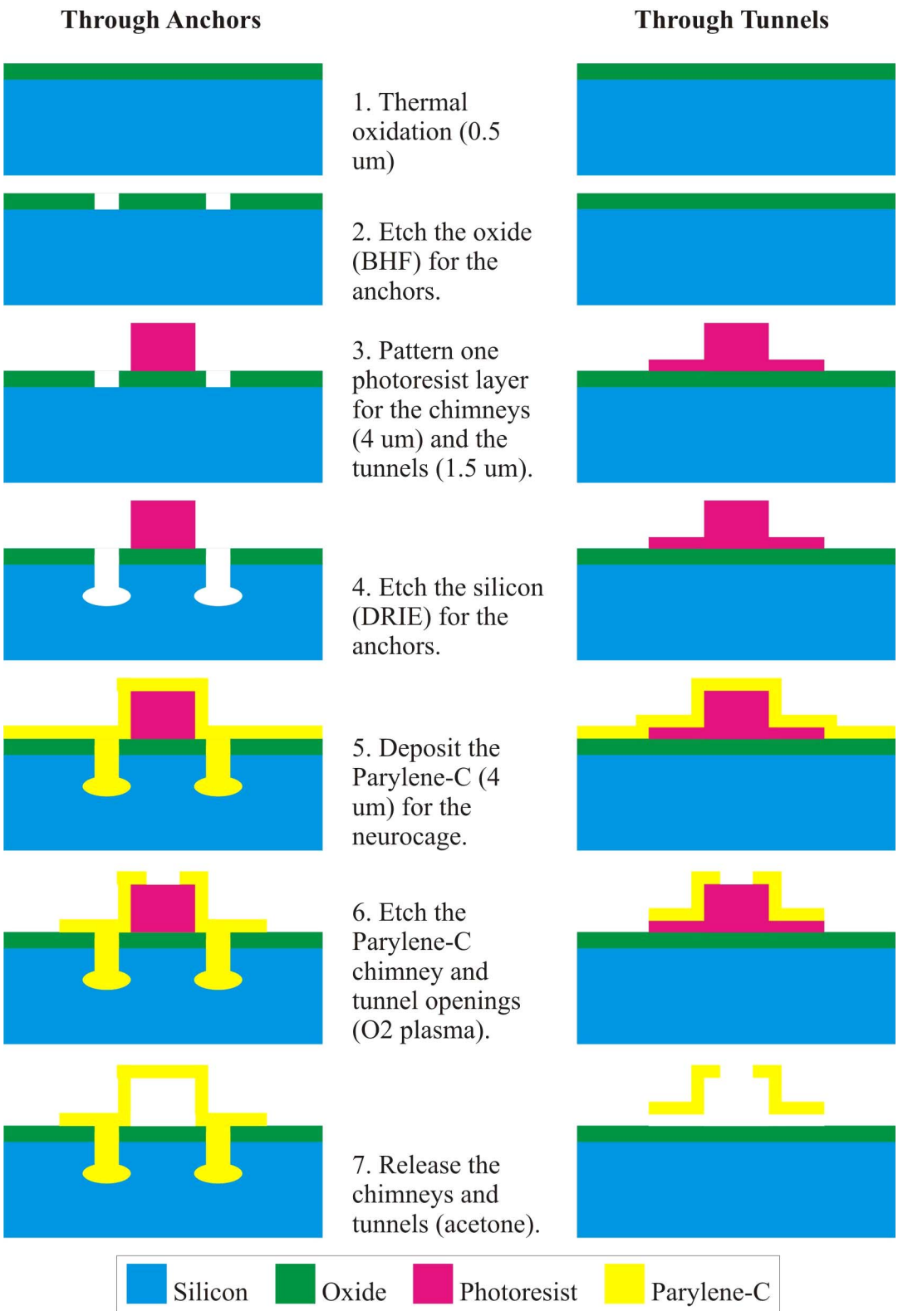


Fig. 3-12. Process flow for the neurocages on silicon with soft-baked photoresist as the sacrificial material for the tunnels and chimneys. (Not drawn to scale.)

To eliminate the problem in the previous process (Section 3.3.1) the anchors in this process are etched in two separate steps. The silicon wafer is first baked at 100°C for 10 minutes and then treated with HMDS for 1 minute. A layer of photoresist, approximately 4 μm thick, is then spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the anchors. The wafer is treated briefly with O_2 plasma to ensure all of the photoresist in the anchor openings has been removed. The anchors are then etched into the oxide using BHF; they are not etched into the silicon at this point. The photoresist is stripped in acetone and the wafer is cleaned in piranha and HF to prepare for the sacrificial photoresist.

After baking the silicon wafer at 100°C for 10 minutes and treating it with HMDS for 1 minute, a single layer of photoresist, approximately 4 μm thick, is spun on and soft-baked at 100°C for 30 minutes. This photoresist layer will form both the tunnels and the chimneys. Using the partial exposure method, the chimneys are not exposed, the tunnels are exposed for half the total exposure time, and the remainder of the chip is exposed for the entire exposure time. Thus, when the photoresist is developed, the chimneys, having not been exposed, will remain their original height of 4.15 μm (± 0.06 μm). The tunnels, being partly exposed, will be partly developed to height of 1.83 μm (± 0.06 μm). The remainder of the chip, being completely exposed, will be completely developed. This will leave only the photoresist comprising the tunnels and chimneys, both having different heights.

The next step in the fabrication process is to etch the silicon for the anchors using the DRIE process outlined in Section 3.1.1. No additional photoresist steps are required for this second anchor etching. The oxide remaining on the chip serves as a mask for the

anchor etching as the DRIE process does not etch oxide significantly. The photoresist for the tunnels and the chimneys, however, is minimally etched during the DRIE process. After the DRIE etching, the resulting chimney height was 3.80 μm (± 0.05 μm), for a height loss of 0.35 μm (8.34%), and the resulting tunnel height was 1.47 μm (± 0.07 μm), for a height loss of 0.36 μm (20.48%). The resulting tunnel and chimney heights are still within the design specifications.

A single layer of Parylene-C, approximately 4 μm thick, is then deposited to form the neurocage. A single layer of photoresist, 15 μm thick, is spun on and soft-baked at 90°C for 40 minutes. The openings for the tunnels and chimneys are then exposed and developed. O_2 plasma is then used to etch the Parylene-C to form the final neurocage. Once the etching is complete, the sacrificial photoresist for the tunnels and chimneys is removed in acetone. Finally, the resulting chips are cleaned in piranha and HF to prepare them for culturing. Optical images and SEMs of the final neurocages are shown in Figs. 3-13, 3-14, and 3-15. As can be seen in the SEMs in Fig. 3-14, the shorter tunnels allow the entire length of the tunnel to be visualized, ensuring the sacrificial material has been completely removed.

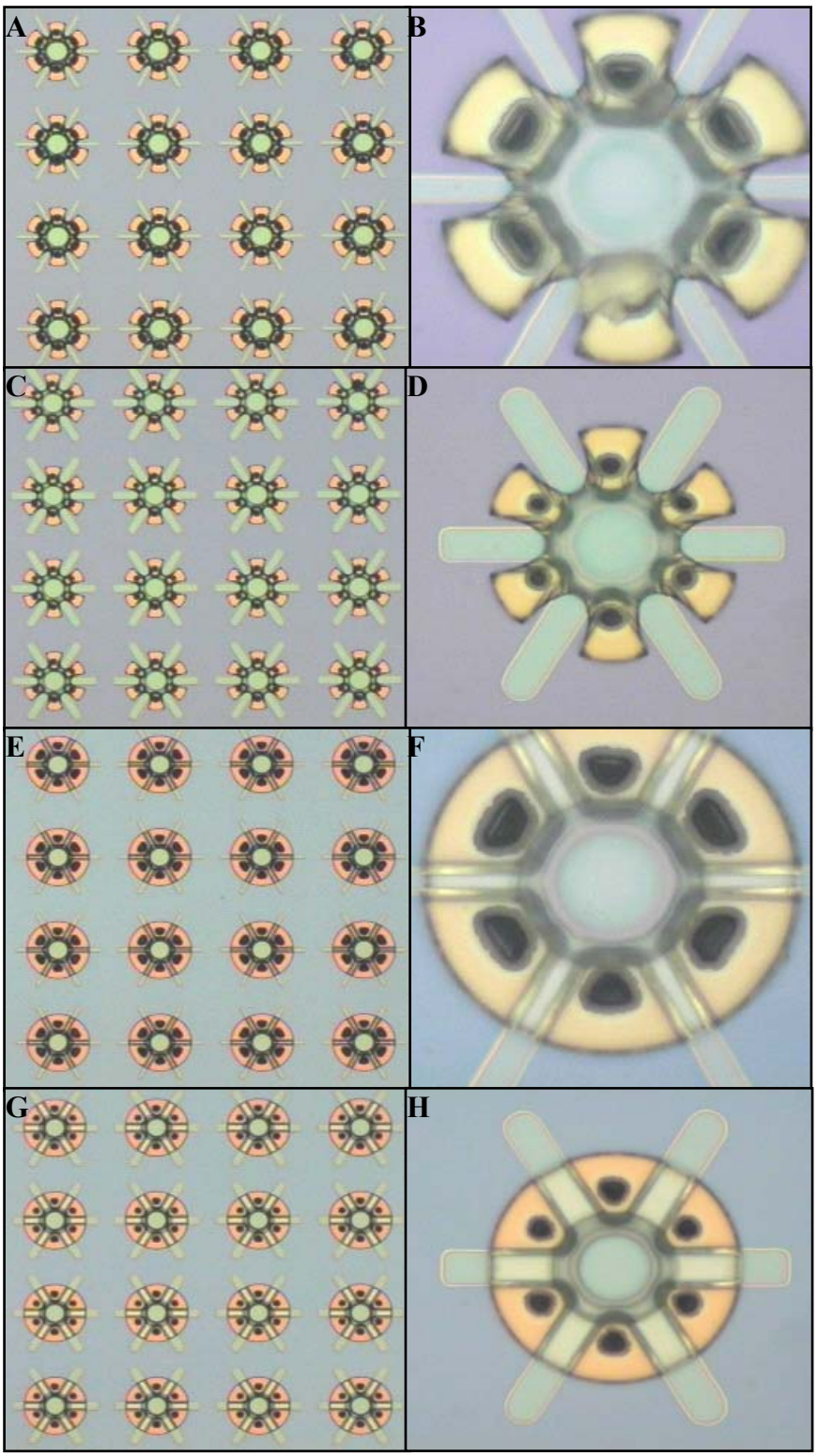


Fig. 3-13. Optical images of neurocage arrays (**A, C, E,** and **G**) and individual neurocages (**B, D, F,** and **H**) with soft-baked photoresist tunnels and chimneys. **A-D** show neurocages with 4 μm tunnel lengths. **E-H** show neurocages with 25 μm tunnel lengths. **A-B** and **E-F** show neurocages with 5 μm tunnel widths. **C-D** and **G-H** show neurocages with 10 μm tunnel widths.

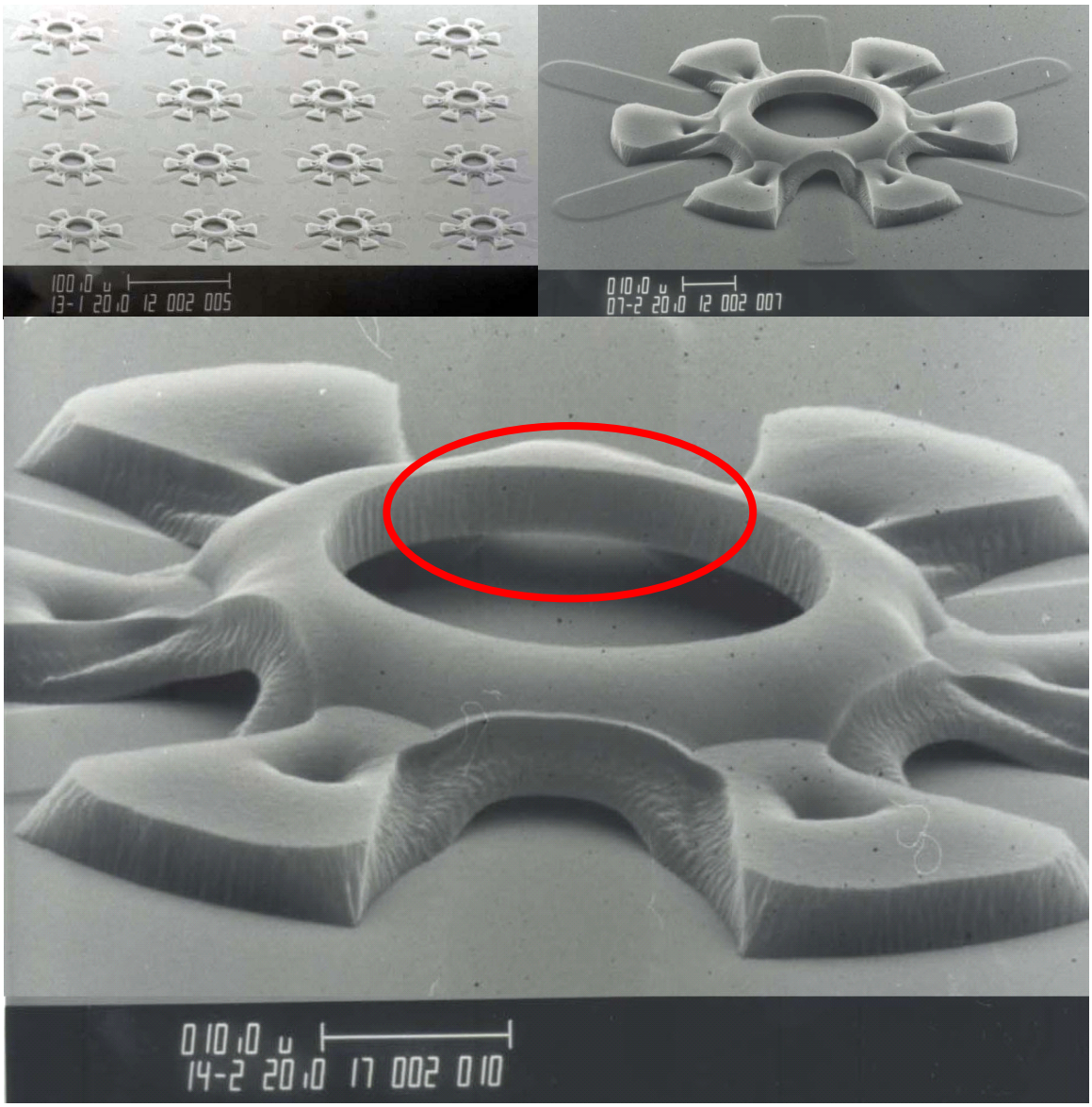


Fig. 3-14. SEMs of neurocages with soft-baked photoresist tunnels and chimneys. The tunnels are 4 µm long and 10 µm wide. The short tunnel length enables visualization of the entire tunnel length. The tunnel circled in red is clearly open.

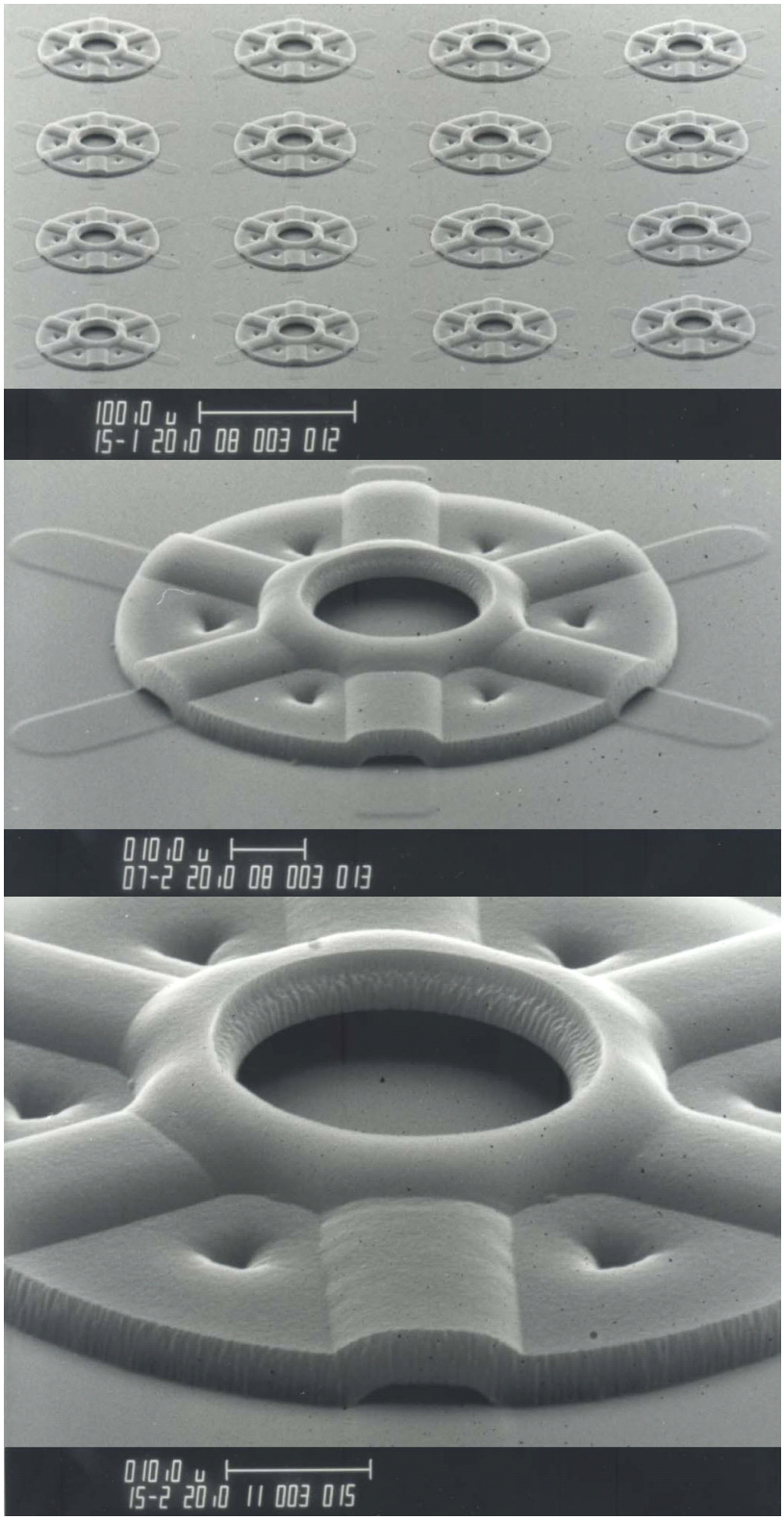


Fig. 3-15. SEMs of neurocages with soft-baked photoresist tunnels and chimneys. The tunnels are 25 µm long and 10 µm wide.

3.4.2 Culturing Results

These neurocages were cultured using the same procedure described in Section 3.2.2. Nomarski images of these cultured neurons are shown in Fig. 3-16. The neurons are clearly visible in the neurocages, extending neurites out through the tunnels to form synaptic connections with their neighbors. In addition, due to the transparency of the Parylene-C, it is possible to see the neurites when they are in the tunnels.

The survival rate for neurons in these neurocages is very good, nearly 50% after 2 weeks (Fig. 3-17). This survival rate includes neurons grown in all four kinds of neurocages. No significant differences in neuronal survival rate were seen among the various combinations of tunnel length and width. If only the initially viable neurons are considered (i.e., those neurons that were alive at day 3), the survival rate increases to nearly 90% after 2 weeks. Most importantly, however, the neurons remained in the neurocages and did not escape through either the tunnels or the chimney.

These neurocages are incredibly robust and can be reused for multiple experiments. The neurocages can withstand a variety of chemicals, including acetone, piranha, and HF, as well as ultrasonic agitation, with no visible delamination or deformation. In addition, the neurocages can survive for long periods, up to 81 days, in saline at 37°C, again with no visible delamination or deformation. (The study was concluded after 81 days, so no data is available for longer periods.) Once the neurons have died, the neurocages can be cleaned of the remaining cellular debris (Fig. 3-18) and used in subsequent culturing experiments.

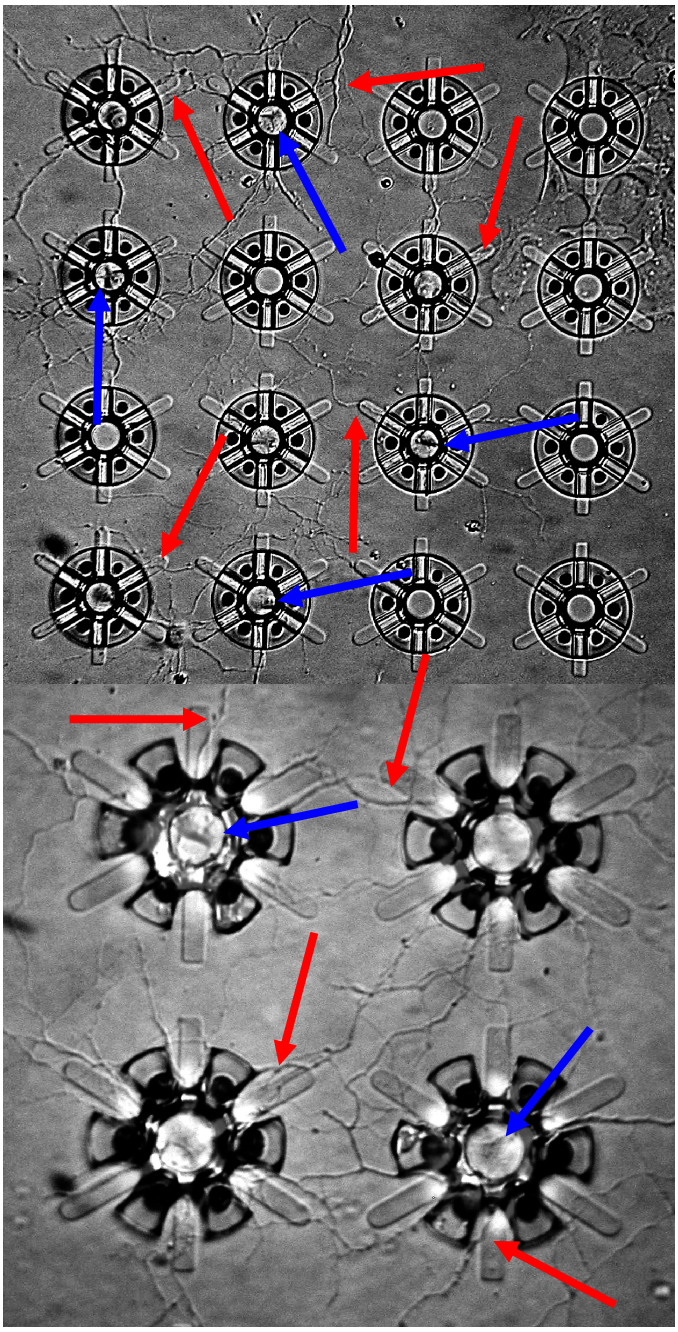


Fig. 3-16. Nomarksi images of growing neuronal cultures. The top image shows a growing culture in a 4 x 4 array of neurocages with 25 µm long and 10 µm wide tunnels. The bottom image shows a growing culture in neurocages with 4 µm long and 10 µm wide tunnels. The blue arrows indicate some of the neurons inside the neurocages. The red arrows indicate some of the neurites extending out of the tunnels to form synaptic connections with neighboring neurons.

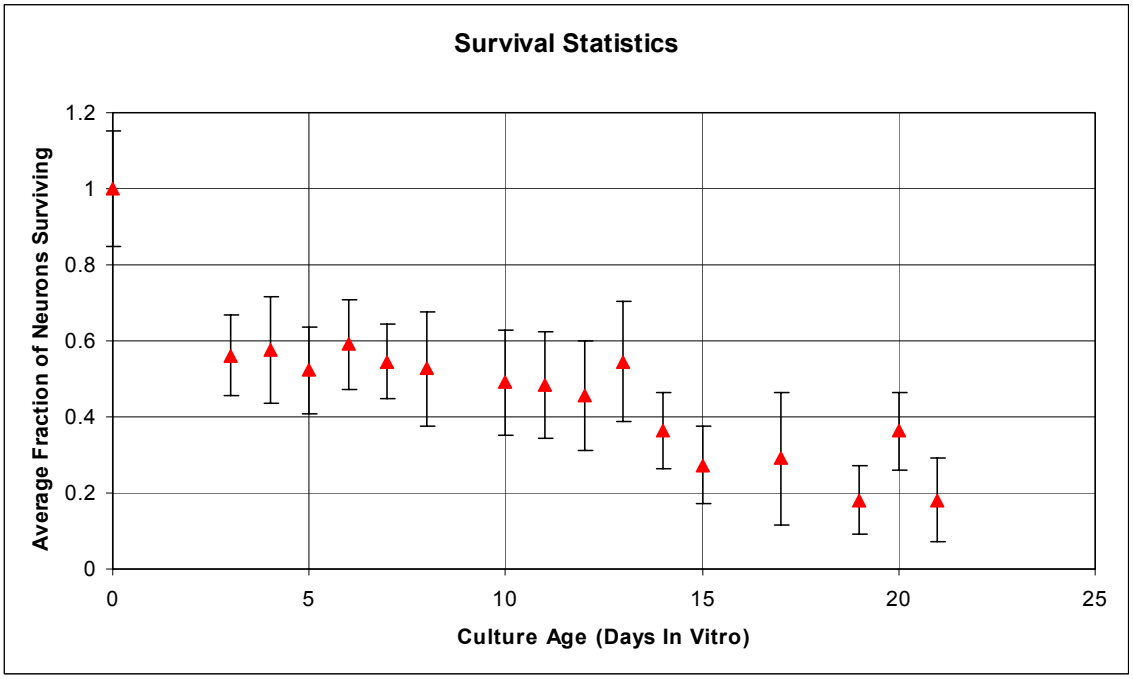


Fig. 3-17. Survival statistics for neurons in neurocages (includes neurocages with both 4 µm and 25 µm long and 5 µm and 10 µm wide tunnels). After 2 weeks, approximately 50% of the neurons survive. If only initially viable neurons are considered (neurons alive after 3 days), the survival rate at 2 weeks increases to approximately 90%.

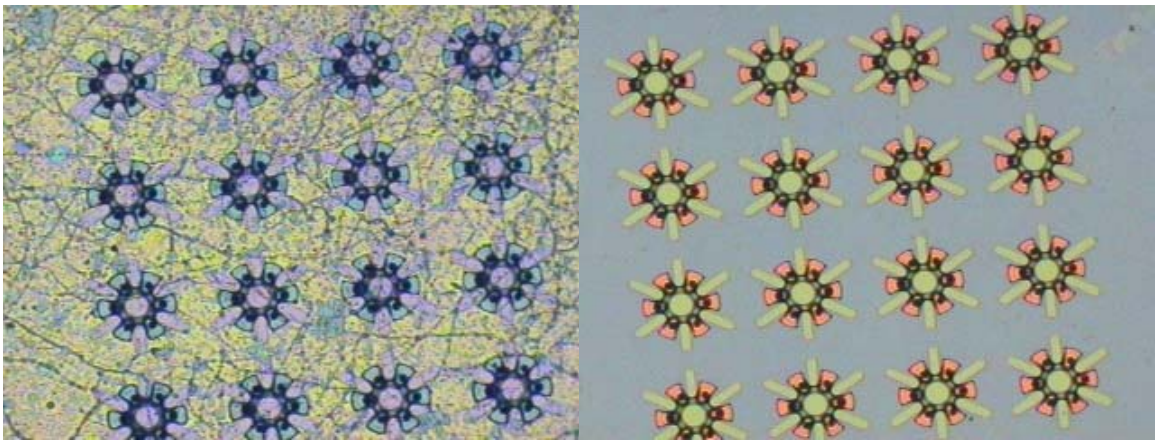


Fig. 3-18. Optical images of a previously cultured array of neurocages (left) and the same array of neurocages after cleaning in piranha and HF (right). As can be seen, the neurocages can be cleaned of all debris and reused.

3.5 Future Work

The final fabrication process, outlined in Section 3.4, created neurocages with a high neuronal survival rate, even after 2 weeks. It is not clear, however, whether these results are attributable to the modified fabrication process with soft-baked photoresist in the tunnels and chimneys to ensure the sacrificial material is completely removed, or to the change in geometry, reducing the chimney height from 15µm to 4µm. Further tests should be completed to determine which change, the sacrificial material or the geometry, led to the increased neuronal survival rate. In addition, although a neuronal survival rate of 50% after two weeks is acceptable, a higher survival rate would be more advantageous. It is possible that further refinements in the geometry of the neurocage would lead to increased neuronal survival. Nevertheless, with the successful completion of these neurocages, electrodes can now be incorporated so that the neurons can be stimulated and action potentials recorded.

CHAPTER 4
Neurocages on Silicon with Electrodes

With the successful completion of the neurocages on silicon, the next step is to incorporate the electrodes, to allow the neurons to be stimulated and recorded from. Each neurocage will have its own electrode at the bottom of the chimney. The material for the electrodes is comprised of two metal layers: chrome and gold. The chrome is a very thin layer that is used solely as an adhesion layer between the gold and the oxide.

4.1 Insulation Materials

A variety of different materials can be used as the insulator for the electrodes: silicon-oxide, silicon-nitride, or polymers, such as Parylene-C. Table 4-1 lists the dielectric constants of these various materials. As can be seen, they have similar dielectric constants, indicating they will behave similarly as insulators. The primary advantage of Parylene-C, and the reason it was chosen for the neurocages, as opposed to oxide or nitride, is that its deposition is done at room temperature. In addition, Parylene-C has a long history as an insulator for electrodes in biological applications [31–36]. Although Parylene-C was the primary insulator, some later fabrication was also done with low-stress silicon-nitride insulation. Low-stress silicon-nitride is an alternative to standard silicon-nitride, as standard silicon-nitride can be a high-stress material and is

prone to cracking. However, the Parylene-C and the low-stress silicon-nitride were nearly indistinguishable from one another with regard to action potential detection and neuronal survival rate.

	Silicon-Oxide (Thermal)	**Silicon-Nitride (PECVD)**	**Parylene-C**	**Silicones**
Dielectric Constant	3.9 [43]	~ 5 [44]	3.10 [30]	~ 2.6 [30]

Table 4-1. Dielectric constants for some insulating materials

4.2 Parylene-C and the Aluminum Etch Stop

To fabricate the neurocages with electrodes, it was initially believed that the metal for the electrodes could be deposited, followed by the Parylene-C for the insulation. Once openings for the electrodes were etched in the Parylene-C with O_2 plasma, the neurocages could be fabricated on top using the same process outlined in Section 3.4.1. Unfortunately, this procedure did not result in the desired neurocages, as the SEMs in Fig. 4-1 show. At first glance, the neurocage itself looks promising, however, closer

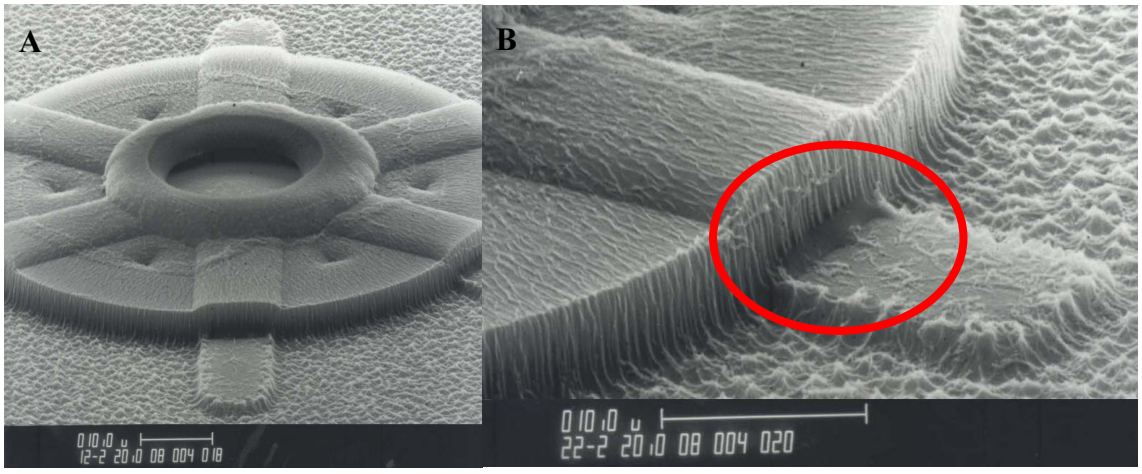


Fig. 4-1. SEMs of neurocages with Parylene-C insulation. Fig. **A** shows the Parylene-C insulation surrounding the neurocage is not smooth, as it has been roughened by the O_2 plasma. Fig. **B** shows the tunnels (circled in red) have not been opened.

inspection reveals two problems: closed tunnels and roughened Parylene-C insulation.

4.2.1 Closed Tunnels

During the fabrication process, the Parylene-C comprising the neurocage itself is deposited directly on top of the Parylene-C forming the insulation layer. As there is nothing between the two layers of Parylene-C, they become, in effect, one single layer (Fig. 4-2). Thus, to open the tunnels it is necessary to etch down through this now single layer of Parylene-C. The question is: how much etching is required (Fig. 4-3)? If too much Parylene-C is etched the tunnels will definitely be open, although the Parylene-C remaining as the insulation for the electrodes will be too thin or have holes (caused by the same O_2 plasma that opened the tunnels) (Fig. 4-3A). On the other hand, if not enough Parylene-C is etched then there will be enough Parylene-C remaining to act as a good insulator for the electrodes but, unfortunately, then the tunnels will not be open (Fig. 4-3B). Therefore, in order to open the tunnels, without compromising the insulation, the

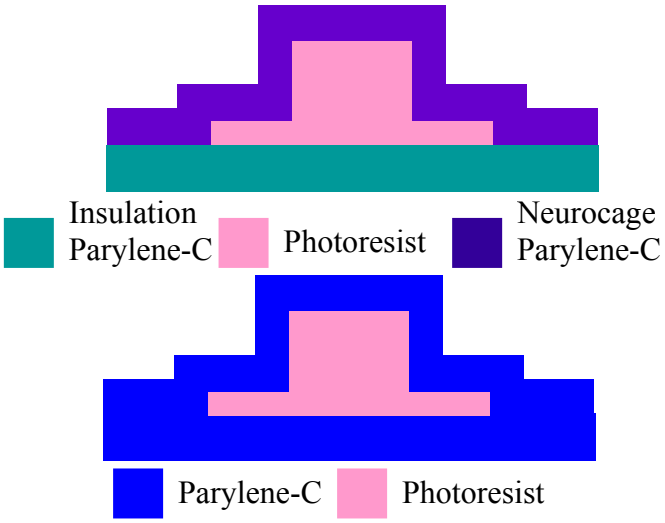
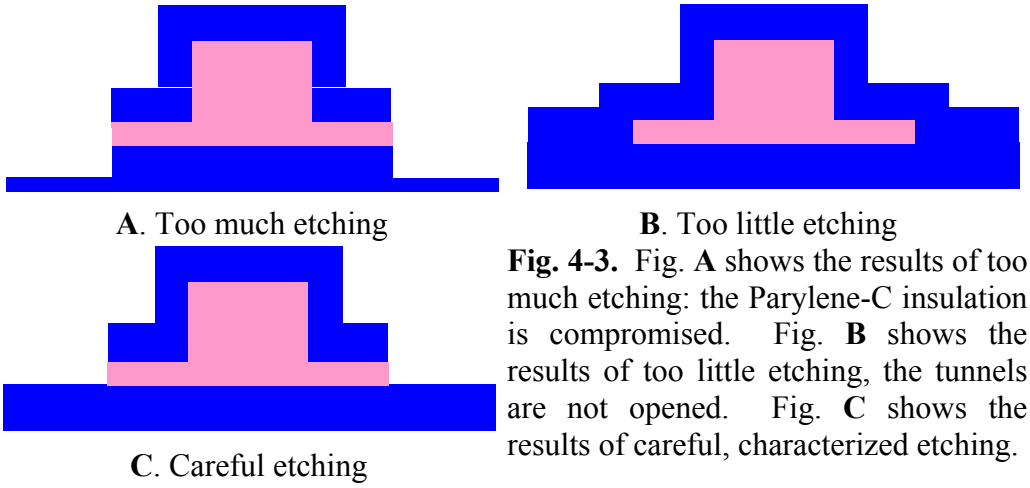


Fig. 4-2. The top image shows the neurocage Parylene-C deposited on top of the insulation Parylene-C. With nothing separating the two Parylene-C layers, they become in effect, one layer.



A. Too much etching

B. Too little etching

C. Careful etching

Fig. 4-3. Fig. **A** shows the results of too much etching: the Parylene-C insulation is compromised. Fig. **B** shows the results of too little etching, the tunnels are not opened. Fig. **C** shows the results of careful, characterized etching.

two Parylene-C deposition steps, for the insulation and the neurocage, must have documented thicknesses and the Parylene-C etch rate must also be well-known and controllable. Knowing these two fabrication parameters, it is possible to etch through the single layer of Parylene-C sufficiently to open the tunnels, without removing too much of the insulation (Fig. 4-3C).

4.2.2 Roughened Parylene-C Insulation

The second problem is the roughened Parylene-C insulation. As-deposited Parylene-C is quite smooth; it is the O_2 plasma used to etch open the tunnels and the chimneys, that roughens the surface as it etches. As mentioned previously, when the Parylene-C for the neurocage is deposited, it forms a single layer with the Parylene-C insulation. Thus, it is impossible to etch the neurocage Parylene-C without the O_2 plasma also coming in contact with, and roughening, the insulation Parylene-C. The result is a very rough surface, as shown in Fig. 4-1.

Assuming that the enough of the Parylene-C insulation remains after the tunnels are etched open and there are no holes in the insulation layer (i.e., the Parylene-C has not

been over-etched), this roughness will not affect the insulation properties of the Parylene-C. However, it greatly impedes the visualization of the neurites as they grow out of the tunnels (Fig. 4-4). As this Nomarski image shows, the neurons in the neurocages can be seen, as well as the processes in the tunnels; once the processes have grown out of the tunnels, though, they are no longer visible.

It is impossible to etch the neurocage Parylene-C without the insulation also coming in contact with the O_2 plasma and, thus, roughening the insulation. Unlike the previous problem, the closed tunnels, this problem cannot be solved by careful etching of the Parylene-C.

4.2.3 Aluminum Etch Stop

Fortunately, both of these problems can be solved through the use of an etch stop layer. This etch stop is a material deposited on top of the Parylene-C insulation, prior to fabricating the neurocage, which serves to keep the Parylene-C insulation and neurocage layers separate. If the etch stop is not affected by the O_2 plasma used to etch the

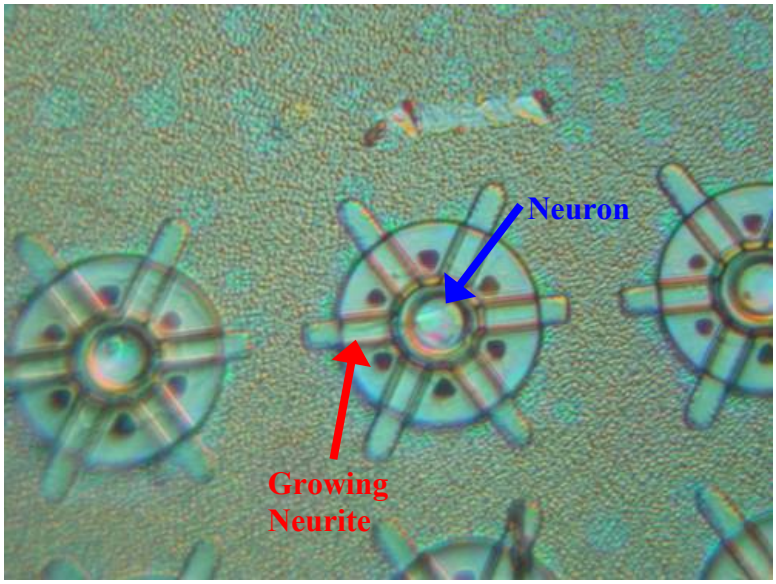


Fig. 4-4. This is a Nomarski image of a growing neuron. The neuron inside the neurocage is visible, as is the neurite inside the tunnel. However, due to the roughened Parylene-C insulation, once the neurite extends beyond the neurocage it cannot be visualized.

neurocage Parylene-C it will remain intact and, thus, prevent the Parylene-C insulation from coming in contact with the O_2 plasma. This will ensure the tunnels are completely etched open while protecting the insulation from being roughened, allowing the growing neurons to be easily visualized.

A variety of different materials could be used for the etch stop layer, provided they are impervious to O_2 plasma. Some possible materials are silicon, silicon-oxide, silicon-nitride, or metals. Aluminum was chosen because it is inexpensive and very easy to deposit and subsequently remove.

4.3 Moats, Curtains, and Melted Chimneys

4.3.1 Moats

Original designs called for the aluminum etch stop layer to cover the insulation Parylene-C, without extending underneath the neurocages. It was believed that if the aluminum extended too far underneath the edges of the neurocage, it could cause the neurocage to lift off the surface. Then, once the etching is complete, the aluminum etch stop layer is removed. Unfortunately, this illuminated yet another problem: the Parylene-C on top of the aluminum etches significantly slower than the Parylene-C on top of the oxide. Hence, in the time required to remove the Parylene-C covering the aluminum etch stop layer, the insulation Parylene-C in areas where there is no aluminum protecting it has already been etched. Since the aluminum does not extend underneath the neurocages, this created moats around the neurocages (Fig. 4-5). This can cause the electrode, as it leads into the neurocage, to be exposed. Obviously, extending the aluminum etch stop

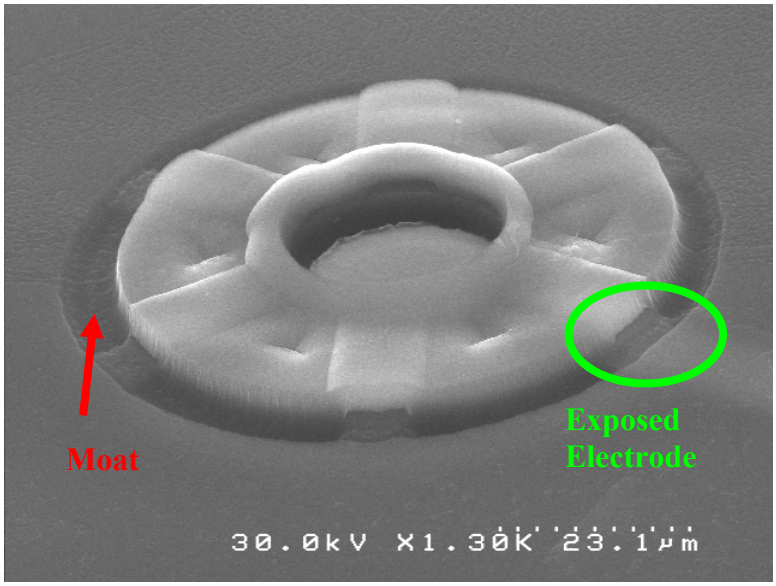


Fig. 4-5. SEM of a neurocage fabricated with an aluminum etch stop layer. As the aluminum etch stop layer did not extend underneath the neurocage, and Parylene-C on aluminum etches slower than Parylene-C on oxide, a moat is created around the neurocage, which can expose the electrode.

underneath the edge of the neurocage will eliminate the moats, and if it does not extend too far underneath the neurocage, the removal of the aluminum etch stop should not cause severe lifting of the neurocage from the surface. However, extending the aluminum etch stop created two additional problems: curtains and melted chimneys.

4.3.2 Curtains

The curtains appear on both the tunnel and chimney openings (Fig. 4-6). These curtains are actually very thin Parylene-C membranes that result from the longer etching time required by the presence of the aluminum etch stop layer. With the increased etching time, the top surface of the Parylene-C becomes very hot and begins to reflow as the etching continues. Towards the end of the etching, some of the sacrificial soft-baked photoresist comprising the tunnels and chimneys begins to be etched by the O_2 plasma. The Parylene-C then flows downward creating very thin membranes that block the tunnel and chimney openings.

Attempts were made to prevent the formation of these curtains. By etching with lower-powered O_2 plasma and separating the total etching time into smaller periods, we hoped to minimize the total heating of the Parylene-C and prevent it from reflowing. These methods, however, were not completely effective and the curtains still formed.

As seen on the SEMs (Fig. 4-6), the curtains appear to be very thin and fragile. Since their formation could not be prevented, a variety of different chemical and mechanical methods were tested to remove the curtains once etching was complete.

The chemical methods tried were RCA1, Aluminum Etchant Type A, Piranha, dichlorobenzene, and chromic acid. RCA1, a combination of ammonium hydroxide and hydrogen peroxide, after 60 minutes at room temperature did not remove the curtains. Likewise, Aluminum Etchant, a combination of nitric, acetic, and phosphoric acids, after 30 minutes at 60°C resulted in no change. Piranha heated to 110°C for 10 minutes

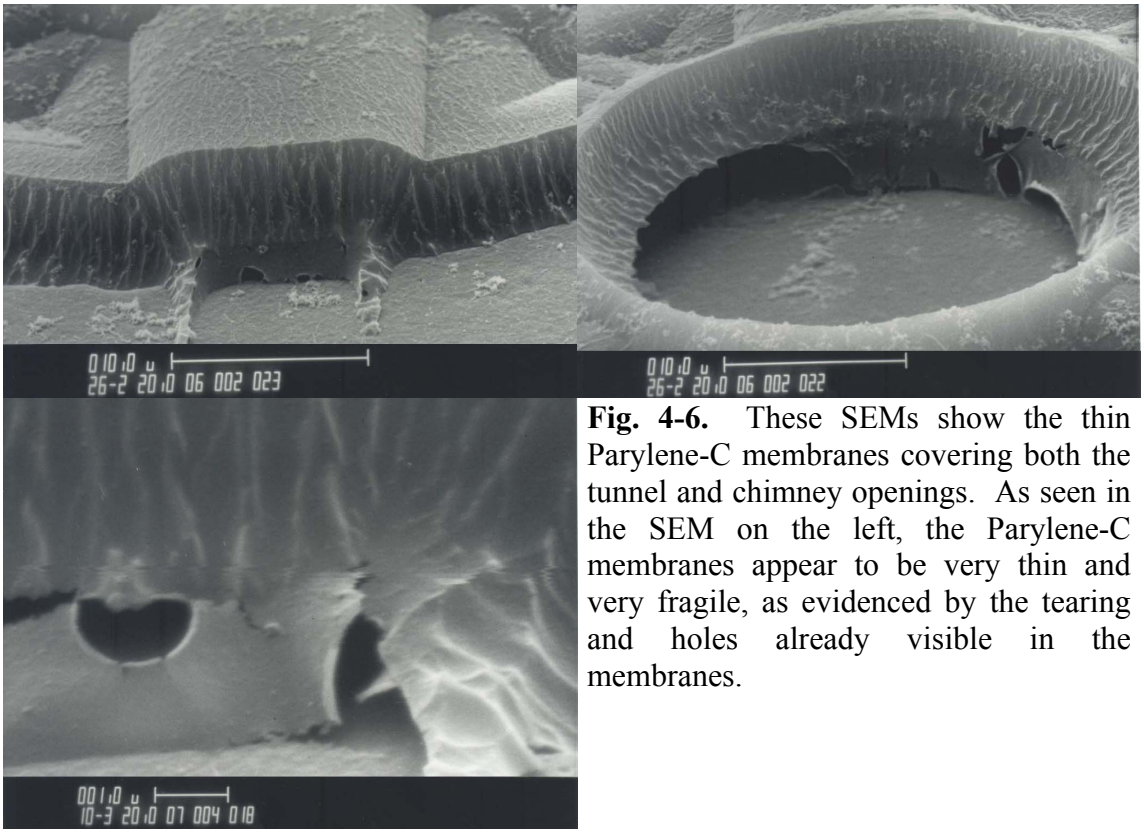


Fig. 4-6. These SEMs show the thin Parylene-C membranes covering both the tunnel and chimney openings. As seen in the SEM on the left, the Parylene-C membranes appear to be very thin and very fragile, as evidenced by the tearing and holes already visible in the membranes.

removed the entire neurocage from the surface. Dichlorobenzene, one of the few chemicals capable of dissolving Parylene-C, did remove the curtains for short exposure times (less than 30 minutes). Unfortunately, the neurocages also started lifting off the surface (Fig. 4-7). Longer exposure times caused the neurocages to be removed completely from the surface. Chromic acid was also successful in removing the curtains, without also removing the neurocages (Fig. 4-8).

The two mechanical methods tested for removing the curtains were O_2 plasma and ultrasonic bath in water. A short O_2 plasma treatment also removed the curtains, however, it also roughened the Parylene-C creating a "fuzzy" neurocage (Fig. 4-9). This

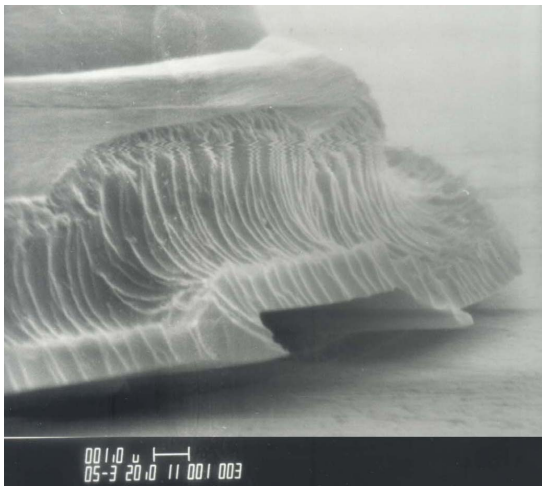


Fig. 4.7. SEM of neurocage treated with dichlorobenzene to remove the curtains on the tunnels and chimneys. This treatment successfully removed the curtains for 15 and 30 minute exposures. The dichlorobenzene, however, caused the neurocages to lift-off the surface. For 60 minute exposures, the neurocages were completely removed from the surface.

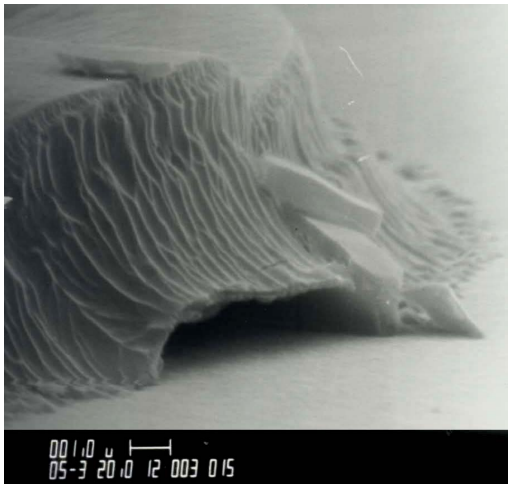


Fig. 4-8. SEM of a neurocage cleaned with chromic acid. The chromic acid was successful in removing the curtains on the tunnels and chimneys.

roughened neurocage will impede the visualization of the neurons inside the neurocage. An ultrasonic bath in water for short periods of time, up to 30 minutes, also removed the curtains (Fig. 4-10). For longer periods, the ultrasonic agitation also removed the neurocages.

Of the methods tested, chromic acid and an ultrasonic bath in water (for short periods of time) were the only ones to successfully remove the curtains without also removing the neurocages. As the ultrasonic bath in water is the simpler method, it was incorporated into the fabrication process as part of the final cleaning step to remove the curtains from the tunnel and chimney openings.

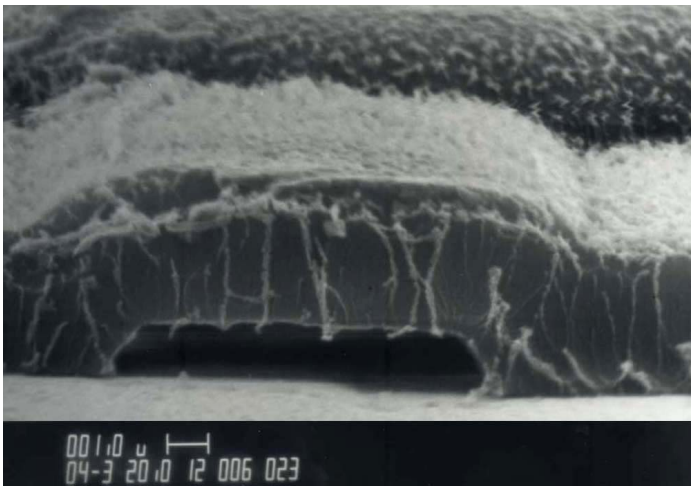


Fig. 4-9. SEM of a neurocage treated with O_2 plasma to remove the curtains on the tunnel and chimney exits. Although the curtains were removed, the O_2 plasma roughened the Parylene-C creating a "fuzzy" neurocage that impeded the visualization of the neurons.

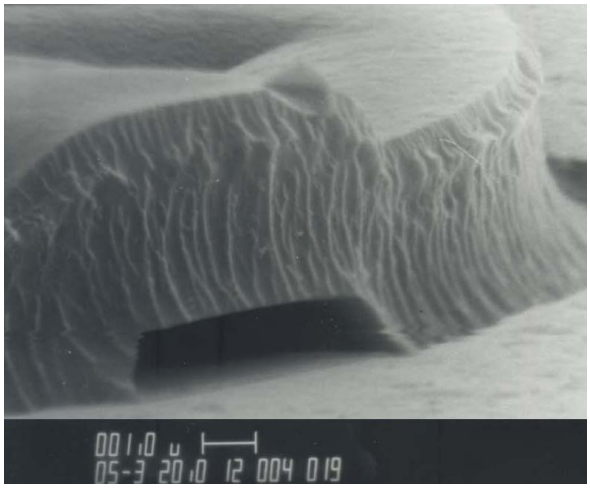


Fig. 4-10. SEM of a neurocage treated with ultrasonic agitation. The ultrasonic bath successfully removed the curtains covering the tunnel and chimney openings.

4.3.3 Melted Chimneys

The melted chimneys were another problem encountered after the introduction of the aluminum etch stop layer. Fig. 4-11 shows the difference between the original chimneys, prior to the introduction of the aluminum etch stop, and the new melted chimneys, created after the aluminum etch stop was added. These melted chimneys exhibit smaller, bowl-shaped openings, with very raggedy edges. Like the curtains, the melted chimneys are a result of the longer etching time required because of the aluminum etch stop. The chimneys, unlike the tunnels, do not have aluminum underneath. Hence, the etching time required to open the chimneys is much less than that required to open the tunnels. Since the chimneys and tunnels are etched as part of a single step, the chimneys are being severely over-etched. This creates the raggedy, bowl-shaped chimneys. The best solution to this problem is to etch the chimneys and the tunnels in two separate steps. Thus, the tunnels can have a longer etch time, without subjecting the chimneys to unnecessary etching.

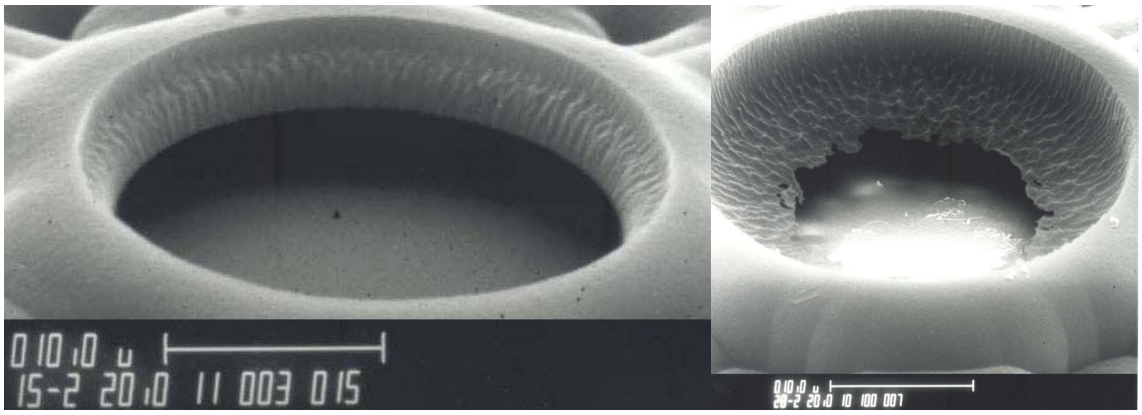


Fig. 4-11. SEM images of the original chimneys (left) and the melted chimneys (right) created after the introduction of the aluminum etch stop.

4.3.4 Resulting Neurocages

Fig. 4-12 shows the neurocages resulting after incorporating these changes into the fabrication process The incorporation of the aluminum etch stop ensures the Parylene-C insulation is not roughened. The separation of the tunnel and chimney etching steps ensures the chimneys are not over-etched and have clean openings. Finally, cleaning the neurocages with an ultrasonic bath in water ensures the curtains on the tunnels and the chimneys are removed.

4.4 Parylene-C Bubbling

Although as mentioned in Section 4.1, Parylene-C is a good insulator, it is necessary that it adhere well to the oxide surface. As can be seen in Fig. 4-13, there are visible Newton rings in the Parylene-C surface, suggesting that the Parylene-C is

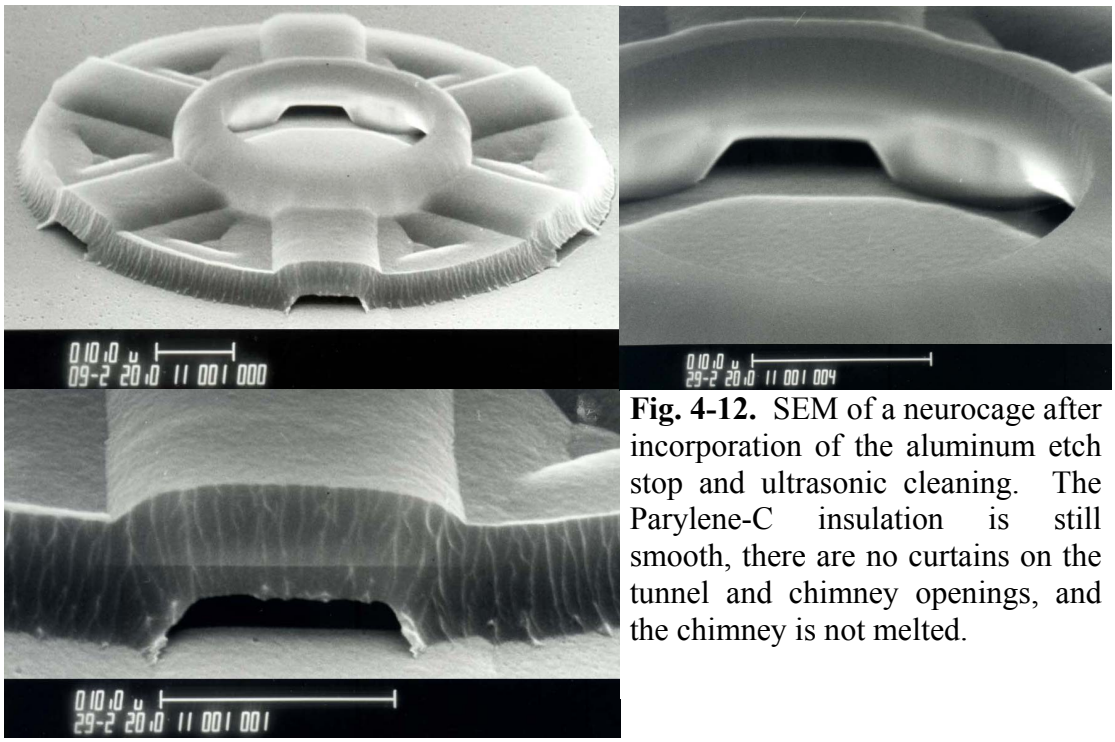


Fig. 4-12. SEM of a neurocage after incorporation of the aluminum etch stop and ultrasonic cleaning. The Parylene-C insulation is still smooth, there are no curtains on the tunnel and chimney openings, and the chimney is not melted.

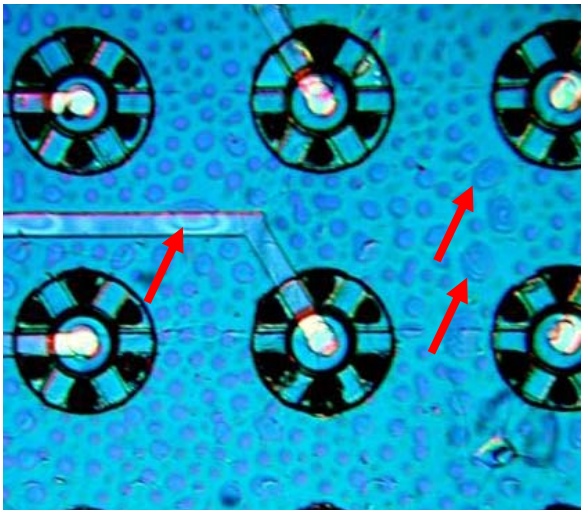


Fig. 4-13. This is a Nomarski image that shows the Newton rings (a few of which are indicated by the red arrows). These Newton rings are evidence that the Parylene-C insulation is delaminating from the oxide surface.

delaminating from the surface. Although the oxide was treated with the A-174 Parylene Adhesion Promoter prior to depositing the Parylene-C insulation, this did not provide the necessary chemical adhesion to ensure the insulation adhered when placed in the neuronal culture media at 37°C.

To improve the adhesion of the Parylene-C, several steps were incorporated into the fabrication process. First, prior to the Parylene-C deposition, the oxide surface was cleaned thoroughly in an ultrasonic bath in acetone, to ensure any potential organic contaminants, as well as any particulates, had been removed. Next, the surface was treated with piranha at 120°C for 5 minutes. This served to both further clean the surface and provide a very hydrophilic surface, through the addition of –OH groups to the top surface of the oxide. Longer treatment in piranha would provide an even more hydrophilic surface; however, the piranha is detrimental to the chrome/gold for the electrodes and with sufficient time, can remove them from the surface completely. The hydrophilic surface is beneficial for the A-174 Parylene Adhesion Promoter, as it ensures a better, and more uniform layer. Thus, after the piranha cleaning, the oxide surface is treated with the A-174 Parylene Adhesion Promoter and the Parylene-C is subsequently

deposited. Studies conducted as part of this process have shown that the combined use of both piranha and A-174 Parylene Adhesion Promoter can dramatically improve the adhesion of the Parylene-C, allowing it to withstand upwards of 200 days in saline at 37°C (as compared to less than 1 day with no treatment).

Finally, the Parylene-C insulation is annealed at 200°C for 48 hours in a vacuum oven. This annealing step enhances the Parylene-C adhesion in several ways. First, the high temperature ensures the A-174 Parylene Adhesion Promoter molecules bind strongly to both the oxide surface and the Parylene-C. Second, the annealing removes any potential contaminants that may have been part of the Parylene-C dimer and deposited in the film. Third, the Parylene-C molecules become cross-linked, forming a denser, less permeable film. Fourth, unlike the A-174 Parylene Adhesion Promoter, the annealing dramatically improves the adhesion of the Parylene-C to the metal electrodes.

The last method used to decrease the delamination of the Parylene-C was to increase the insulation thickness from 2 μm to 4 μm. The thicker Parylene-C ensures a more uniform, pinhole-free film. In addition, the thicker the film, the less likely it is that media can penetrate the entire thickness and reach the oxide-Parylene-C interface and cause delamination of the Parylene-C film.

Combining all of these procedures dramatically improves the adhesion of the Parylene-C and minimizes the delamination from the oxide when placed in culture media at 37°C.

4.5 Anchors

In addition to the methods described in the previous section for improving the chemical adhesion of the Parylene-C insulation to the oxide surface, the insulation is also mechanically anchored to the surface, using the DRIE anchoring process described in Section 3.1.1. Although this will not prevent delamination of the Parylene-C insulation when placed in culture media at 37°C, it does provide significant mechanical adhesion. As the anchors for the Parylene-C insulation extend around the entire edge of the neurochip, forming one long trench, they mechanically lock the Parylene-C to the surface and ensure it is not ripped off during dicing and subsequent cleaning and handling.

During the fabrication process, the anchors for both the insulation and neurocage Parylene-C were etched at the same time (to minimize the number of fabrication steps). However, once the insulation Parylene-C is deposited, the anchors for the neurocage become partially filled with Parylene-C (Fig. 4-14A). Thus, the mushroom cap that is essential for locking the Parylene-C to the substrate is already filled. Hence, when the neurocage Parylene-C is deposited, the anchor is only a vertical hole, rather than the desired inverted mushroom, which is not sufficient to lock the neurocage to the substrate even though the anchor is present. The solution for this problem is to etch the neurocage

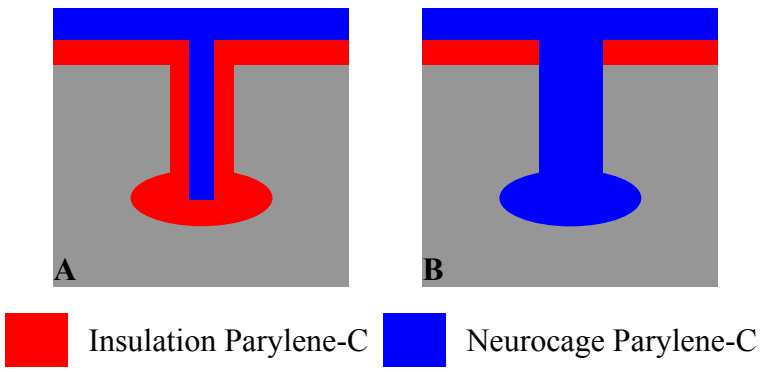


Fig. 4-14. Fig. **A** shows a neurocage anchor pre-filled with the insulation Parylene-C which eliminates the locking structure for the neurocage Parylene-C rendering the anchor useless. Fig. **B** shows the ideal inverted mushroom structure for locking the neurocage Parylene-C to the substrate.

anchors after the insulation Parylene-C has been deposited, ensuring they are not pre-filled with Parylene-C and will still lock the neurocage Parylene-C to the substrate (Fig. 4-14B).

4.6 Neurocage Design

4.6.1 Neuron Escape Rate

Originally, the electrode inside the neurocage was designed to encompass virtually the entire floor of the chimney. The electrodes were 26 µm in diameter, with a 22 µm diameter via. The chimney, for comparison, was 30 µm in diameter. Ultimately, we wanted the neuron to be as close as possible to the electrode to achieve the best possible signal. With this large electrode diameter, the neuron was guaranteed to be in contact with the electrode. Unfortunately, these large electrodes had an unanticipated consequence: neurons escaped through the tunnels out of the neurocage. As seen in Fig. 4-15, the neuron extends its axon out one of the tunnels and then follows that axon, squeezing out of the neurocage. This was a previously unseen phenomenon.

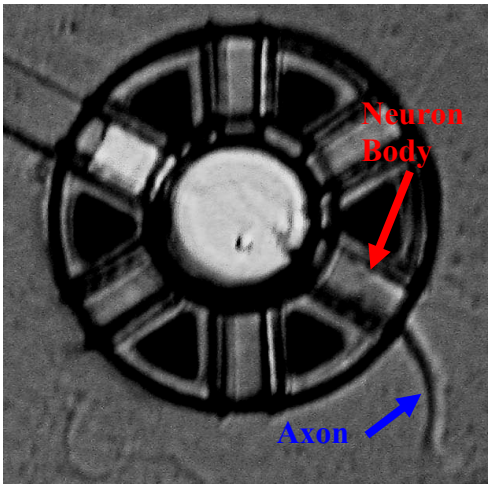


Fig. 4-15. Nomarksi image of a neuron escaping from a neurocage. The neuron extended its axon (indicated by the blue arrow) out through the tunnel and then the neuron body (indicated by the red arrow) followed its axon right out of the neurocage.

Initial studies were done in neurocages with both closed and open electrodes. (The tunnels were 10 μm wide and 25 μm long.) Closed electrodes were ones still covered in the insulation Parylene-C; the via had not been etched. Although rendering them useless for electrical studies, these neurocages provided a useful comparison to the neurocages with open electrodes in studying neuronal escape. As seen in Fig. 4-16, the escape rate in neurocages with open electrodes is nearly twice the escape rate in neurocages with closed electrodes. Although it was unclear what caused the difference in escape rate, an easy solution to minimize the escape rate for all neurocages was to reduce the tunnel height. If the tunnels are small enough, the neurons will be able to extend their processes through the tunnels but will be unable to follow them. Fig. 4-17 shows the escape rate for neurons cultured in tunnels 1.6 μm high and in tunnels 0.7 μm high. As can be seen, reducing the tunnel height in neurocages with closed electrodes reduced the escape rate by nearly 75%. Interestingly, though, there was not a corresponding decrease in the escape rate for neurocages with open electrodes, which exhibited only about a 15% decrease.

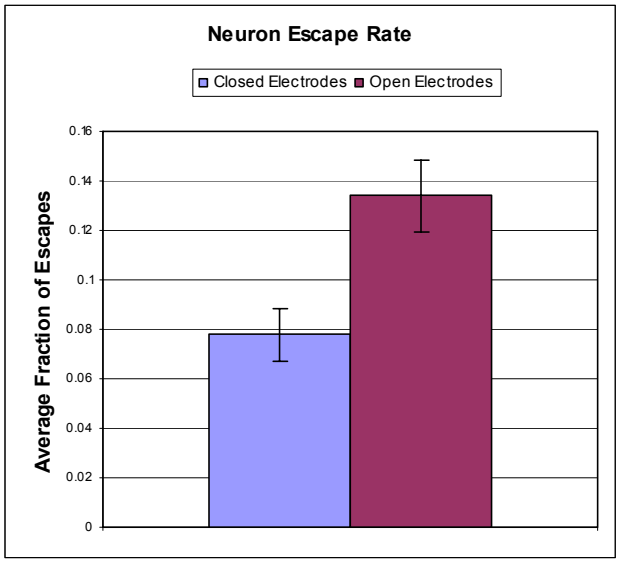


Fig. 4-16. This graph shows the escape rate for neurons in neurocages with both closed (the electrode vias have not been etched open) and open electrodes. The escape rate in neurocages with open electrodes is nearly twice the rate as that in neurocages with closed electrodes.

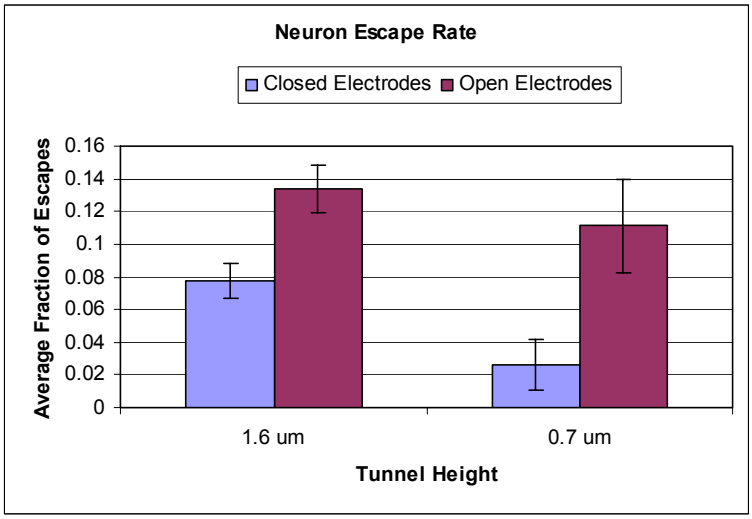


Fig. 4-17. This graph compares the neuronal escape rates for different tunnel heights and electrode configurations. Decreasing the tunnel height does decrease the escape rate for both electrode types. Unfortunately, the decrease is not as significant for the open electrodes and the neuronal escape rate is still high (greater than 10%).

Given this difference in escape rate between neurocages with closed and open electrodes, for both tunnel heights, it seems clear that the open electrodes themselves are affecting the escape rate. The open electrodes are effectively larger craters, 22 µm in diameter, encompassing the entire floor of the neurocage. The electrodes were changed to create a flatter geometry in the floor of the neurocage, like the neurocages with closed electrodes, which as seen in Figs. 4-16 and 4-17, have a lower escape rate. The electrode diameter was reduced from 26 µm to 12 µm and the via was reduced from 22 µm to 10 µm. Thus, the electrode no longer encompasses the entire floor of the neurocage. In addition, the Parylene-C insulation thickness was reduced from 4 µm to 2 µm. Thus, even if the neuron climbs out of this now smaller electrode via, it will see an essentially flat surface, like the closed electrode neurocage, which has a lower escape rate. Fig. 4-18 shows the escape rate for these smaller electrodes. As can be seen, decreasing the electrode via dramatically reduces the neuronal escape rate to less than 1%. Although this data is for a 2 µm Parylene-C insulation thickness, subsequent tests have shown that the increasing the Parylene-C insulation to 4 µm does not significantly change the escape

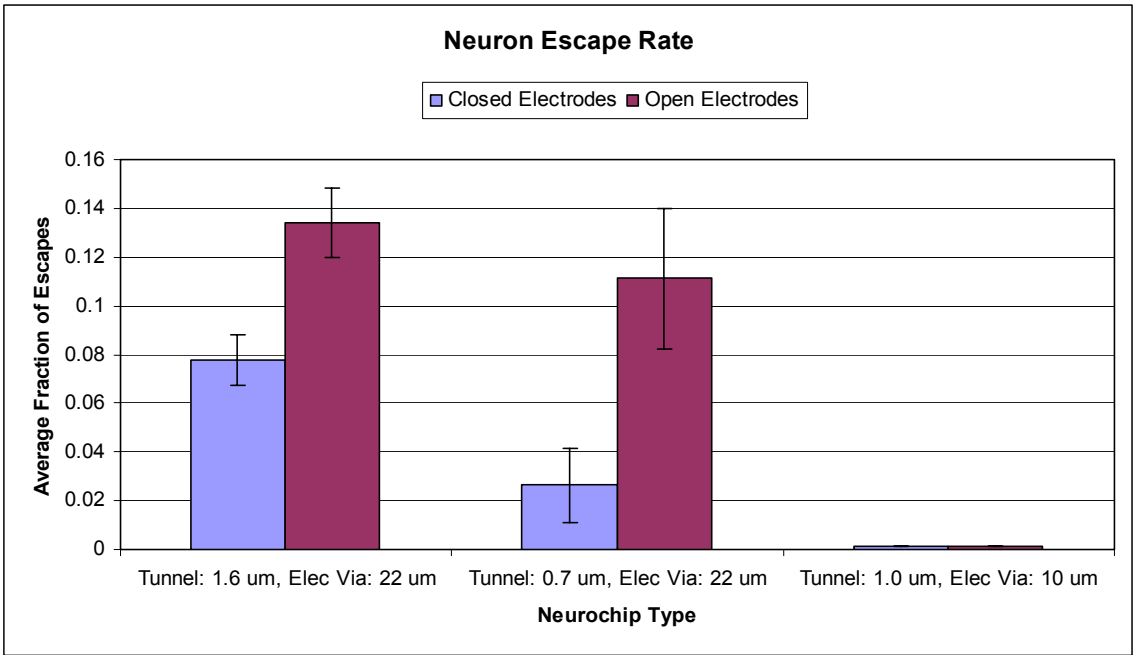


Fig. 4-18. This graph shows the neuronal escape rate for various tunnel heights and electrode configurations. Although modifying the tunnel heights does not produce corresponding changes in the escape rate, reducing the electrode via diameter from 22 µm to 10 µm drastically reduces the escape rate to less than 1% for both the open and closed electrodes.

rate. As this data shows, the primary design feature that affects the neuronal escape rate is the electrode geometry, not the tunnel height as was originally hypothesized.

4.6.2 Tunnel Sacrificial Material

The tunnel sacrificial material chosen for the neurocages on silicon without electrodes was soft-baked photoresist. As shown in Chapter 3, with this material, neural networks were successfully created using caged neurons. Furthermore, the neurons in these neurocages had a survival rate of approximately 50% after 2 weeks. Unfortunately, the partial-exposure method used to make the tunnels and chimneys with the soft-baked photoresist has limited height control. Although very repeatable for some tunnel heights, such as 1.6 µm, the partial-exposure method proved unreliable for shorter tunnels heights,

such as 0.7 μm, often creating neurocages with no tunnels. The previous section demonstrated that the tunnel height was not critical in minimizing the escape rate. However, in fabricating the neurocages with different tunnel heights to test the escape rate, a better method for controlling the tunnel height was needed. Therefore, the tunnel sacrificial material was changed from soft-baked photoresist to aluminum. Simply due to the deposition method, it is much easier to control the thickness of the thermally evaporated aluminum than the spun-on photoresist. In addition, using the soft-baked photoresist for both the tunnels and the chimneys requires the use of the partial-exposure method which links the tunnel and chimney heights, limiting the range of possible heights. Using aluminum for the tunnel sacrificial material and the soft-baked photoresist for the chimney sacrificial material removes this restriction, allowing the tunnel and chimney heights to be changed independently of one another.

Aluminum was tested as the sacrificial material for the tunnels, as described in Section 3.2. Unfortunately, with those neurocages on silicon without electrodes the neuronal survival rate was very low, less than 25% after 5 days. Use of aluminum in these neurocages with electrodes, however, did not result in such low survival rates. It is hypothesized that the concurrent change in chimney heights was responsible for the increased survival rate. No significant increase in neuronal survival was seen in the neurocages without electrodes, regardless of the tunnel sacrificial material, until the chimney height was reduced from 15 μm to 4 μm. This chimney height change was dictated by the use of soft-baked photoresist as the sacrificial material for the tunnels. It was originally believed that the aluminum was not completely removed, hence why the original neurocages with aluminum as the tunnel sacrificial material had a low neuronal

survival rate. At that time, aluminum tunnels with 4 μm high soft-baked photoresist chimneys had not been tested. Neurocages fabricated with electrodes, with aluminum as the tunnel sacrificial material and 4 μm tall chimneys, prove that it was primarily the geometry of the neurocage that caused the low survival rate. These neurocages have a neuronal survival rate similar to that found in neurocages without electrodes with soft-baked photoresist as the sacrificial material for the tunnels and chimneys.

4.6.3 Platinized Electrodes

In order to successfully stimulate and record from the neurons it was necessary to increase the capacitance of the electrodes. This was done by platinizing the electrodes inside the neurocage [45–46]. Using a solution of hydrochloric acid, lead acetate, and chloroplatinic, the gold electrodes were platinized, increasing the capacitance from approximately 40±10 pF to approximately 4000±300 pF. While this allows the neurons to be stimulated and recorded from, the neurons dislike the platinized electrode and always move as far away from the electrode as possible.

4.6.3.1 Chimney Diameter

As the neuron moves from the electrode, it compresses itself against the edge of the neurocage chimney. Thus, although the chimney is cylindrical, with a 30 μm diameter, the actual area in which the neuron lives is the cylindrical annulus around the platinized electrode. This annulus is only 10 μm wide; the inner radius is 5 μm long and the outer radius is 15 μm. Given that the neurons used in these experiments are 10–15 μm in diameter when first loaded and grow to be nearly 25 μm in diameter, this is

potentially too small an area for the neuron to live and grow normally. Therefore, the chimney diameter was increased to 40 μm to provide additional living space for the neuron.

4.6.3.2 Parylene-C Insulation Thickness

The platinization on the electrodes forms a sparse, spiny, bush structure on top of the electrode. This bush fills in the electrode via created by the Parylene-C insulation. Once it has filled in the via, the platinization starts growing out on top of the Parylene-C insulation, expanding out of the electrode via. Obviously, the further beyond the edges of the electrode via that the platinization extends, the smaller the area the neuron has to live. Thus, a balance must be achieved between increasing the platinization, which increases the capacitance and obtains better signal, and decreasing the area over which the platinization extends, to provide more living space for the neuron. One way to do this is to increase the Parylene-C insulation thickness. This will create a deeper electrode via, allowing the electrode to be platinized further before the platinization extends outside the electrode via. Therefore, the Parylene-C insulation thickness was increased from 2 μm to 4 μm.

4.6.3.3 Neurocage Electrode Location and Anchors

As mentioned previously, the presence of the platinized electrode inside the neurocage decreases the effective area in which the neuron can grow. The neuron, to be as far away from the platinization as possible compresses itself against the chimney walls. As the electrode is in the exact center of the chimney, the area in which the neuron

can grow is reduced to an annulus around the electrode. However, the neuron cannot grow and encompass that entire annulus, rather it remains on one side of the annulus, and the effective area available for neuron growth is further reduced. In addition, as the neuron stays on only one side, it tends to extend neurites out of only the 3 or 4 tunnels closest to it, rather than all 6 tunnels, since it will not extend neurites over the platinized electrode and is unlikely to wrap its neurites around the edges of the electrode to access the tunnels on the opposite side. The chimney diameter was increased to accommodate the neuron's dislike for the platinized electrode and to provide additional living space. This provides only a limited increase in effective living space due to the location of the electrode and still does not provide easy access for all 6 tunnels.

One solution to this problem is to move the electrode to the edge of the chimney rather than the center. This would provide a larger effective area inside the chimney for the neuron to grow. In addition, this would ensure that easy access for the neurites is provided to all 6 tunnels. The center of the electrode was thus moved 10 μm from the center of the chimney towards one of the anchors. Placing the electrode in front of the one of the anchors, rather than one of the tunnels, prevents the neuron from perceiving that the tunnel entrance inside the neurocage is "blocked" by the platinized electrode. Thus, direct access to all 6 tunnels is assured. The electrode lead then extends directly out of the neurocage between two adjacent tunnels. The anchor in that location is therefore removed, leaving only 5 anchors for the neurocage, rather than the original 6. Tests have shown that the loss of only 1 anchor does not reduce the robustness of the neurocage structure.

4.6.4 Final Neurocage Design and Electrode Layout

The final neurocage design consists of a chimney, tunnels, and anchors [47–50]. The chimney is 40 μm in diameter and 4 μm high, with a 30 μm diameter opening at the top for loading neurons. There are 6 tunnels, each 10 μm wide and 1 μm high. Two different tunnel lengths were tested: 4 μm and 25 μm. Each neurocage has 5 anchors, trapezoidal in shape with an area approximately 64 μm^2.

The bottom layer of insulation is 0.5 μm of oxide. The top layer of insulation is either 4 μm of Parylene-C or 1 μm of low-stress silicon-nitride. If Parylene-C is the insulation, the anchors for the insulation are 6 μm wide and extend, in a single line, around the entire edge of the chip. The electrodes are comprised of 0.01 μm of chrome and 0.3 μm of gold. The electrode inside the neurocage is 14 μm in diameter with a 10 μm diameter via, offset from the center of the chimney by 10 μm. The electrode lead is 10 μm wide and extends for 3.6–8 mm (depending on the location of the particular neurocage and its corresponding bonding pad). The electrode inside the neurocage extends out between two neighboring tunnels (in the location of the missing anchor) and is connected to a bonding pad at the edge of the neurochip to which an external wire can be wire-bonded to provide the necessary electrical connections. The bonding pads are 500 μm x 500 μm, with a 450 μm x 450 μm via. The electrode layout is shown in Fig. 4-19.

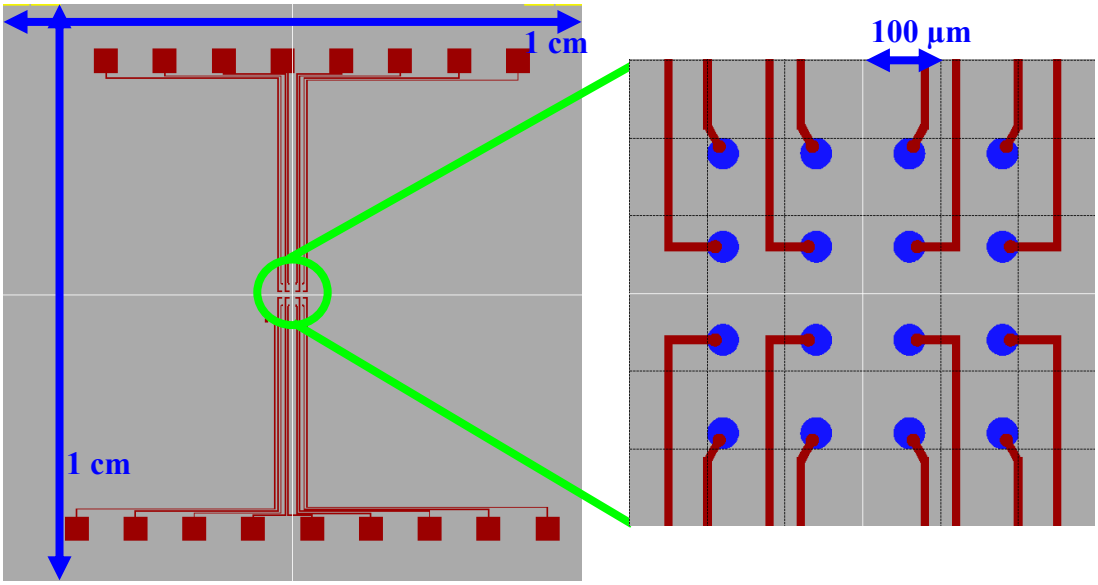
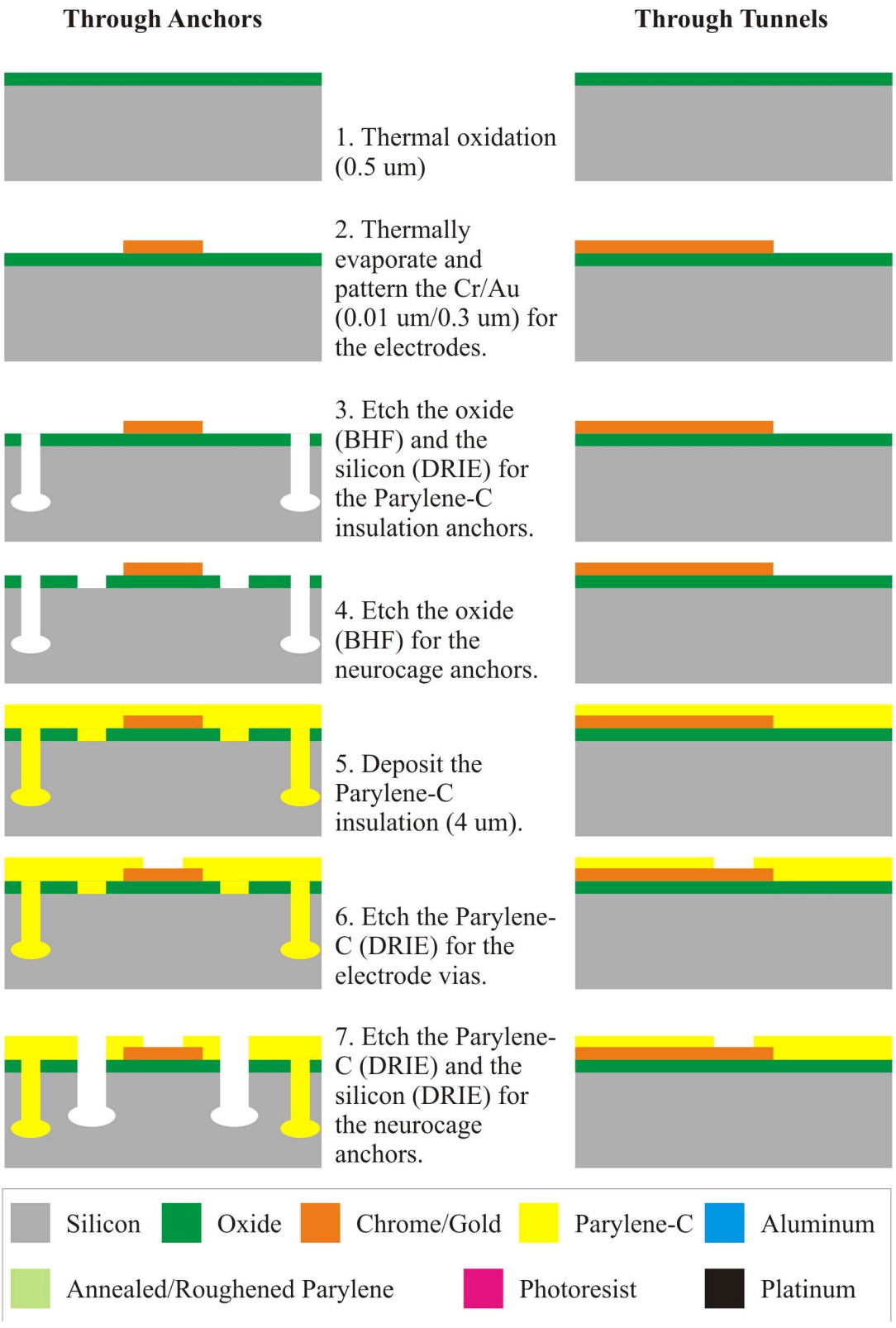
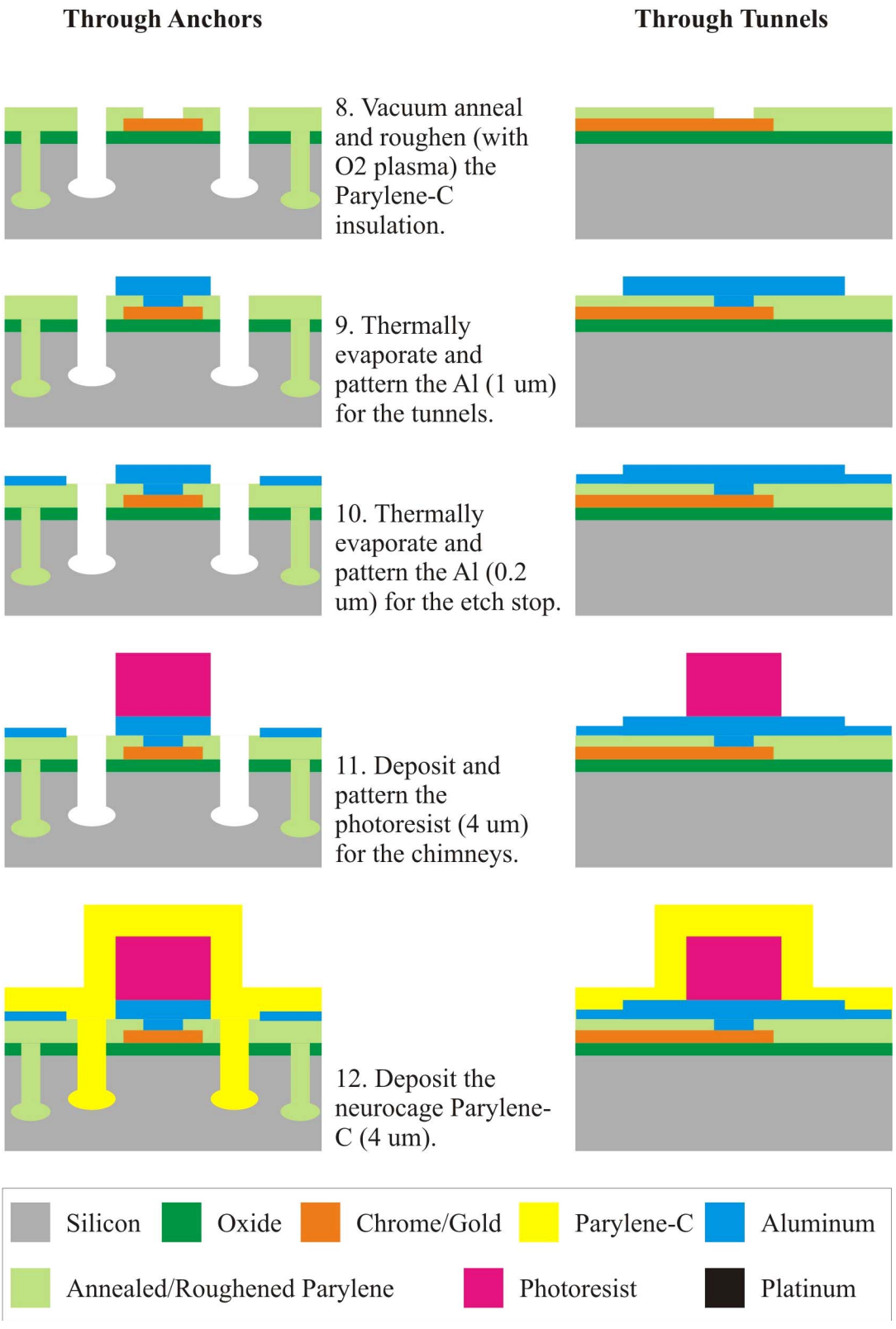


Fig. 4-19. The electrode layout for the neurocages is shown here in red. The right image shows an expanded view of the electrode layout inside the neurocages (the chimney locations are shown in blue). The electrode leads are 10 µm wide and the center of the electrode inside the neurocage is offset by 10 µm from the center of the chimney.

4.7 Fabrication Process

The outline of the fabrication process for the neurocages with Parylene-C insulation is shown in Fig. 4-20 [47–50]. The fabrication process for the neurocages with low-stress silicon-nitride insulation is shown in Fig. 4-21 [48–49]. (Detailed fabrication processes for both Parylene-C and low-stress silicon-nitride insulation can be found in Appendices II and III, respectively.)


Through Anchors
Through Tunnels
1. Thermal oxidation (0.5 um)
2. Thermally evaporate and pattern the Cr/Au (0.01 um/0.3 um) for the electrodes.
3. Etch the oxide (BHF) and the silicon (DRIE) for the Parylene-C insulation anchors.
4. Etch the oxide (BHF) for the neurocage anchors.
5. Deposit the Parylene-C insulation (4 um).
6. Etch the Parylene-C (DRIE) for the electrode vias.
7. Etch the Parylene-C (DRIE) and the silicon (DRIE) for the neurocage anchors.
Silicon
Oxide
Chrome/Gold
Parylene-C
Aluminum
Annealed/Roughened Parylene
Photoresist
Platinum


Through Anchors
Through Tunnels
8. Vacuum anneal and roughen (with O2 plasma) the Parylene-C insulation.
9. Thermally evaporate and pattern the Al (1 um) for the tunnels.
10. Thermally evaporate and pattern the Al (0.2 um) for the etch stop.
11. Deposit and pattern the photoresist (4 um) for the chimneys.
12. Deposit the neurocage Parylene-C (4 um).
Silicon
Oxide
Chrome/Gold
Parylene-C
Aluminum
Annealed/Roughened Parylene
Photoresist
Platinum

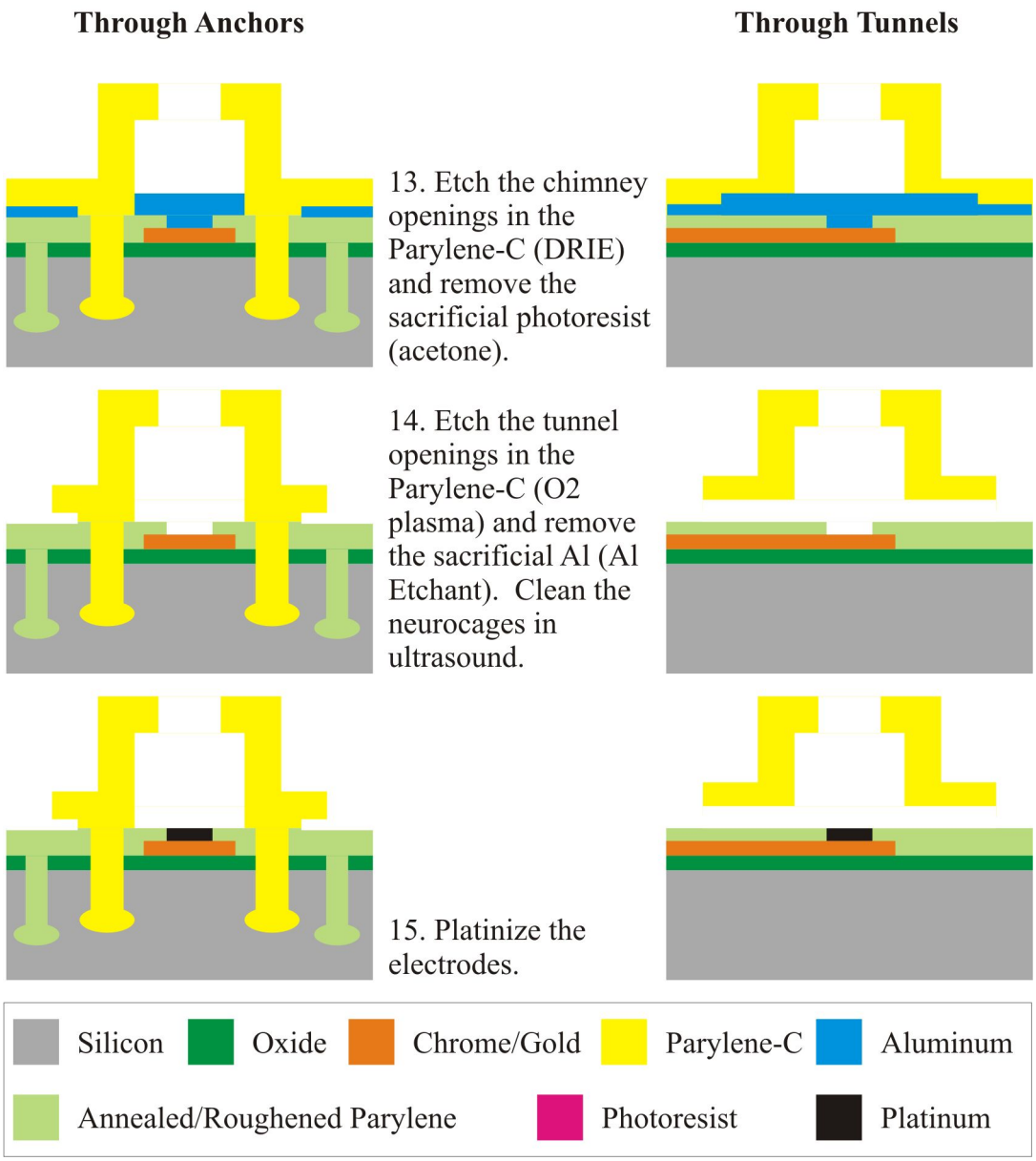
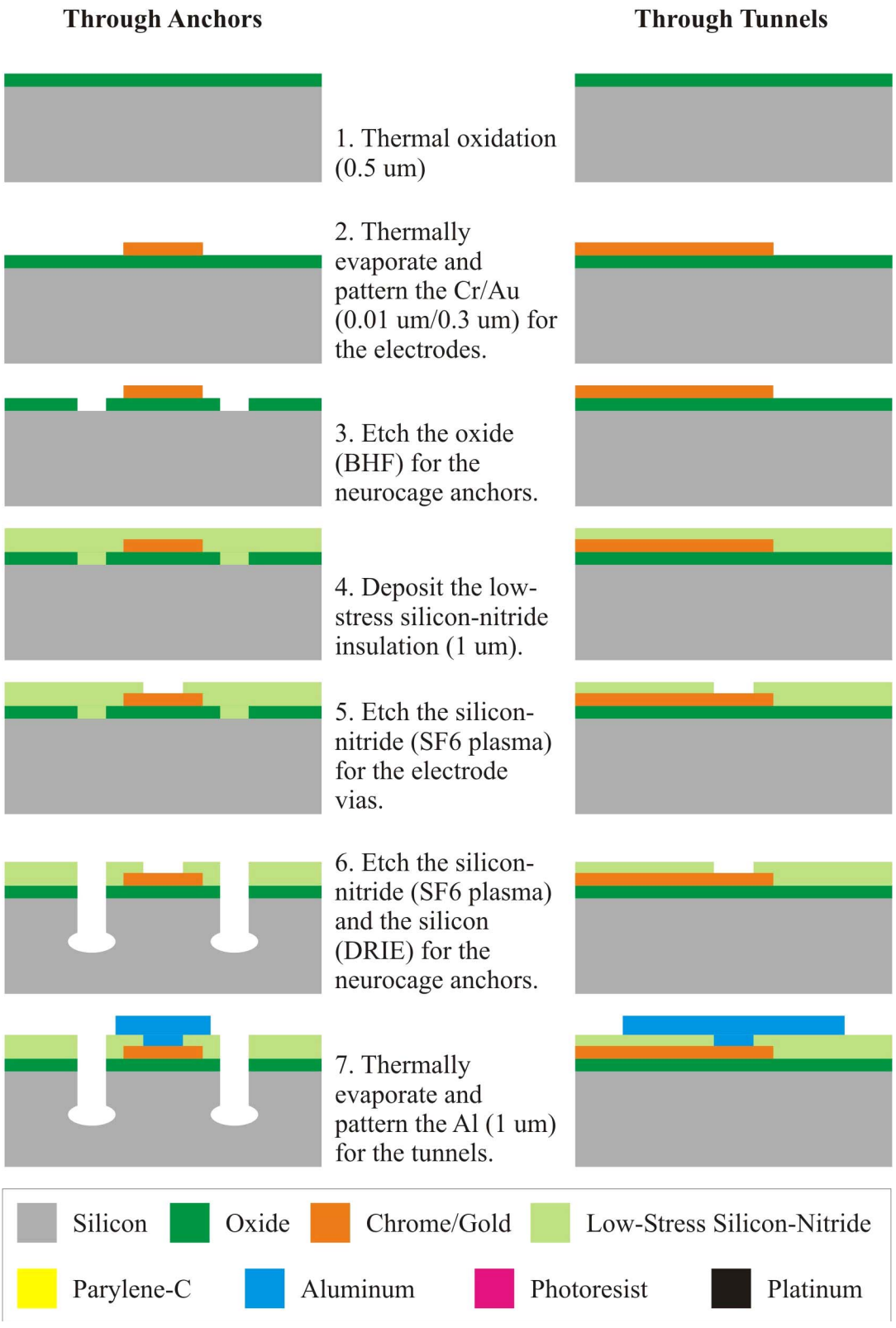
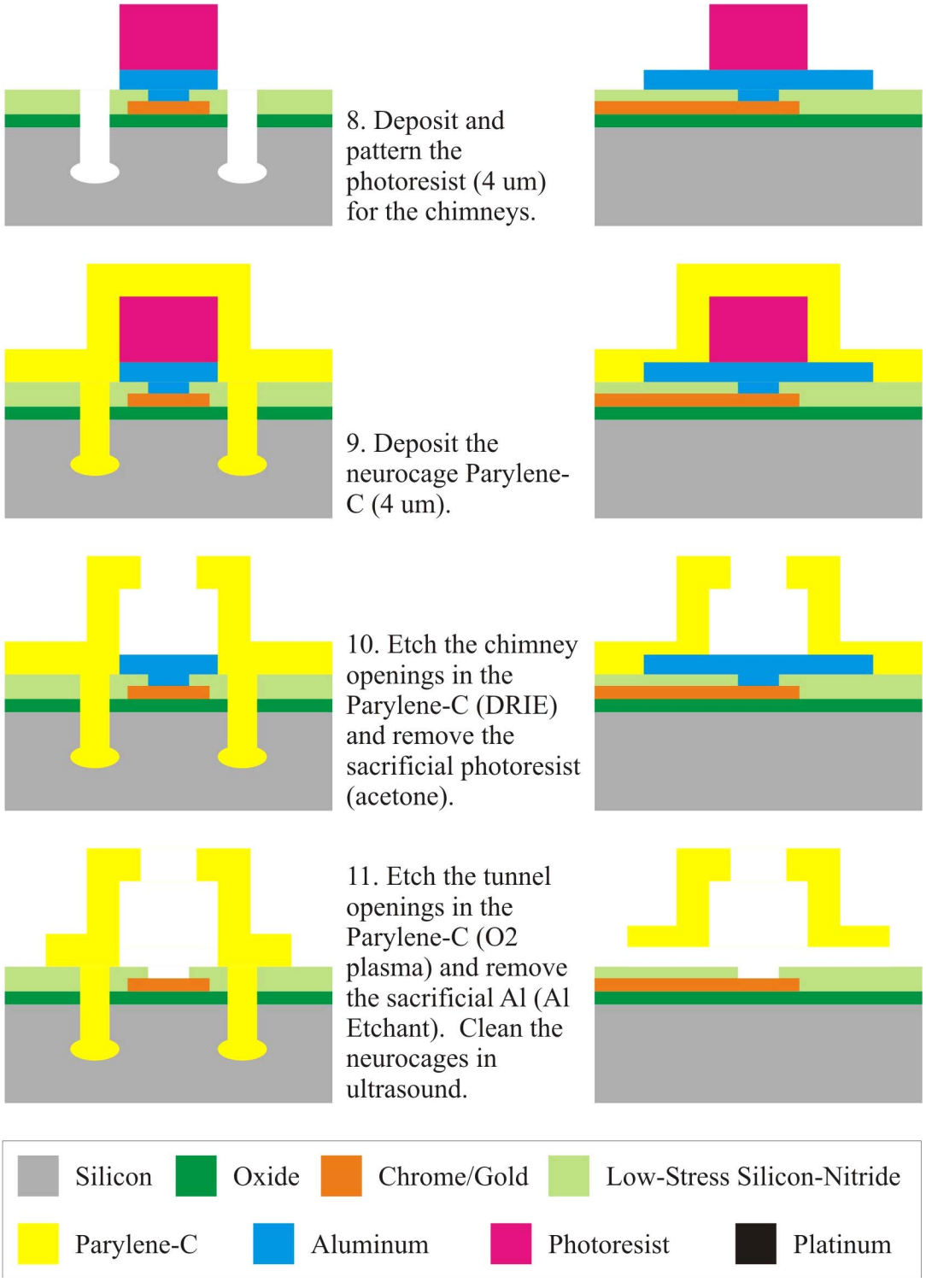


Fig. 4-20. Process flow for the neurocages on silicon with Parylene-C insulation, sacrificial aluminum for the tunnels, and sacrificial soft-baked photoresist for the chimneys. (Not drawn to scale)


Through Anchors
Through Tunnels
1. Thermal oxidation (0.5 um)
2. Thermally evaporate and pattern the Cr/Au (0.01 um/0.3 um) for the electrodes.
3. Etch the oxide (BHF) for the neurocage anchors.
4. Deposit the low-stress silicon-nitride insulation (1 um).
5. Etch the silicon-nitride (SF6 plasma) for the electrode vias.
6. Etch the silicon-nitride (SF6 plasma) and the silicon (DRIE) for the neurocage anchors.
7. Thermally evaporate and pattern the Al (1 um) for the tunnels.
Silicon
Oxide
Chrome/Gold
Low-Stress Silicon-Nitride
Parylene-C
Aluminum
Photoresist
Platinum

Through Anchors **Through Tunnels**



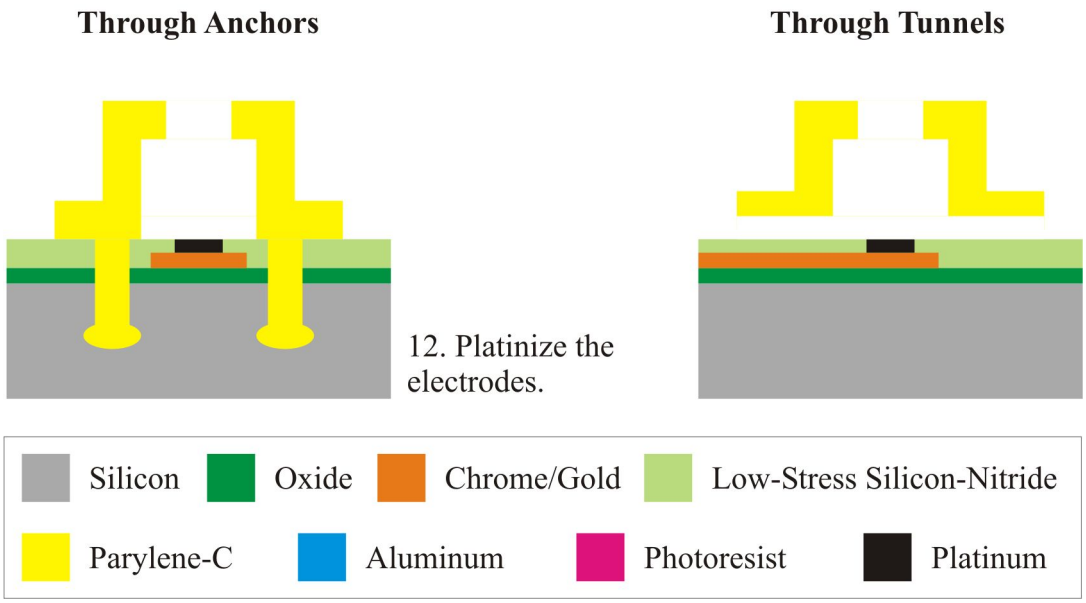


Fig. 4-21. Process flow for the neurocages on silicon with low-stress silicon-nitride insulation, sacrificial aluminum for the tunnels, and sacrificial soft-baked photoresist for the chimneys. (Not drawn to scale)

The fabrication process begins by first cleaning the silicon wafer thoroughly in piranha, followed by HF, to remove any potential organic or metallic contaminants. Next, a thin layer, 0.5 μm, of thermal oxide is grown on the silicon.

A thin layer of lift-off resist (LOR3B, MicroChem Corporation, Newton, MA) is then spun onto the wafer and soft-baked at 190°C for 10 minutes. This lift-off resist is used to create the undercut, such as that described in Section 3.2.1 (Fig. 3-5), to allow easy metal lift-off. A second layer of photoresist, approximately 1 μm thick, is then spun onto the wafer and soft-baked at 100°C for 30 minutes. Following the exposure and development of the two layers of photoresist, the wafer is then treated briefly with O_2 plasma to ensure all of the photoresist has been removed from the electrode regions. The chrome and gold for the electrodes is then thermally evaporated. The photoresist underneath the undesired metal is then dissolved in ST-22 Stripper (ATMI, Danbury,

CT), a photoresist stripper, followed by acetone with ultrasonic agitation, leaving only the chrome-gold for the electrodes (Fig. 4-22).

If Parylene-C is the insulation material, anchors for the insulation are next etched. (This step is not necessary if the insulation is low-stress silicon-nitride.) The silicon wafer is baked at 100°C for 10 minutes and treated with HMDS for 1 minute. A single layer of photoresist, approximately 4 μm thick, is spun on, soft-baked at 100°C for 30 minutes, and patterned to form the openings for the insulation anchors. A brief O_2 plasma treatment is done to ensure all of the photoresist in the insulation anchor openings has been removed. The insulation anchors are first etched into the oxide using a BHF solution. Subsequently, the insulation anchors are etched into the silicon using the DRIE process outlined in Section 3.1.1. The wafer is again treated with O_2 plasma to ensure any C_4F_8 remaining on the surface after the DRIE etching process is removed. The photoresist is then stripped in ST-22 Stripper, followed by acetone with ultrasonic agitation.

Next, the silicon wafer is baked at 100°C for 10 minutes and treated with HMDS for 1 minute. A single layer of photoresist, approximately 4 μm thick, is spun on, soft-baked at 100°C for 30 minutes, and patterned to form the openings for the neurocage anchors. A brief O_2 plasma treatment is done to ensure all of the photoresist in the

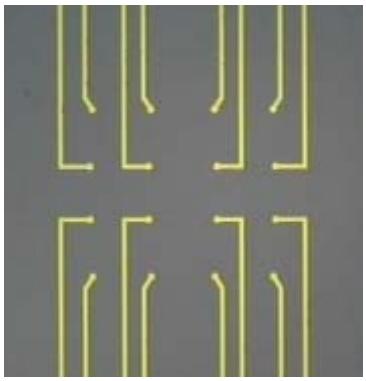


Fig. 4-22. Optical image of the chrome/gold electrodes after thermal evaporation and lift-off

neurocage anchor openings has been removed. The neurocage anchors are etched into the oxide using BHF solution. This is done prior to the deposition of the insulation layer as the BHF solution tends to undercut both the Parylene-C and the low-stress silicon-nitride, enlarging the anchors and potentially undercutting the tunnels. The neurocage anchors are not etched into the silicon at this point to prevent them from being pre-filled with either Parylene-C (in the case of Parylene-C insulation) or photoresist. The photoresist is then stripped in ST-22 Stripper, followed by acetone with ultrasonic agitation (Fig. 4-23).

The insulation layer is then deposited. If Parylene-C is used for the insulation, the wafer is first treated with piranha at 120° for 5 minutes and then the A-174 Parylene Adhesion promoter for 30 minutes. 4 µm of Parylene-C is then deposited to form the insulation. If low-stress silicon-nitride is used for the insulation, the nitride is deposited using plasma-enhanced chemical vapor deposition.

If the insulation is silicon-nitride, the wafer is baked at 100°C for 10 minutes and treated with HMDS for 1 minute. This is not necessary if the insulation is Parylene-C as the HMDS, used to promote the adhesion of photoresist, does not adhere to the Parylene-C. The process then continues by spinning a layer of photoresist, approximately 15 µm thick, soft-baking at 100°C for 30 minutes, and then patterning the photoresist for the

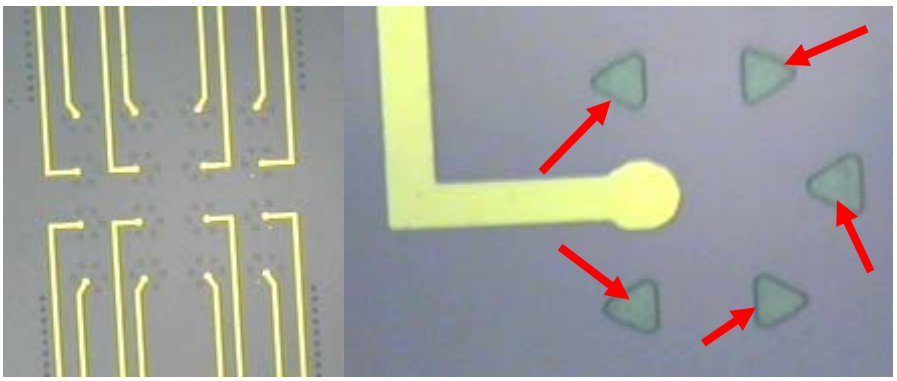


Fig. 4-23. Optical image of the neurocage anchors after etching into the oxide. The right image shows a closeup of the anchors (red arrows) for one neurocage.

electrode vias. If the insulation is Parylene-C, the electrode vias are etched using a DRIE process with alternating O_2 and C_4F_8 plasmas [51–52]. The C_4F_8 plasma serves the same function in this process as in the standard Bosch process, creating a more anisotropic etch process for vertical side-walls in the Parylene-C. If the insulation is silicon-nitride, a brief O_2 plasma treatment is used to ensure all of the photoresist is removed from the electrode vias. SF_6 plasma is then used to etch the silicon-nitride to create the electrode vias. For both insulation types, the photoresist is then stripped in ST-22 Stripper, followed by acetone with ultrasonic agitation (Fig. 4-24).

Again, if the insulation is silicon-nitride, the wafer is baked at 100°C for 10 minutes and treated with HMDS for 1 minute. The process continues, for both insulation types, by spinning a layer of photoresist, approximately 15 μm thick, and soft-baking at 100°C for 30 minutes. The openings for the neurocage anchors are patterned in the photoresist. If the insulation is silicon-nitride, a brief O_2 plasma treatment is used to ensure all of the photoresist is removed from the neurocage anchors. The insulation is

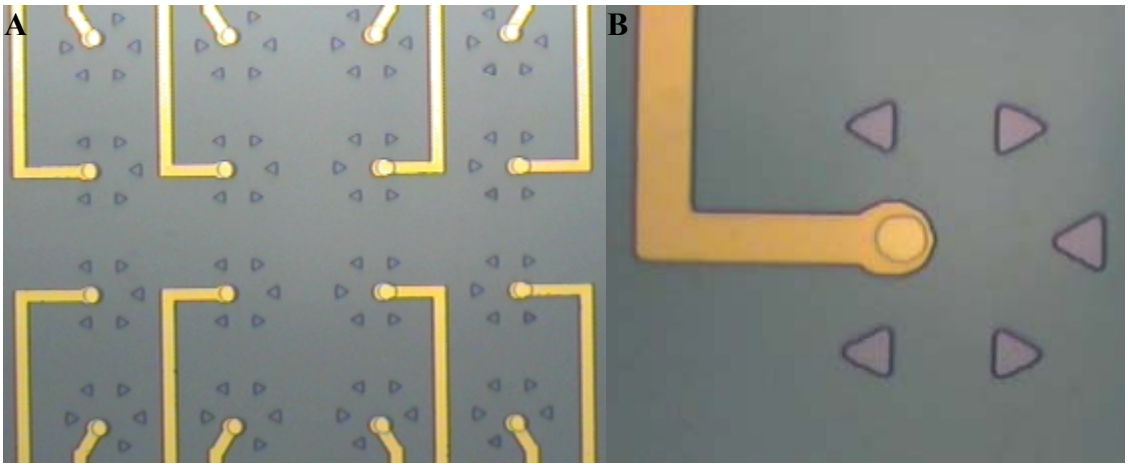


Fig. 4-24. Optical image of the electrode vias etched through the insulation. Fig. **A** shows the neurocage array with vias etched through the Parylene-C insulation. Fig. **B** shows a closeup of a single neurocage with the via etched through the low-stress silicon-nitride insulation.

then removed from the neurocage anchor openings with the DRIE process, with alternating O_2 and C_4F_8 plasmas, for the Parylene-C and with SF_6 plasma for the silicon-nitride. The wafer is treated briefly with a dilute HF solution to ensure the native oxide is removed from the neurocage anchors. Next, the neurocage anchors are etched into the silicon using the DRIE process described in Section 3.1.1. The photoresist is then stripped in ST-22 Stripper, followed by acetone with ultrasonic agitation (Fig. 4-25).

If the insulation is Parylene-C, the next step is to anneal the Parylene-C, to improve its chemical adhesion. This annealing is done in a vacuum oven at 200°C for 48 hours. Next, the Parylene-C is treated with very low-powered O_2 plasma for 30 seconds. This roughens the Parylene-C slightly and puts hydroxyl groups on the Parylene-C surface. Untreated Parylene-C is very hydrophobic, and this ensures the surface is hydrophilic so that the subsequent layers of aluminum adhere properly.

For silicon-nitride insulation, the wafer is first baked at 100°C for 10 minutes and treated with HMDS for 1 minute. Then, for both insulations, a 4 μm thick layer of photoresist is spun on and soft-baked at 100°C for 30 minutes. The photoresist is

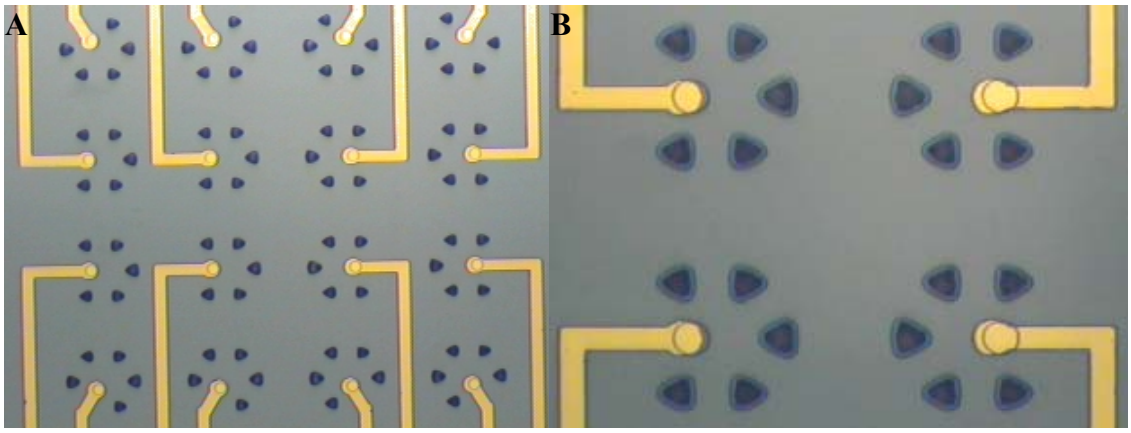


Fig. 4-25. Optical images of the neurocage anchors etched through the insulation and into the silicon. Fig. **A** shows the neurocage array with anchors etched through the low-stress silicon-nitride insulation. Fig. **B** shows a closeup of neurocages with anchors etched through the Parylene-C insulation.

exposed and developed to create the openings for the tunnels. 1 μm of aluminum is thermally evaporated, in two consecutive depositions. The photoresist underneath the undesired aluminum is lifted off in acetone with ultrasonic agitation, leaving only the aluminum for the tunnels (Fig. 4-26). The final tunnel height was 0.93 μm (±0.06 μm).

Next, for the Parylene-C insulation, a 4 μm thick layer of photoresist is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to define the areas where the aluminum etch stop will be deposited. Next, 0.2 μm of aluminum is thermally evaporated. The photoresist, and the unwanted aluminum, is lifted off in acetone with ultrasonic agitation, leaving only the Al etch stop (Fig. 4-27). This etch stop is not necessary when silicon-nitride is used as the insulation, as the silicon-nitride, unlike the Parylene-C, is impervious to O_2 plasma and serves as its own

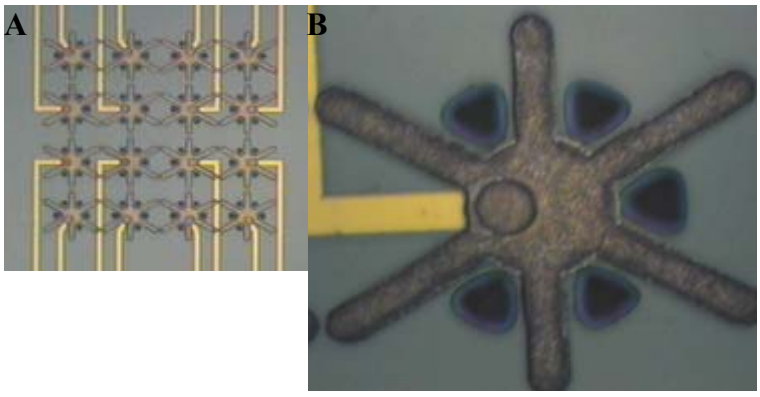


Fig. 4-26. Optical images of the aluminum tunnels. Fig. **A** shows the neurocage array with aluminum tunnels on the low-stress silicon-nitride insulation. Fig. **B** shows a closeup of a neurocage with aluminum tunnels on the Parylene-C insulation.

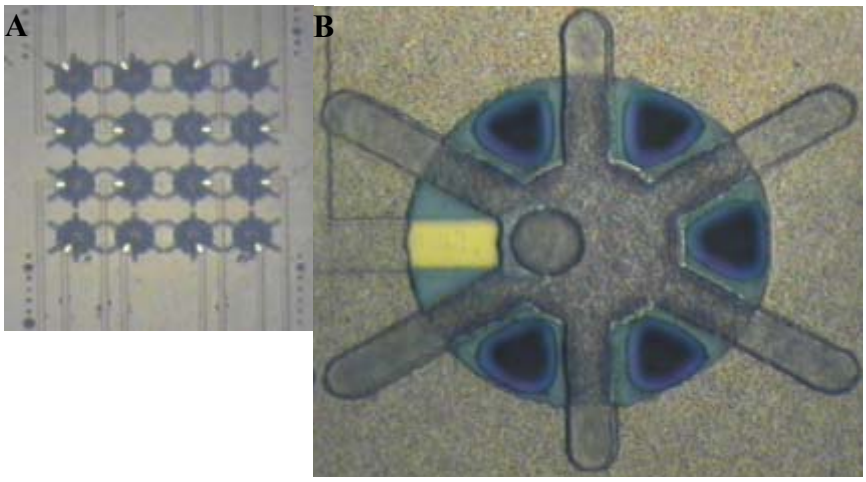


Fig. 4-27. Optical images of the aluminum etch stop on the Parylene-C insulation. Fig. **A** shows a neurocage array. Fig. **B** shows a closeup of a neurocage.

etch stop.

If silicon-nitride is the insulation, the wafer is baked at 100°C for 10 minutes an treated with HMDS for 1 minute. For both insulation types, the 4 μm thick layer of photoresist for the chimneys is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to define the chimneys (Fig. 4-28). The final chimney height was 4.11 μm (±0.63 μm). Next, the 4 μm of Parylene-C to form the neurocage is deposited.

A 15 μm thick layer of photoresist is spun onto the wafer and soft-baked at 90°C for 40 minutes. The photoresist is exposed and developed to form the chimney openings. The Parylene-C is etched in the DRIE, with alternating O_2 and C_4F_8 plasmas, to open the chimneys. The photoresist in the chimneys is then dissolved in acetone.

15 μm of photoresist is spun on and soft-baked at 85°C for 45 minutes. The photoresist is exposed and developed to create the tunnel openings. The Parylene-C is etched with O_2 plasma to open the tunnels. Once the etching is complete, the sacrificial aluminum for the tunnels and the etch stop is removed in Aluminum Etchant Type A at 60°C. Finally, the neurocages are cleaned in an ultrasonic bath to remove any remaining Parylene-C at the tunnel and chimney openings. Optical images and SEMs of the final neurocages are shown in Figs. 4-29 and 4-30, respectively.

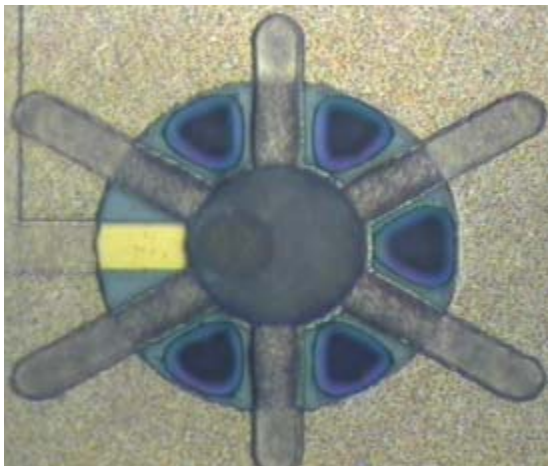


Fig. 4-28. Optical image of a neurocage with a photoresist chimney. This neurocage has Parylene-C insulation. The aluminum tunnels and aluminum etch stop are also visible.

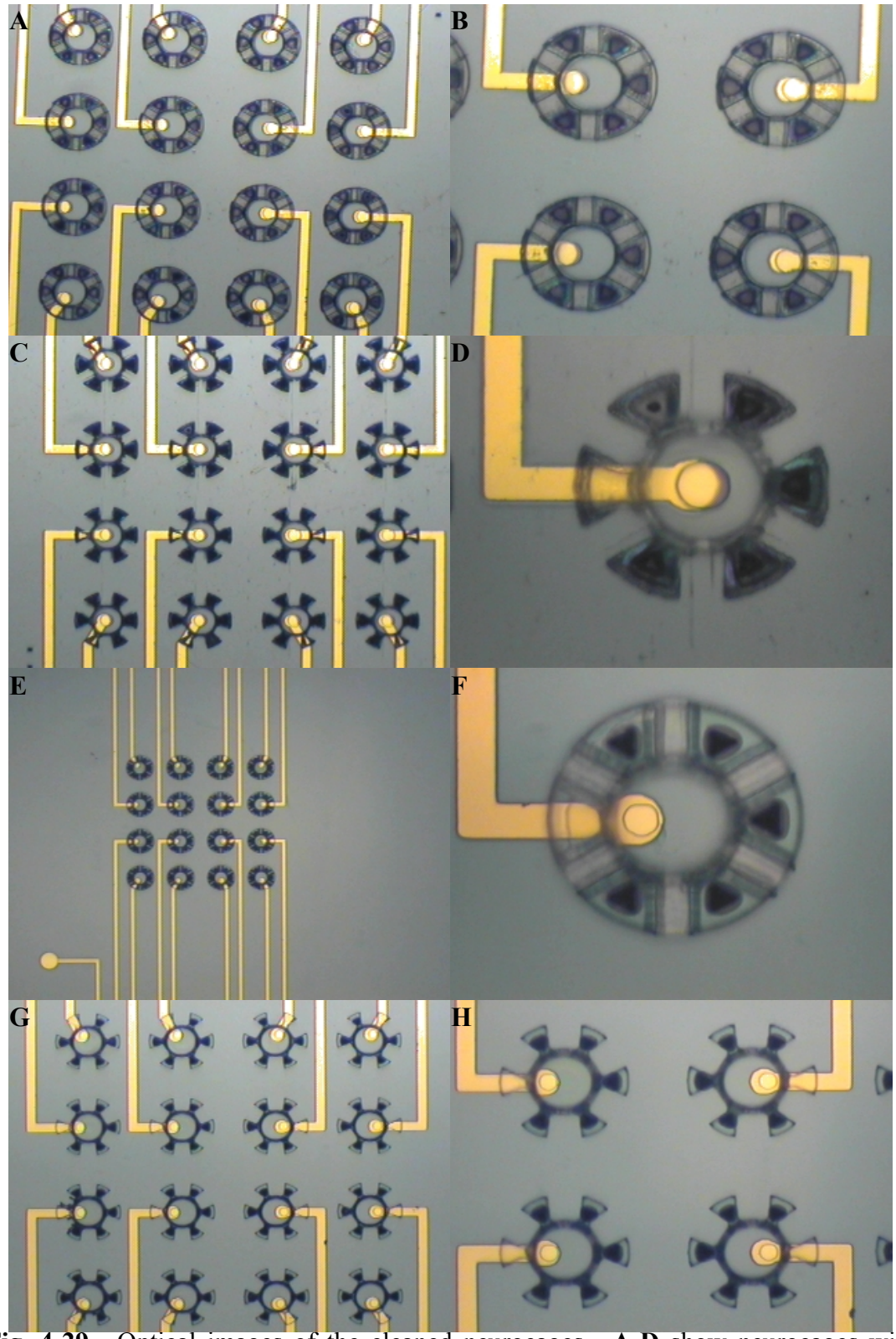
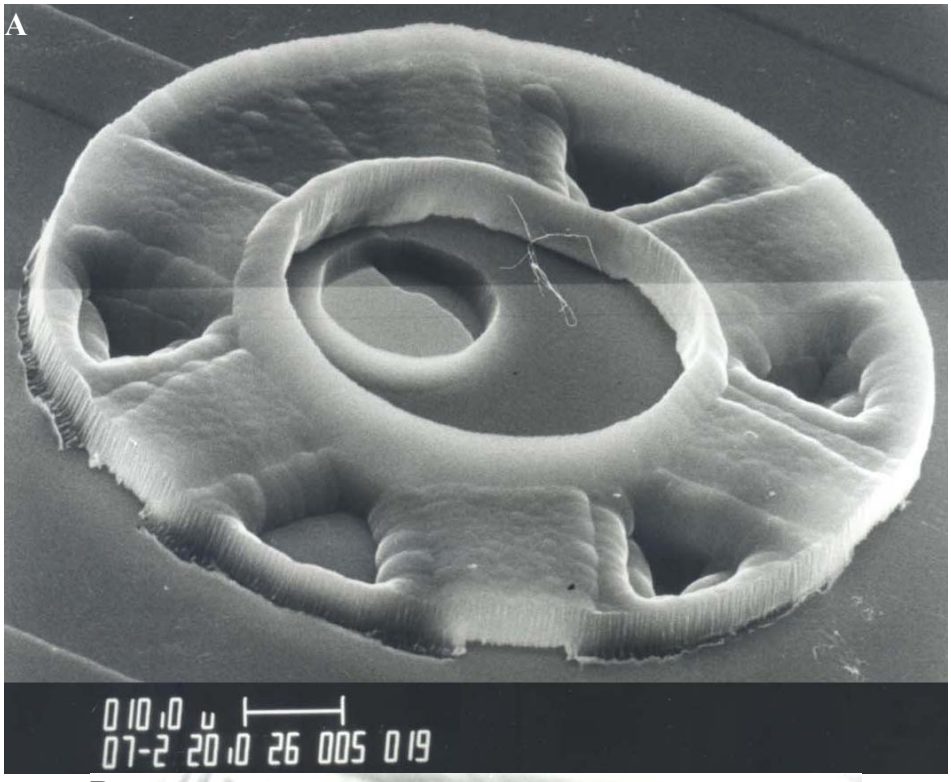


Fig. 4-29. Optical images of the cleaned neurocages. **A-D** show neurocages with Parylene-C insulation. **E-H** show neurocages with low-stress silicon-nitride insulation. **A**, **B**, **E**, and **F** show neurocages with 25 µm long tunnels. **C**, **D**, **G**, and **H** show neurocages with 4 µm long tunnels.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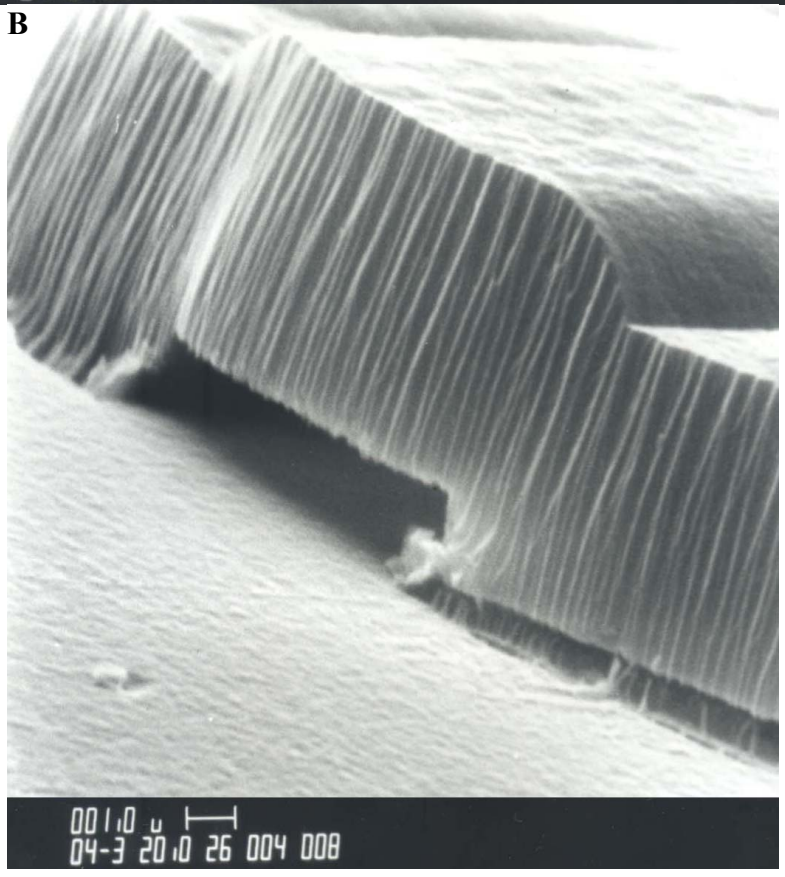
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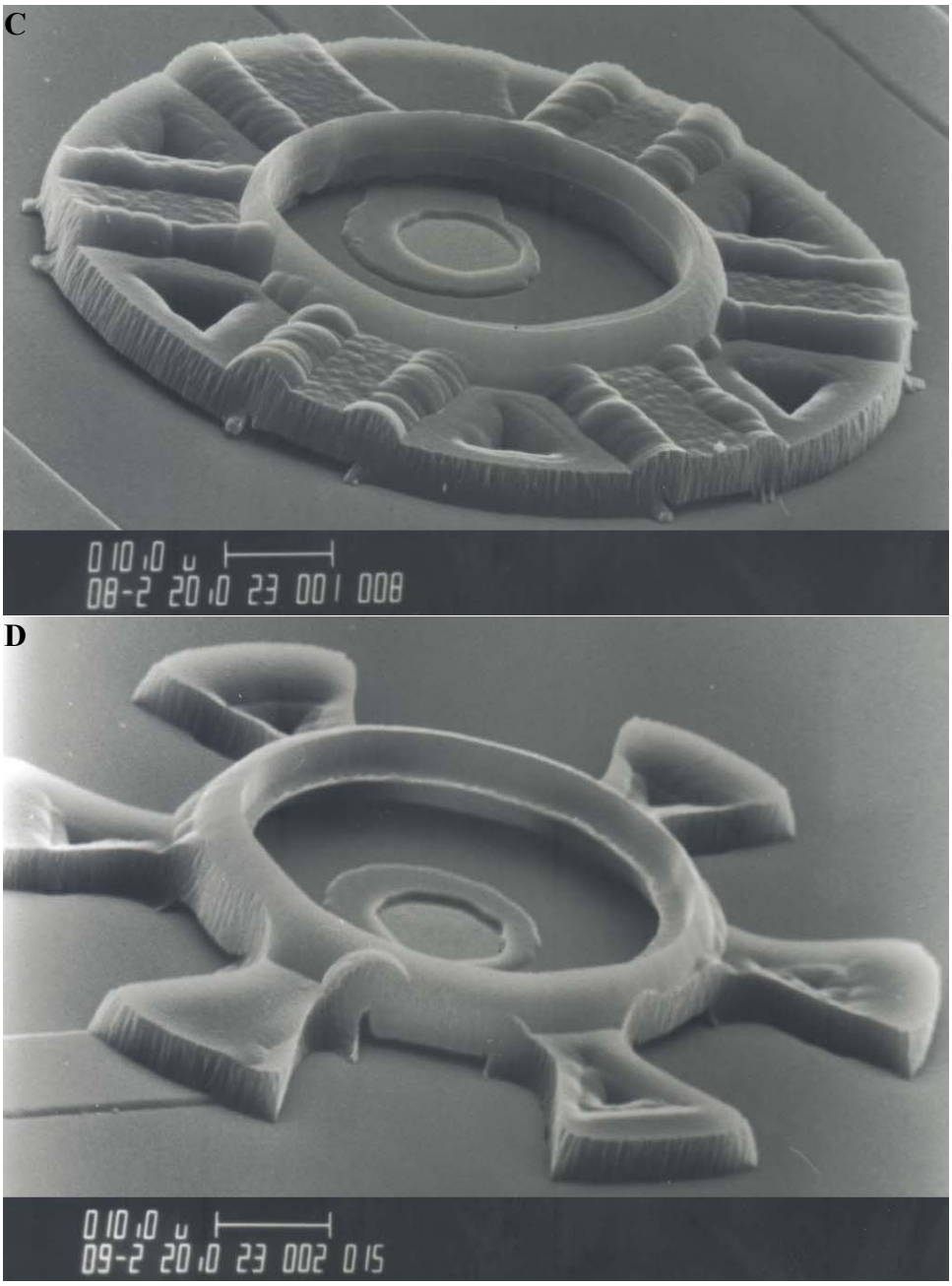


Fig. 4-30. SEMs of neurocages on silicon with electrodes. **A** and **B** are neurocages on Parylene-C insulation. **A** shows a neurocage with 25 μm long tunnels. **B** is a closeup of one of the tunnels. **C** and **D** are neurocages on low-stress silicon-nitride insulation. **C** shows a neurocage with 25 μm long tunnels. **D** shows a neurocage with 4 μm long tunnels.

4.8 Culturing Results

Once the neurocages have been fabricated and cleaned, the chips are wire-bonded to a printed circuit board (PCB) and culture dishes are glued on top (Fig. 4-31) [47–50]. The neurochips are then ready for culturing.

First, the neurocages are sterilized with UV light and then covered with warm (37°C) 0.05% PEI solution in borate buffer solution for 12 hours, which penetrates the neurocages, including the tunnels. The PEI is subsequently rinsed out, and 2 μM laminin is added. After overnight incubation, the laminin is rinsed out. This procedure is repeated a total of three times so that there are alternating layers of PEI and laminin. This is known as the "layer-by-layer" method. The laminin promotes neuronal process outgrowth and the laminin serves as the negatively charged layer to which the positively charged PEI binds. Once the three layers of PEI/laminin are deposited, the culture dish is drained and dried. The background neurons are plated to a density of 30 K/cm^2 on the dry surface and the dish is flooded with neurobasal culture media. Individual neurons are then loaded manually into the neurocages with a pressure-driven micropipette. The first

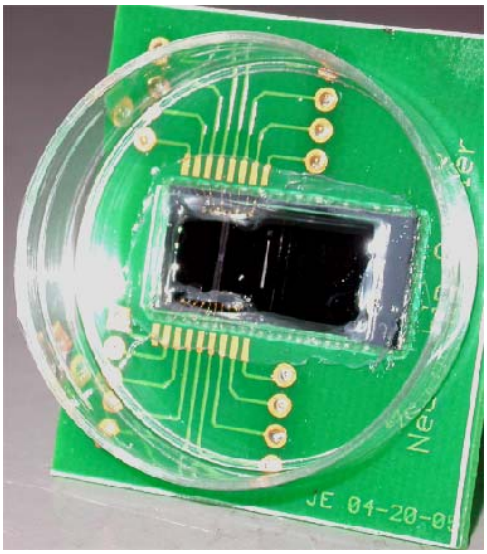


Fig. 4-31. Optical image of a neurochip ready for culturing. The neurochip (in the center) has been glued and wire-bonded to the PCB. The culture dish (with a hole in the center for the neurochip) is then glued on top. The neurochip is then ready for culturing.

signs of neuron growth usually appear within 12–24 hours of loading. In addition to the neurobasal media, brain-derived neurotrophic factor (20 ng/mL) is also added to improve the long-term neuronal survival rate. The osmolarity of the cultures is also carefully controlled.

Nomarski images of these cultured neurons are shown in Fig. 4-32. The neurons are clearly visible in the neurocages, extending neurites out through the tunnels to form synaptic connections with their neighbors. In addition, due to the transparency of the Parylene-C, it is possible to see the neurites when they are in the tunnels. Fig. 4-33 shows an SEM of a fixed neuron inside a neurocage.

The survival rate for neurons in these neurocages is good, nearly 50% even after 3 weeks (Fig. 4-34). If only the initially viable neurons are considered (i.e., those neurons

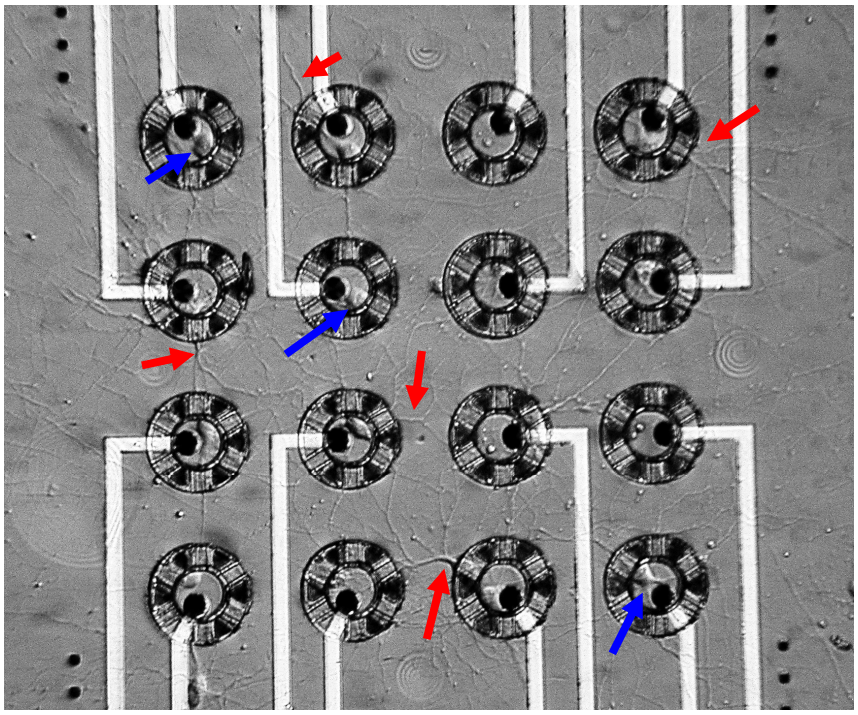


Fig. 4-32. Nomarksi image of neurons growing in neurocages with Parylene-C insulation. The blue arrows indicate some of the neurons in neurocages. The red arrows indicate some of the neurites extending out of the neurocages.

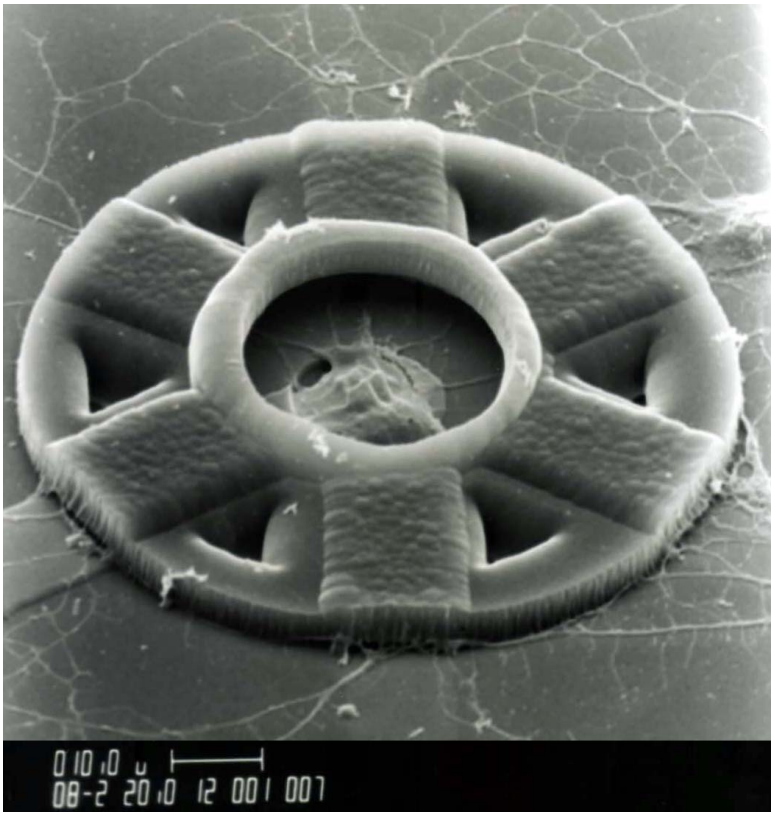


Fig. 4-33. SEM of a fixed neuron inside a neurocage after 8 days of growth. The neurites extending out through the tunnels are visible.

that were alive at day 2), the survival rate increases to nearly 75% after 3 weeks. In addition, these neurocages had a neuronal escape rate less than 1%. Some neurons have survived in the neurocages for up to 4 weeks.

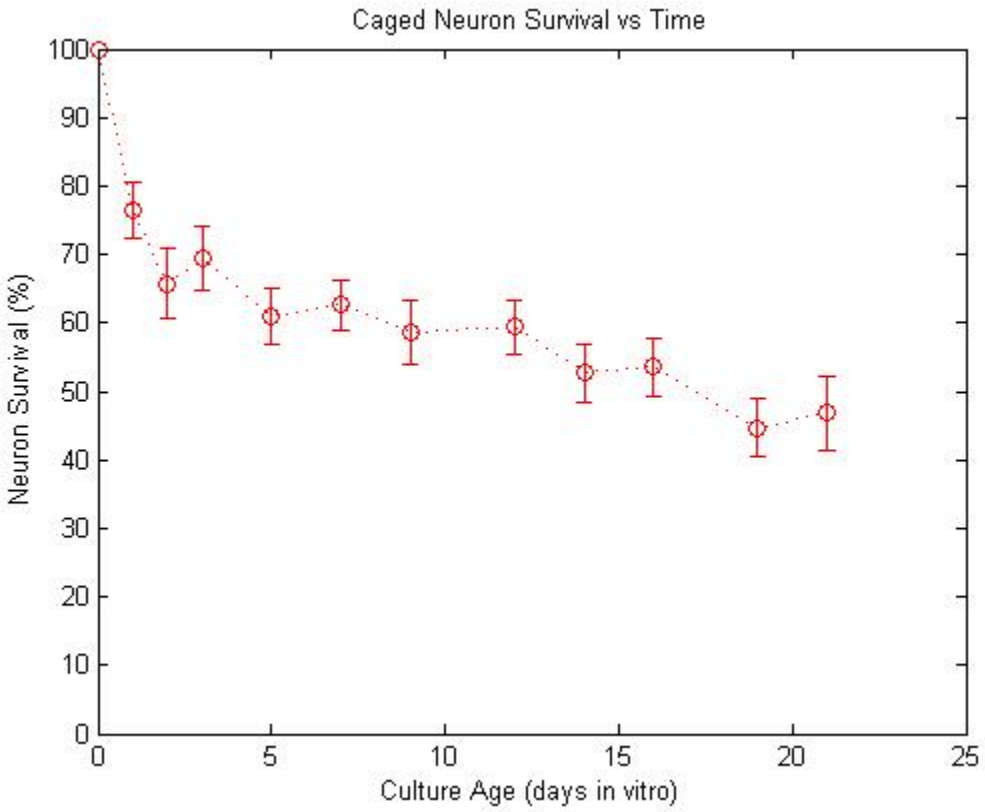


Fig. 4-34. Neuronal survival rate for neurons inside neurocages on silicon (includes data from neurocages with both Parylene-C and low-stress silicon-nitride insulation)

4.9 Electrical Stimulation and Recording

To test our ability to successfully stimulate the caged neurons, the voltage-sensitive dye (RH237 or Di-4-ANNEPDHQ, Invitrogen Corporation, Carlsbad, CA) responses of the neurons were recorded at 2 kHz with a CCD camera [51]. Neurons inside neurocages were successfully stimulated with current pulses passing through the electrode at the base of the neurocage. Either polarity of bipolar pulses was effective in exciting action potentials. Fig. 4-35 shows the results of these stimulation tests for two neurons. The graph shows the change in fluorescence intensity for two neurons. The black trace corresponds to an un-stimulated neuron and the blue trace is the response for a stimulated neuron. The red line marks the onset of the current pulse stimulus. As can

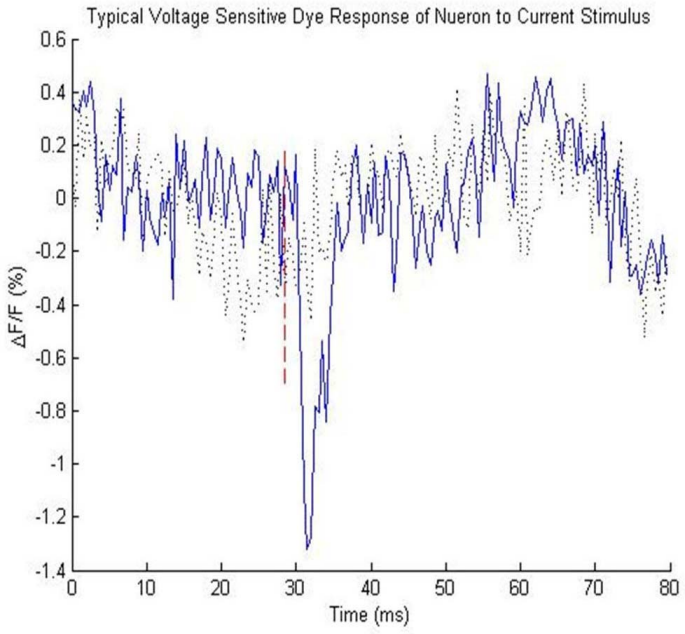


Fig. 4-35. This graph shows the change in fluorescence intensity in response to a current stimulus (denoted in red) for two different neurons. The black-dotted trace corresponds to the un-stimulated neuron exhibiting no significant change. The blue trace corresponds to the stimulated neuron, which exhibits a change in fluorescence indicative of an action potential response.

be seen, the un-stimulated neuron exhibits no real change in fluorescence intensity. The stimulated neuron, however, exhibits a change in fluorescence intensity after the stimulus. The change is approximately -1.3%, corresponding to approximately 100 mV. The peak is about 3 msec wide. Both of these are indicative of an action potential, indicating that the neuron has been successfully stimulated.

Electrical recordings from neurons in neurocages have also been obtained. Fig. 4-36 shows electrical recordings for an array of neurons inside neurocages. The neurons in this experiment are 14 days old, although recordings have been made in cultures as old as 4 weeks. This graph shows the response of the neural network after one of the neurons (Channel 14) is stimulated with a 12 μA current pulse. (The graph shows an overlay of the neural network response for 5 separate trials.) The current pulse is applied at t = 40 ms. As can be seen, neurons on Channels 4, 7, 11, and 15 fire action potentials (seen as voltage spikes) after the stimulation This shows that the neurons on these 5 channels (4, 7, 11, 14, and 15) have formed synaptic connections. Neurons are present in the

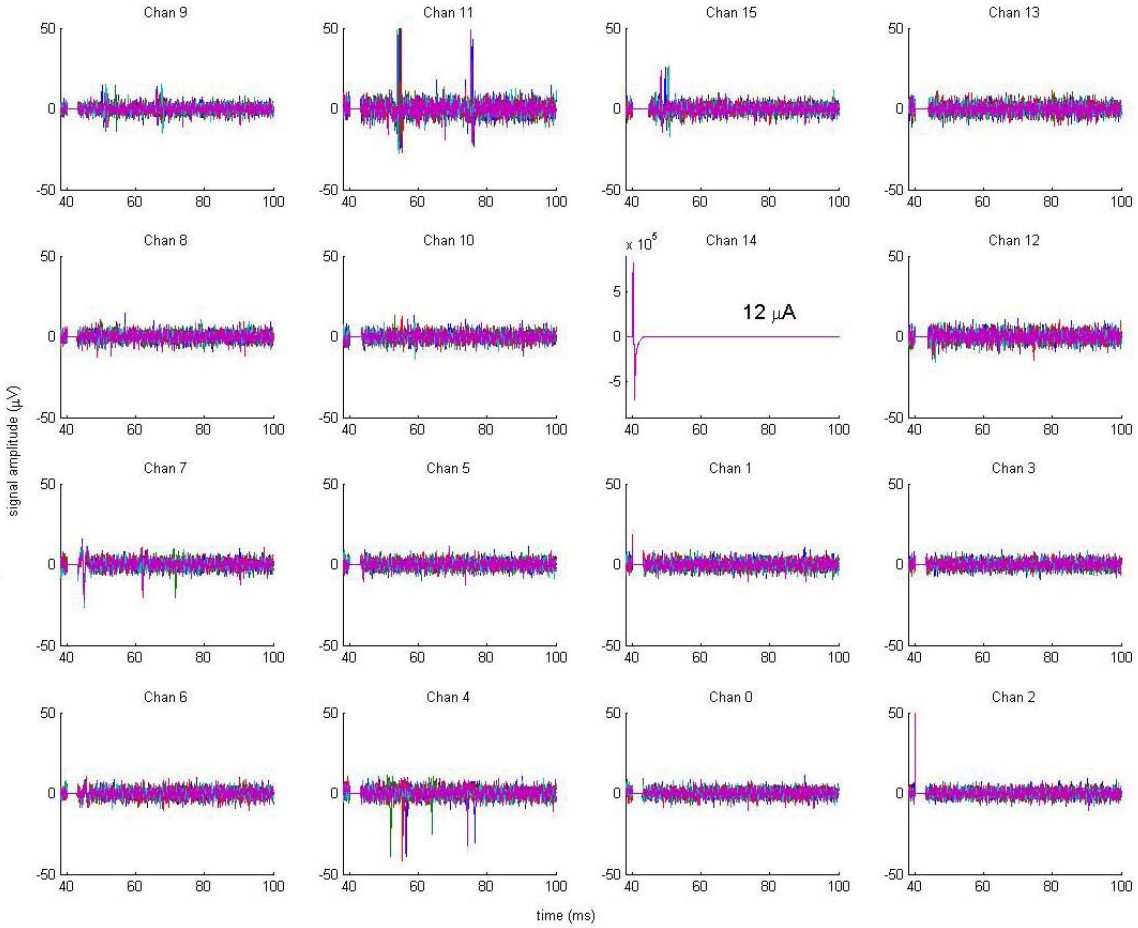


Fig. 4-36. Electrical recordings from the neurons in the neural network. The neuron on Channel 14 received a current stimulus (12 μA) at t = 40 ms. Corresponding action potentials (the large spikes of magnitude 20–50 μV) were recorded from the neurons on Channels 4, 7, 11, and 15, indicating that these 5 neurons have formed synaptic connections.

neurocages at the other channels; however, neurons do not form synaptic connections with all of the other neurons in the neurocage array. Hence, stimulating the neuron on Channel 14 does not stimulate a response in all of the remaining 15 neurons in the array. Fig. 4-37 shows the spontaneous activity (i.e., neurons firing without a stimulus present) in the neural network. As can be seen, multiple spontaneous action potentials are recorded on roughly half the channels.

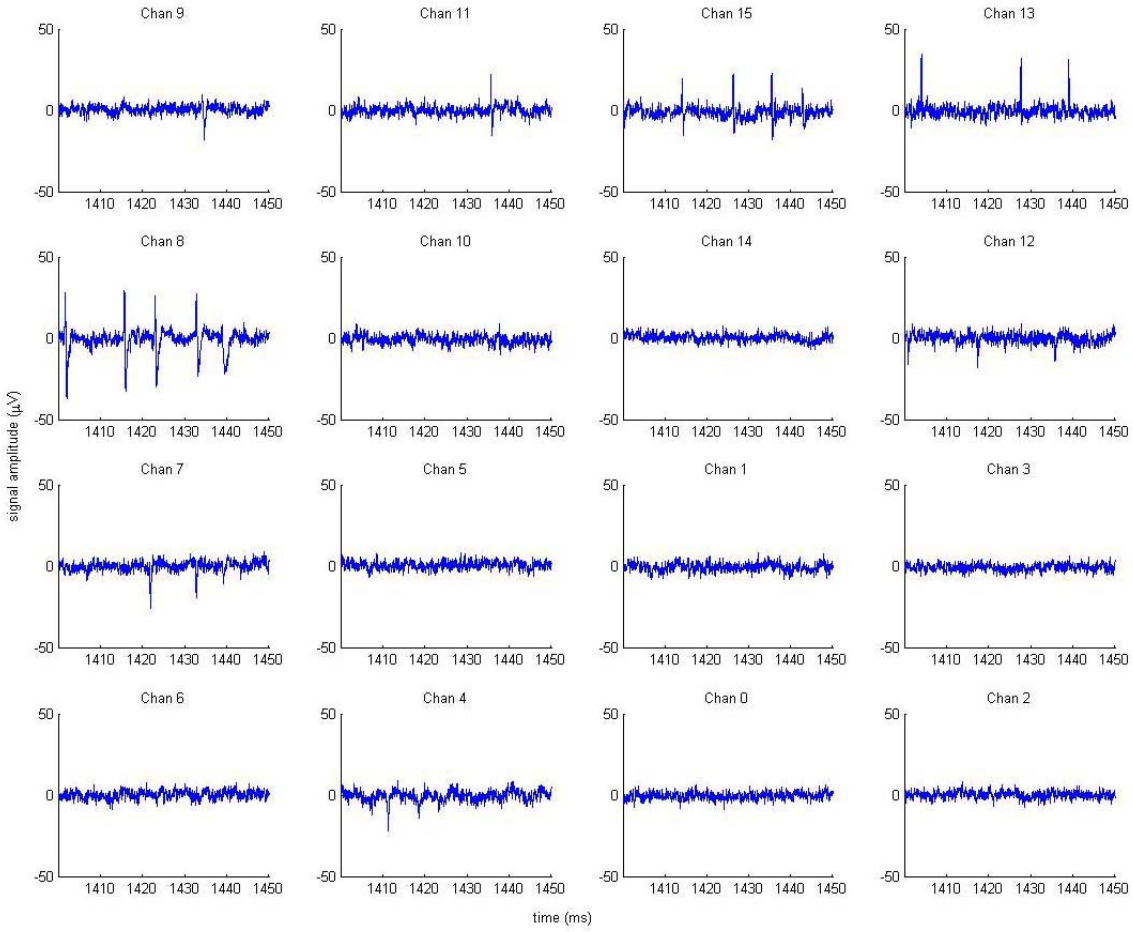


Fig. 4-37. These graphs show the spontaneous activity in the neural network. No stimulus is required for the network to exhibit this activity. The action potentials are recorded on roughly half the channels (4, 7, 8, 9, 11, 12, 13, and 15).

4.10 Long-Term Impedance Testing

The long-term electrical impedance of the electrodes, with 4 μm of Parylene-C insulation, was also tested. The setup to test the impedance includes a phase lock-in amplifier (Model 5210, EG&G Princeton Applied Research), micromanipulators with probes, computer with LabVIEW software, and saline. The large bonding pad on the edge of the neurochip is probed using one of the micromanipulators. The small electrode, the one inside the neurocage, is covered with a drop of saline. The probe on the other micromanipulator is put into the saline. Both probes are connected to the lock-in

amplifier. Using the lock-in amplifier and the LabVIEW software, the impedance of the electrodes was calculated.

After the neurochip was tested, it was placed in saline at 77°C. This long-term soaking is designed to simulate the actual working conditions of the neurochip, which during culturing, is covered with a culture media (similar to saline) and placed in an incubator at 37°C. Increasing the temperature to 77°C for this testing allows accelerated life-time testing. Thus, if the neurochip works successfully for 10 days at 77°C, then it will work for longer periods of time at lower temperatures. To calculate how much longer the neurochip will work at the lower temperatures, it is necessary to calculate the life-time at two different temperatures. Then using an Arrhenius relationship, the life-time at all temperatures can be calculated. 4 weeks at 77°C corresponds to more than 5 years at 37°C.

The electrical impedance was tested several times over 4 weeks. Fig. 4-38 shows the electrical impedance for one of the electrodes on the neurochip. (The remaining 15 electrodes on the neurochip evidence similar electrical impedances.) As the graph shows, the impedance does not change significantly over the 4 weeks. Thus, it is reasonable to expect that the neurochips will continue to function normally for longer than 4 weeks when used at 37°C. Given that the cultured neurons do not generally survive for longer than about 4–5 weeks, the lifetime of these devices is more than sufficient.

The graph also shows that the log of the electrical impedance is linear over the given frequency range. This suggests that the response of the electrode is primarily capacitive. This agrees with the literature [46] which says that the impedance of a microelectrode is dominated by the electrolytic capacitance (double-layer capacitance) at

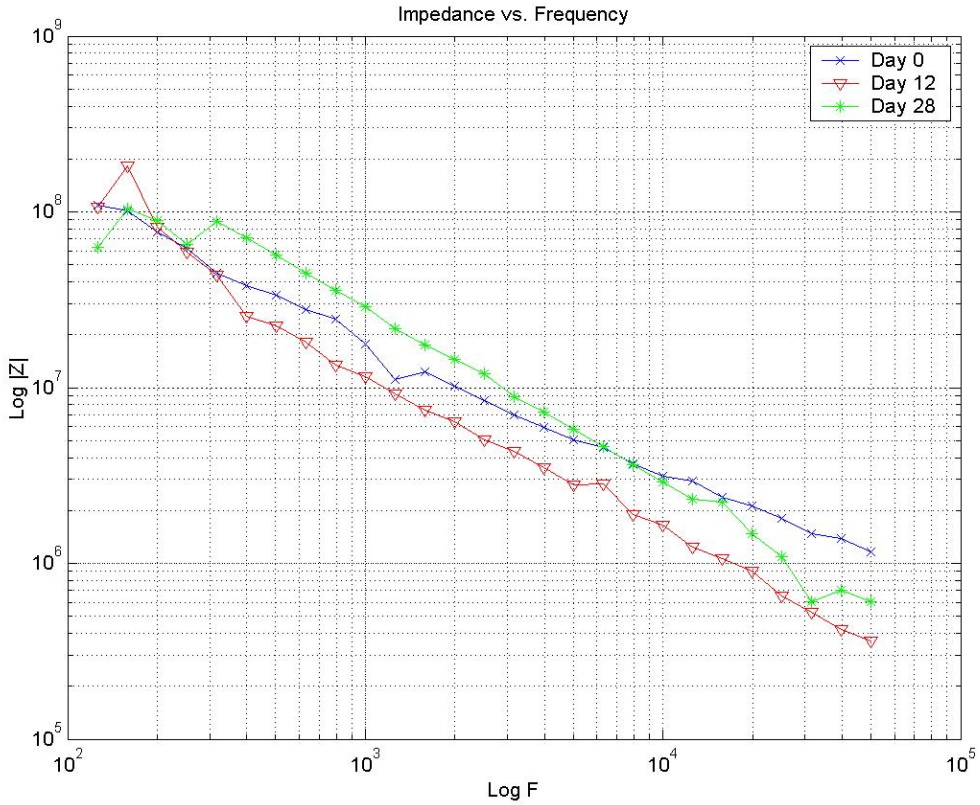


Fig. 4-38. Graph of the impedance versus frequency for one of the neurocage electrodes with Parylene-C insulation. As can be seen, the plotted lines are linear, indicating that the impedance is dominated by the electrolytic capacitance. Also, there is no significant loss in impedance after soaking in saline at 81°C for 28 days.

the electrode-saline interface, rather than the resistance of the microelectrode itself. Hence, it is expected that the log of the impedance of the electrode is linear.

4.11 Future Work

The fabrication process outlined in Section 4.7 successfully creates neurocages capable of stimulating neurons and recording action potentials. However, the neuronal survival rate of 45–50% after 3 weeks, while acceptable, still needs improvement. As shown earlier, changes in tunnel height do affect the neuronal escape rate and changes in

chimney height affect the survival rate. Further geometry changes might yield an increase in survival rate and should be explored.

Although Parylene-C was the primary insulation material for this neurocage, it is possible that other insulation materials, such as the low-stress silicon-nitride explored briefly as part of this project, might provide better insulation. Preliminary studies were conducted to improve the adhesion and permeability properties of Parylene-C, through surface treatments and high-temperature annealing. Further studies should be conducted to better explore the link between the insulating properties of Parylene-C and the high-temperature annealing of Parylene-C. In addition, although the fabrication process is straight-forward, it is quite lengthy and time-consuming. It is possible that other insulation materials might reduce the fabrication time.

Long-term electrical testing of the electrodes with Parylene-C insulation was conducted. It was determined that the neurochips will function normally over more than a 4 week period when cultured at 37°C. In addition, as the literature suggests, the electrode impedance is dominated by the double-layer capacitance between the electrolyte (saline) and the electrode itself. As some neuron cultures have survived for up to 4 weeks, neurochips that only function normally for 4 weeks cannot be safely re-used without suffering a loss of impedance. It has already been demonstrated that the neurocages, themselves, can be cleaned of the neuron debris and re-used, the limiting factor in re-using the neurochips is the degradation of the electrodes. Hence, additional testing should be done to determine how long the neurochips will function at 37°C and whether they can be re-used for multiple experiments. Similar experiments should also

be conducted for the different insulation materials studied, such as low-stress silicon-nitride.

Finally, these stimulation and action potential recording studies were conducted with very small neural networks, comprising fewer than 16 neurons. Such small networks do not mimic the neural networks found in most living creatures, including humans. The same fabrication process presented here can be used to create larger arrays of neurocages, and these larger arrays would more closely conform to neural networks found *in vivo*.

CHAPTER 5
Neurocages on Glass with Electrodes

Although the neurocage fabrication process allows large arrays of neurocages to be fabricated, the limiting factor in culturing larger arrays of neurocages is the time required to load neurons into the neurocages. The pH of the culture medium changes quite rapidly, becoming toxic to the neurons, when the chips are out of the incubator for more than about 30 minutes. Using alternative media that does not change pH in air resulted in poor neuronal survival. Unfortunately, only a limited number of neurons can be loaded within that 30-minute time window. An experienced technician can typically only load about 15 neurons manually within that time limit. Thus, a faster, more automated method is required for loading the neurons. One alternative is to use a computer-controlled laser tweezers system to automatically pick up the neurons and load them into the neurocages. The use of the laser tweezers, however, requires the use of an optically transparent substrate, something other than silicon.

5.1 Laser Tweezers

The laser tweezers system uses a single, tightly focused infrared (IR) laser beam to trap and lift neurons and move them in three dimensions above a culture substrate. Once the

neuron is trapped and lifted, a computer-controlled mechanical stage moves the culture substrate until the neuron is above the neurocage where it can be loaded.

Optical trapping of a small object is based on forces of radiation pressure [53–56]. Light has momentum. There is a change in momentum when a light ray is bent by the object that light is passing through. By conservation of momentum, an equal and opposite force is exerted on the object. For a tightly focused Gaussian beam, the exerted net force pushes the object towards the beam focus where the intensity of light is greatest (Fig. 5-1). This traps the object within the laser beam and guarantees that as the laser beam moves, the object moves with it.

The laser tweezers system consists of an inverted microscope, a 980 nm laser module, a beam expander, a motorized mechanical stage, a CCD camera, and steering mirrors (Fig. 5-2) [57]. A laser beam is generated by the IR laser module, and the beam is expanded by the beam expander to match the size of the back aperture of the objective. The beam is then steered into an inverted microscope (Olympus IX71) via a camera port and reflected by a dichroic mirror into a 63x oil-immersion (Zeiss 440460) objective (N.A. 1.25) where it is focused to a point. A CCD video camera is used for viewing the laser spot and capturing

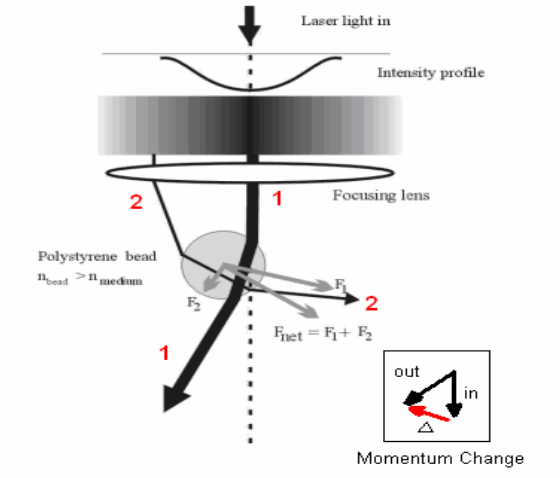


Fig. 5-1. The force F_1 is generated by the momentum change of the thinner ray (the lesser-intensity ray). The force F_2 is generated by the momentum change of the thicker ray (the greater-intensity ray). F_{net} is the sum of the two forces which pushes the bead towards the beam focal point.

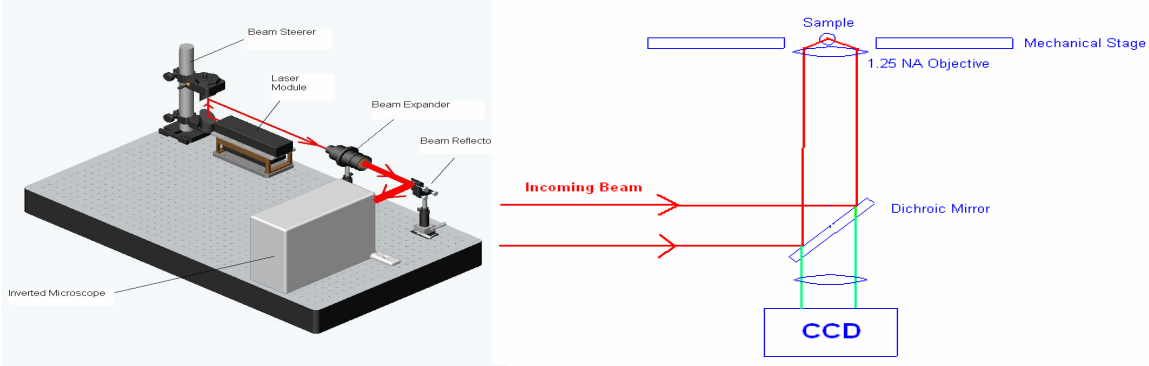


Fig. 5-2. The left picture shows an overview of the laser tweezers system. As the right image shows, the expanded beam is brought to a tight focus at the sample plane (the neuron).

videos or images. Tests have been performed to study the effects of laser intensity and exposure time on neuron survival [57]. It has been determined, with this setup, that a laser power of 100 mW and exposure time of 4 minutes causes no significant photo-damage to the neurons. In general, less than 1 minute is required to move the neuron into the neurocage.

5.2 Design and Fabrication

5.2.1 Glass Slides

The laser tweezers require very thin glass slides, less than 100 μm thick. Unfortunately, these thin substrates are, by themselves, not compatible with the machines used in micro-fabrication as they are incredibly thin and fragile. Standard substrates used in micro-fabrication are four to five times thicker than these glass slides. These glass slides are so fragile that simply rinsing them in water, either under running water or by immersion into a beaker of water, can cause them to crack. Therefore, to use these glass slides it is necessary to mount them on thicker substrates to prevent them from shattering during fabrication.

Standard silicon substrates, 400 μm thick, are used to support the glass slides during fabrication. Prior to each step during the fabrication process, photoresist is put onto the silicon wafer and the glass slide is placed onto the photoresist. It is then baked at 100°C for 5 minutes to ensure the glass slide remains attached during the subsequent processing. At the end of each fabrication step, the photoresist is stripped and the glass slide is removed from the silicon substrate. Ideally, the glass slide would be attached once to the silicon substrate and only removed after the entire fabrication process is complete. However, it was difficult to find a material to attach the glass slide that was capable of withstanding the large number of fabrication steps, the thermal cycling, and the chemicals required at each step, and still allow the glass slide to be removed once fabrication is complete. The photoresist cannot keep the glass slide attached for the entire fabrication process, although it can keep the glass slide attached for a single fabrication step. Unfortunately, since the glass slides must be reattached for each fabrication step, the amount of handling of the glass slides increases with the number of fabrication steps, which increases the likelihood of breaking the glass slide. Thus, on average, only 75% of the glass slides survive the fabrication process without cracking.

5.2.2 Design

The basic neurocage design is not changed by using glass as the substrate [48–50, 57]. The neurocage still has 6 tunnels, 5 anchors, and 1 chimney. The tunnels are 10 μm wide, 1 μm tall, and either 4 μm or 25 μm long. The chimneys are 4 μm tall and 40 μm in diameter. The insulation layer is comprised of either 4 μm of Parylene-C or 1 μm of low-stress silicon-nitride.

5.2.2.1 Electrodes

The laser tweezers limit the size of the electrodes and electrode leads. As the laser tweezers pass over the metal leads the power is attenuated. If too much power is attenuated, the neuron will no longer be trapped in the laser beam. It would be extremely inefficient to have to reacquire the neuron in the laser beam each time an electrode lead is crossed, especially if there are large numbers of neurons or electrodes. The maximum electrode lead width across which the laser tweezers can successfully carry a neuron is 15 μm. The electrode inside the neurocage is 10 μm in diameter with a 10 μm diameter via. The center of the electrode is offset from the center of the neurocage by 10 μm. The electrode is offset to provide a maximal area in the neurocage in which to place the neuron without the electrode interfering with the laser tweezers and causing the neuron to be dropped prematurely outside the neurocage. In addition, once the electrode is platinized, the offset electrode provides a maximal area in which the neuron can grow away from the platinized electrode. The electrode lead extends out underneath one of the anchors. The electrode leads remain 8 μm wide until they are approximately 100–200 μm away from the neurocage at which point they will no longer interfere with the laser tweezers. At that point, the electrode lead width increases to 20 μm wide. The electrode leads are between 4 mm and 10 mm long, depending on the location of the specific neurocage and its associated bonding pad. The bonding pads are 500 μm x 500 μm, with an opening 450 μm x 450 μm. The bonding pads are spaced to allow either wire bonding or bump bonding.

This design has 60 neurocages, each with its own electrode. The electrodes cover an area 1 cm x 2 cm. Fig. 5-3 shows the electrode layout. The electrodes are not symmetrical on the chip because two separate regions must be created to successfully load the neurons.

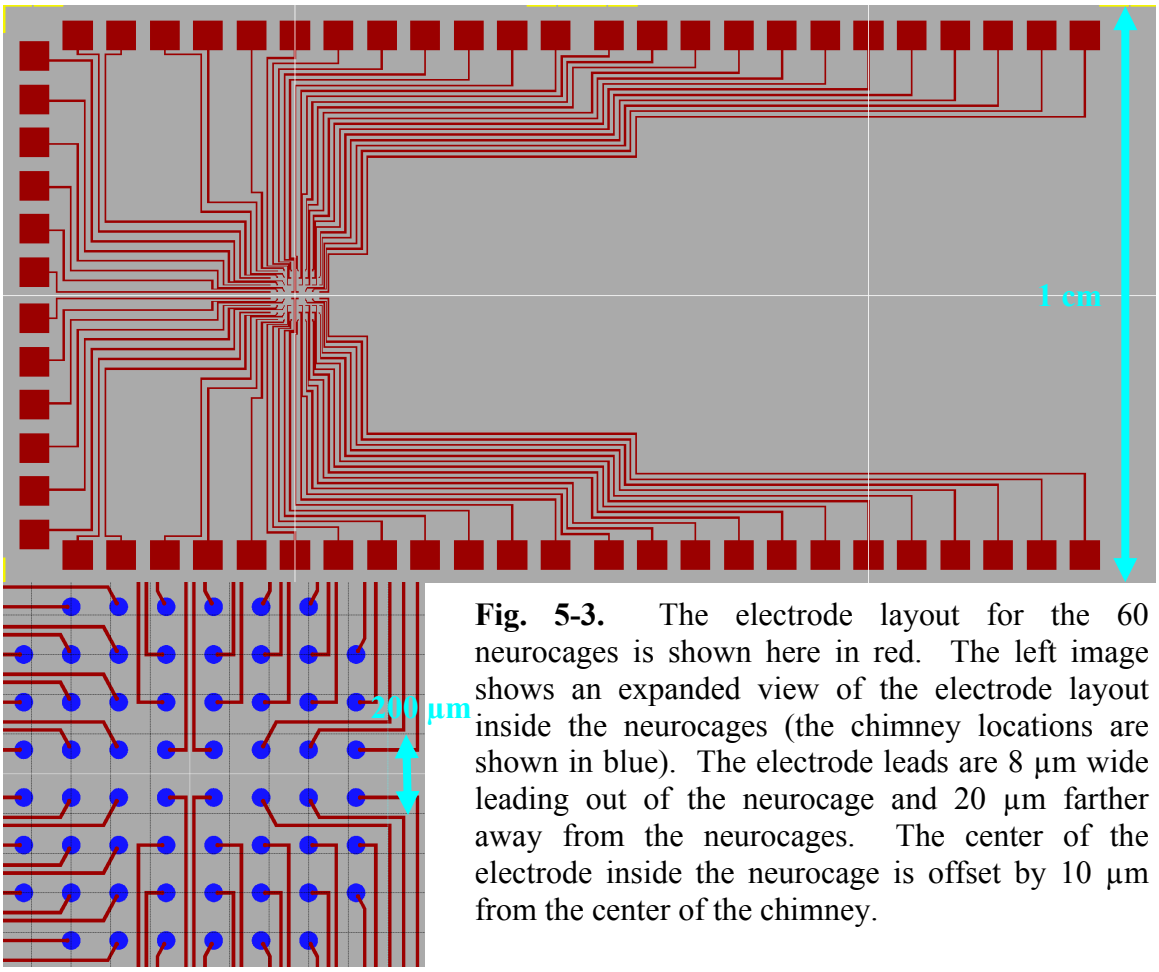


Fig. 5-3. The electrode layout for the 60 neurocages is shown here in red. The left image shows an expanded view of the electrode layout inside the neurocages (the chimney locations are shown in blue). The electrode leads are 8 µm wide leading out of the neurocage and 20 µm farther away from the neurocages. The center of the electrode inside the neurocage is offset by 10 µm from the center of the chimney.

First, a non-adhesive region must be created on which neurons can be placed to await transport to the neurocage by the laser tweezers. The electrode leads are kept out of this region to make it easier to find and trap individual neurons. Secondly, the neurocages and surrounding area must be made adhesive to ensure the neurons will successfully attach to the substrate and grow.

5.2.2.2 Anchors

Other than simply handling the glass slides, the other major problem concerns the anchors. The standard DRIE process, described in Section 3.1.1, used to etch anchors in

silicon does not etch glass. As the Parylene-C does not adhere to the glass any better than it does to the silicon, another anchoring method must be developed.

The inverted mushroom structure is ideal for anchoring the Parylene-C to the substrate. The goal is to recreate this structure in the glass. The common etchants for glass, such as HF or CF_4 plasma, are isotropic. They are sufficient to create the mushroom cap but not the stalk of the mushroom. Either an anisotropic etchant for glass must be found to create the mushroom stalk or another material, which can be etched anisotropically, must be placed on top of the glass.

To pursue the latter solution, Parylene-C was chosen as the new structural material for the anchors. First, a thin layer of Parylene-C is deposited on the glass slides. This layer is then baked in a nitrogen (N_2) atmosphere at 350°C. (The N_2 atmosphere ensures the Parylene-C does not get oxidized and turn brown.) This temperature is above the melting temperature for Parylene-C, thus causing it to melt and re-crystallize [30]. The resulting Parylene-C is very brittle and is fused to the glass. Fortunately, the Parylene-C can still be etched by O_2 plasma, although the re-crystallization causes the density to increase which decreases the etching rate of the Parylene-C by about 50%. The mushroom stalk is then created by etching the Parylene-C with O_2 plasma. Although the Parylene-C etching is not anisotropic, this is not critical since the Parylene-C is thin. Once the Parylene-C has been etched, the mushroom cap is created by etching the glass out from underneath the Parylene-C with HF (Fig. 5-4). Since the Parylene-C has been hardened, it will remain rigid and freestanding when the glass is etched out from underneath. With this technique a short inverted mushroom structure can be created to anchor the Parylene-C.

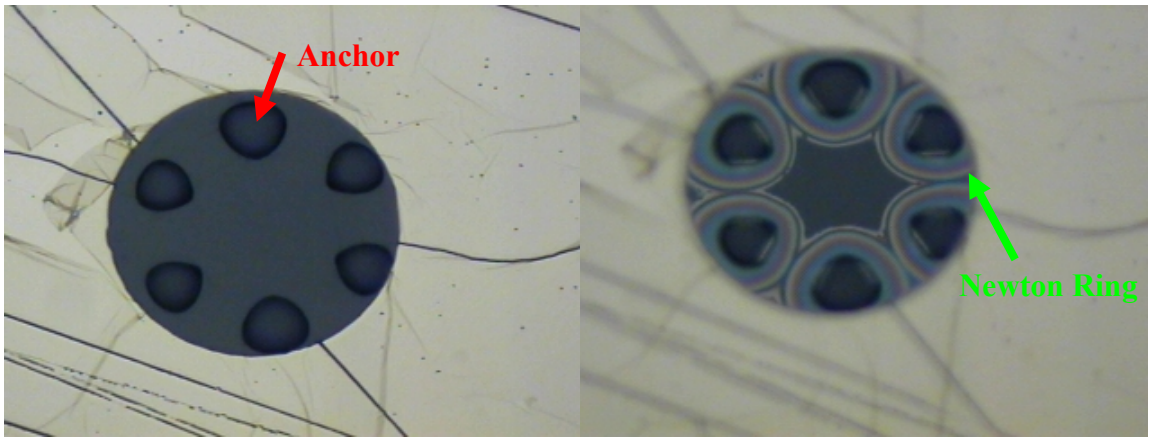
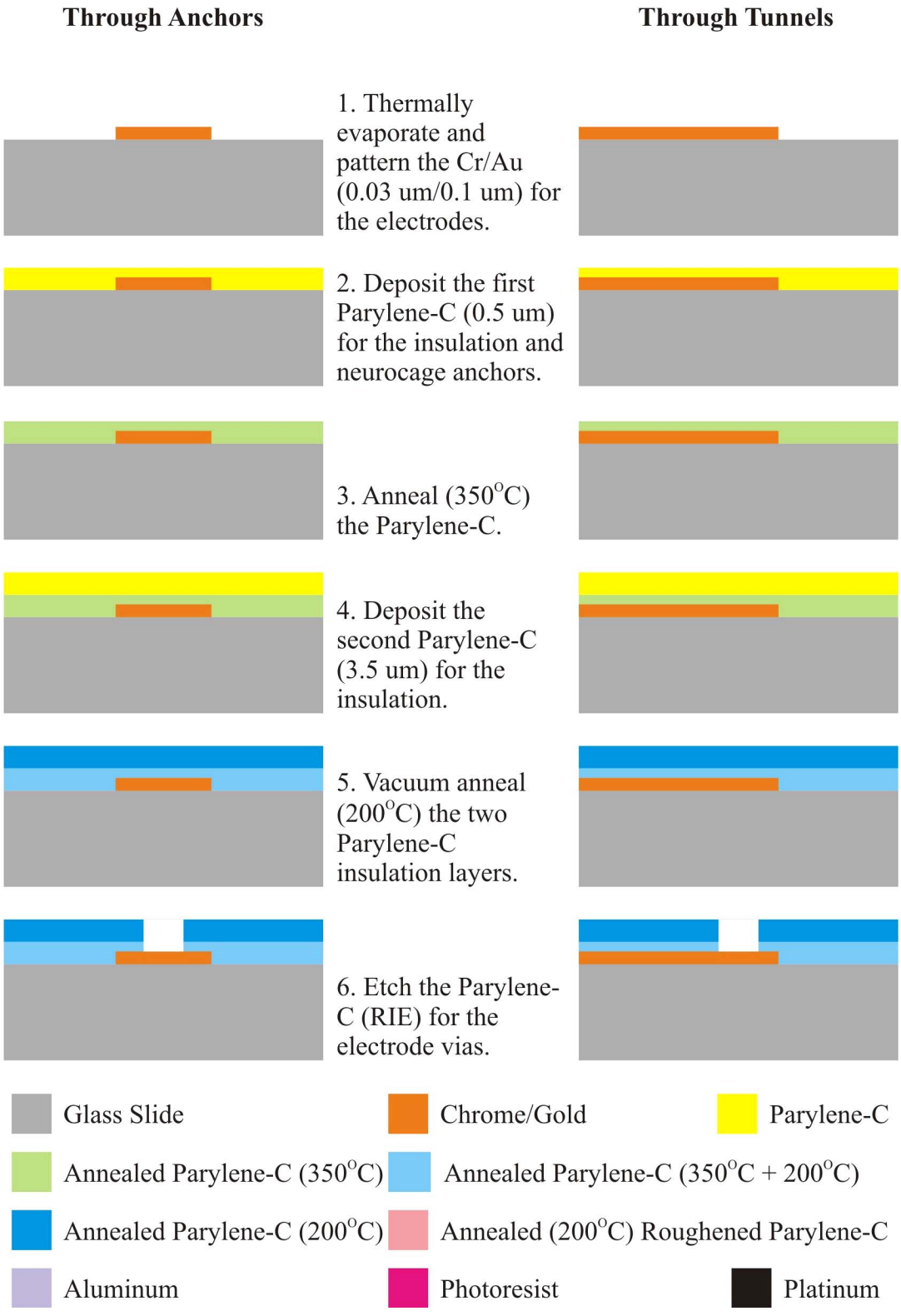


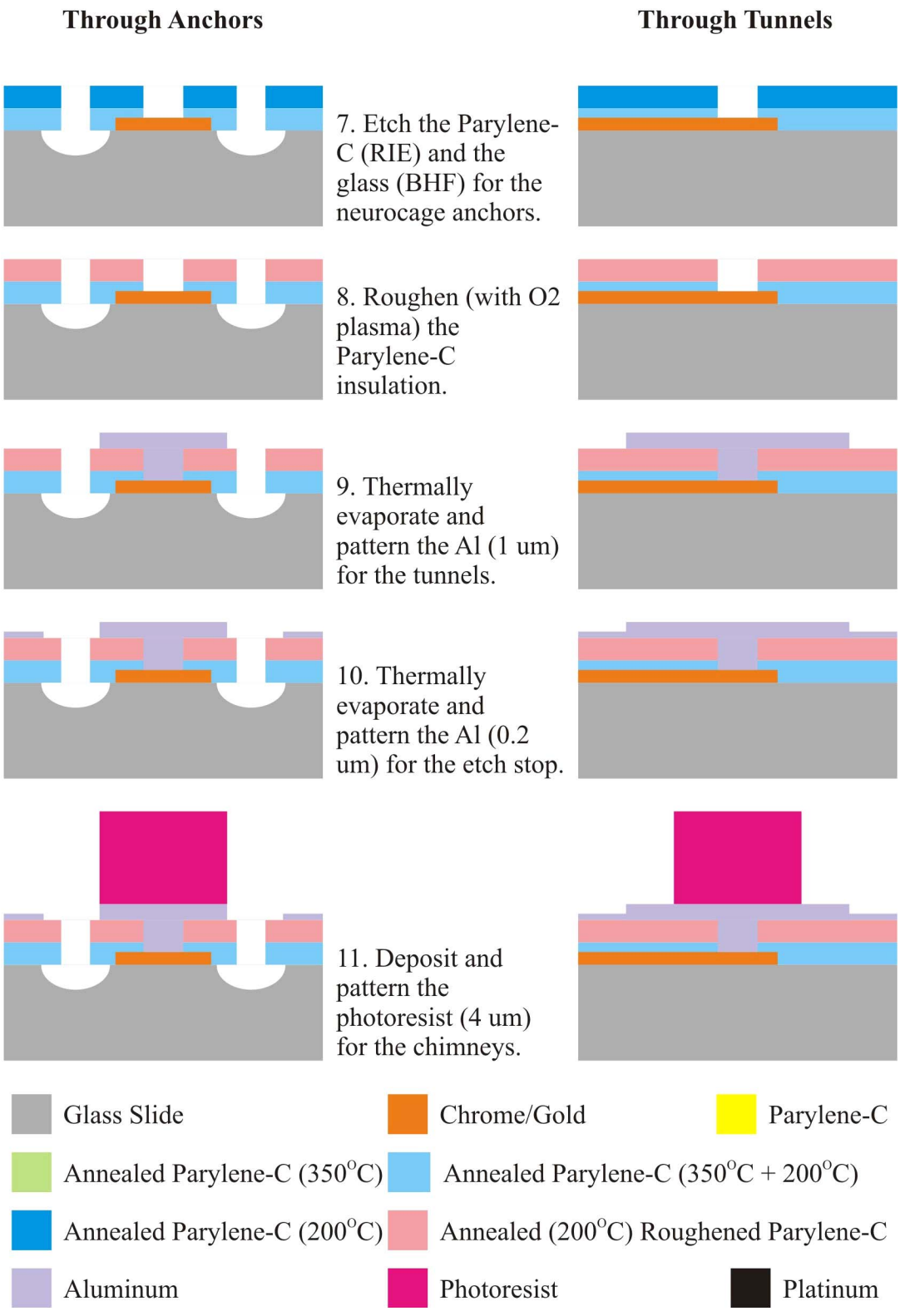
Fig. 5-4. The left image shows the 6 anchors (one of which is indicated by the red arrow) for the neurocage after the openings have been etched in the molten Parylene-C. The right image shows the 6 anchors after the glass has been etched out from underneath the molten Parylene-C, as evidenced by the Newton rings, to create the inverted mushroom structure. The green arrow shows one of the Newton rings created by the air gap underneath the Parylene-C indicating the glass has been etched.

5.2.3 Fabrication with Parylene-C Insulation

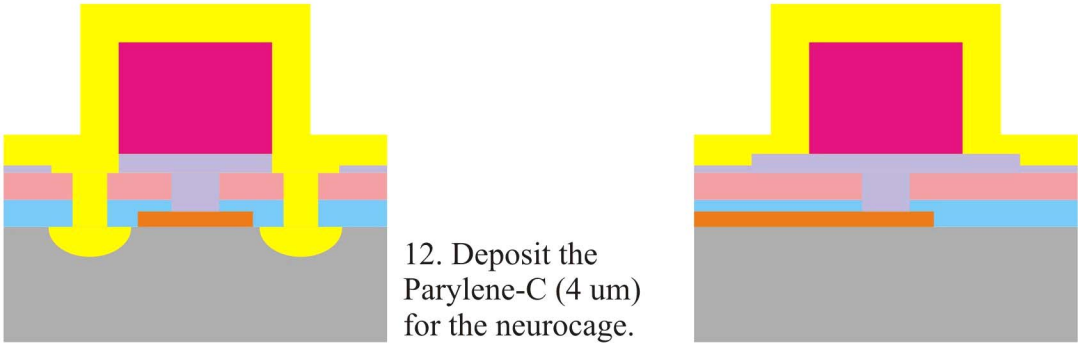
The fabrication procedure for using Parylene-C for insulation is outlined in Fig. 5-5 [48–50, 57]. (The complete details can be found in Appendix IV.)

The first step is to thoroughly clean the glass slide. The glass slide is heated to 400°C for 2 hours in ambient air. Next, the glass slide is treated with high-powered O_2 plasma for 5 minutes. Finally, the glass slide is cleaned in piranha at 120°C for 10 minutes. These steps ensure the glass slides are free of potential contaminants and are hydrophilic so that the metal electrodes adhere well.

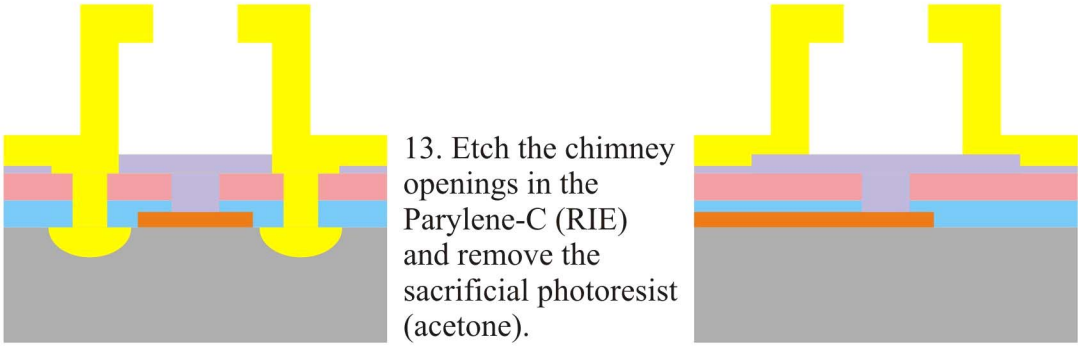

Through Anchors
Through Tunnels
1. Thermally evaporate and pattern the Cr/Au (0.03 um/0.1 um) for the electrodes.
2. Deposit the first Parylene-C (0.5 um) for the insulation and neurocage anchors.
3. Anneal (350°C) the Parylene-C.
4. Deposit the second Parylene-C (3.5 um) for the insulation.
5. Vacuum anneal (200°C) the two Parylene-C insulation layers.
6. Etch the Parylene-C (RIE) for the electrode vias.
Glass Slide
Chrome/Gold
Parylene-C
Annealed Parylene-C (350°C)
Annealed Parylene-C (350°C + 200°C)
Annealed Parylene-C (200°C)
Annealed (200°C) Roughened Parylene-C
Aluminum
Photoresist
Platinum


Through Anchors
Through Tunnels
7. Etch the Parylene-C (RIE) and the glass (BHF) for the neurocage anchors.
8. Roughen (with O2 plasma) the Parylene-C insulation.
9. Thermally evaporate and pattern the Al (1 um) for the tunnels.
10. Thermally evaporate and pattern the Al (0.2 um) for the etch stop.
11. Deposit and pattern the photoresist (4 um) for the chimneys.
Glass Slide
Chrome/Gold
Parylene-C
Annealed Parylene-C (350°C)
Annealed Parylene-C (350°C + 200°C)
Annealed Parylene-C (200°C)
Annealed (200°C) Roughened Parylene-C
Aluminum
Photoresist
Platinum

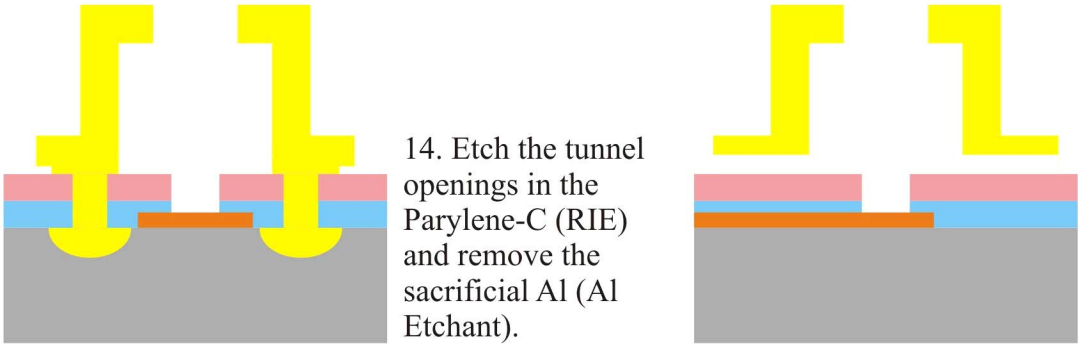
Through Anchors **Through Tunnels**



12. Deposit the Parylene-C (4 um) for the neurocage.



13. Etch the chimney openings in the Parylene-C (RIE) and remove the sacrificial photoresist (acetone).



14. Etch the tunnel openings in the Parylene-C (RIE) and remove the sacrificial Al (Al Etchant).

Glass Slide
Chrome/Gold
Parylene-C
Annealed Parylene-C (350^{o}C)
Annealed Parylene-C (350^{o}C + 200^{o}C)
Annealed Parylene-C (200^{o}C)
Annealed (200^{o}C) Roughened Parylene-C
Aluminum
Photoresist
Platinum

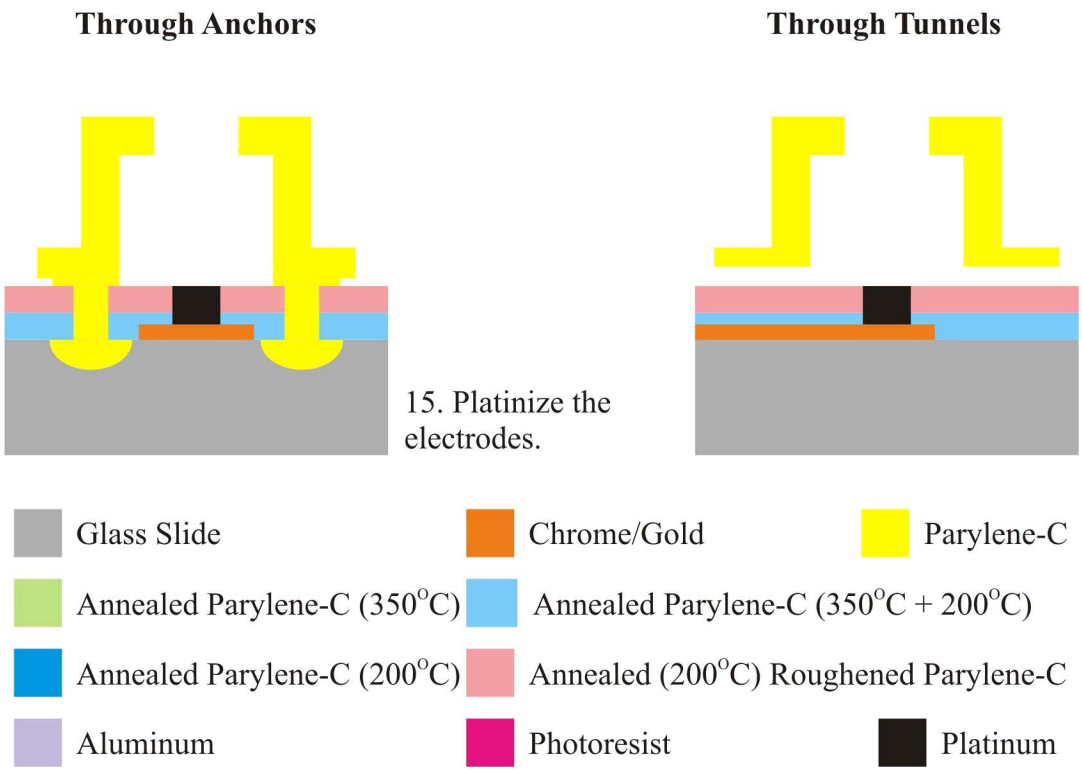


Fig. 5-5. Process flow for the neurocages on glass with Parylene-C insulation, sacrificial aluminum for the tunnels, and sacrificial soft-baked photoresist for the chimneys. (Not drawn to scale)

The glass slide is attached to the wafer with photoresist and baked at 100°C for 10 minutes. This ensures the glass slide is firmly attached and that no water remains on the surface. The glass slide is then treated with HMDS for 1 minute. A layer of photoresist, approximately 4 µm thick, is then spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the electrodes. The wafer is treated briefly with O_2 plasma to ensure all of the photoresist has been removed. Next, 0.01 µm of chrome is thermally evaporated, followed by 0.3 µm of gold. The chrome is used as an adhesion layer between the glass slide and the gold. The photoresist underneath the undesired metal is then dissolved in acetone with ultrasonic agitation, leaving only the chrome/gold for the electrodes on the surface (Fig. 5-6). This acetone also releases the glass slide from the silicon wafer.

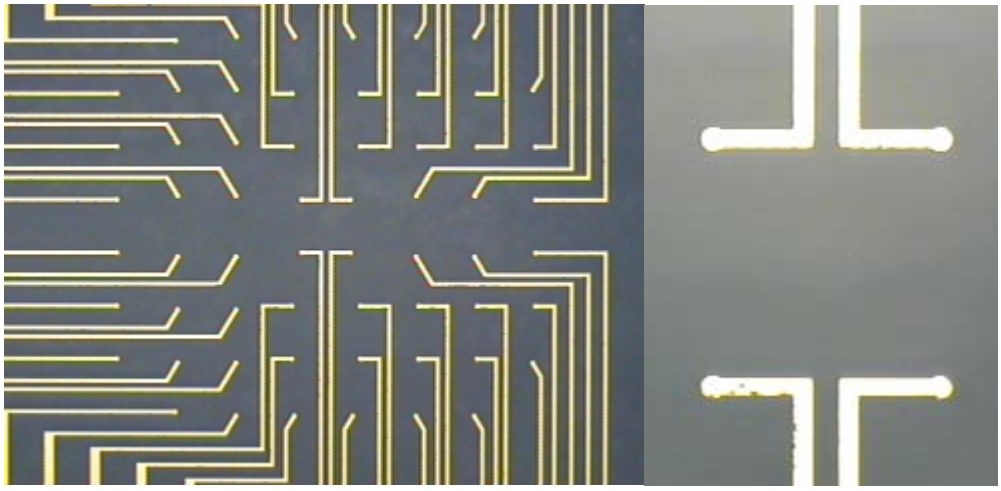


Fig. 5-6. Optical images of the chrome/gold electrodes for the neurocages. The left image shows the electrodes for the array of 60 neurocages. The right image shows a close-up of the electrodes for the 4 neurocages in the center.

The first layer of Parylene-C (0.5 μm thick), used to create the inverted mushroom for the anchors, is then deposited. (The glass slide does not need to be attached to the wafer for these steps.) The Parylene-C is then annealed at 350°C for 2 hours in a N_2 atmosphere. This melts and hardens the Parylene-C, firmly adhering it to the glass. Unfortunately, this also can cause small cracks in the Parylene-C, making it unsuitable, by itself, for insulation. Therefore, if Parylene-C is the desired insulation material, a second layer of Parylene-C, 3.5 μm thick (for a total insulation thickness of 4 μm), is deposited which will fill in any potential cracks in the first layer of Parylene-C. (This second Parylene-C deposition and subsequent annealing are not necessary if silicon-nitride is used as the insulation material.) To ensure the two Parylene-C layers adhere well to each other, the glass slide is then annealed at 200°C for 48 hours in a vacuum oven with a N_2 backfill.

The glass slide is again attached to the wafer with photoresist and baked at 100°C for 5 minutes. A layer of photoresist, approximately 15 μm thick, is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for

the electrode vias. The electrode vias are opened in the Parylene-C using O_2 plasma in the Reactive-Ion Etcher (RIE). The Parylene-C is not etched in the DRIE or the standard plasma etcher, as is the case for the neurocages on silicon, because the vacuum pumps on those machines can cause the glass slides attached to the wafer to shatter. This is most likely caused by pockets of air between the glass slide and the wafer which cause a pressure buildup when a sudden drastic vacuum change is applied. The RIE machine, with a slower pump-down time, does not cause the glass slides to shatter. Once the electrode vias are etched, the photoresist is stripped and the glass slide is removed from the wafer using ST-22 Stripper.

Once again, the glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes. A layer of photoresist, approximately 15 µm thick, is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the anchors. The neurocage anchors are etched open in the Parylene-C with O_2 plasma in the RIE. The glass underneath the Parylene-C is then etched out using BHF to

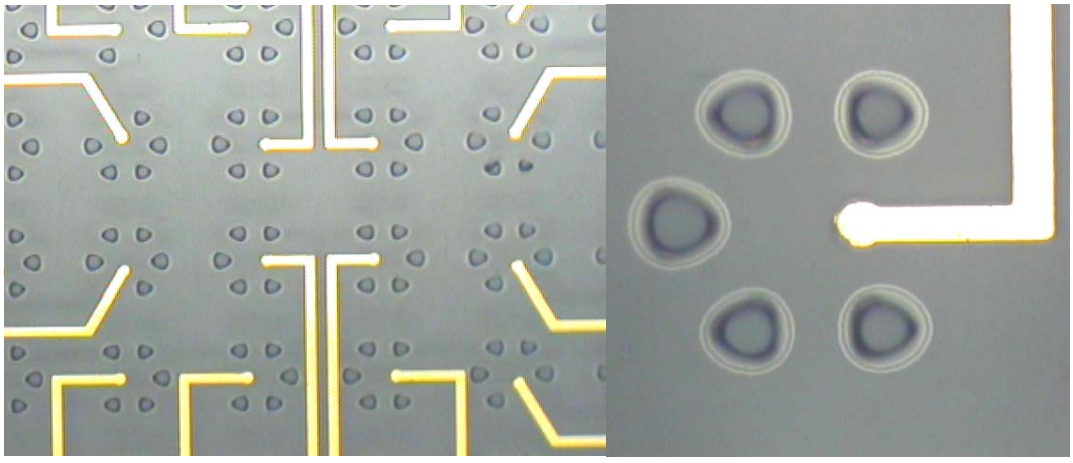


Fig. 5-7. Optical images of the neurocage anchors etched through the Parylene-C insulation and into the glass. The left image shows a section of the array. The right image shows a close-up of the electrode and anchors for a single neurocage. The Newton rings around anchors indicate the glass underneath the Parylene-C has been etched, forming the desired inverted mushroom structure.

create the inverted mushroom structure (Fig. 5-7). The photoresist is stripped and the glass slide is removed in ST-22 Stripper.

Next, the Parylene-C is treated with very low-powered O_2 plasma for 30 seconds. This roughens the Parylene-C slightly and puts hydroxyl groups on the Parylene-C surface. Untreated Parylene-C is very hydrophobic, and this ensures the surface is hydrophilic so that the subsequent layers of aluminum properly adhere. (The glass slide does not need to be attached to the wafer for this step.)

The glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes. A 4 μm thick layer of photoresist is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the tunnels. 1 μm of aluminum is thermally evaporated, in two consecutive depositions. The photoresist underneath the undesired aluminum is lifted off in acetone with ultrasonic agitation, leaving only the aluminum for the tunnels (Fig. 5-8). The acetone also removes the glass slide from the wafer.

Yet again, the glass slide is attached to the wafer with photoresist and baked at 100°C

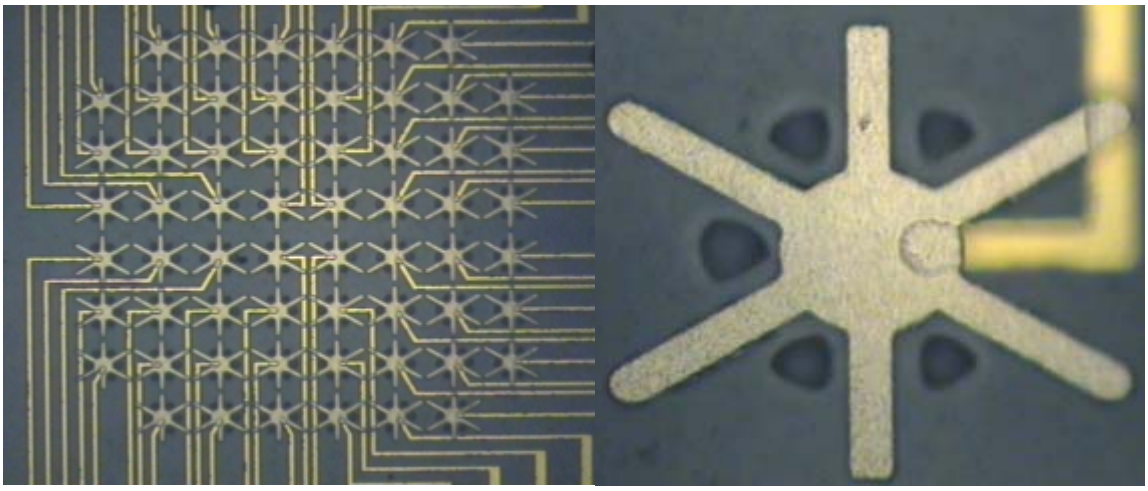


Fig. 5-8. Optical images of neurocages on glass with Parylene-C insulation. The left image shows the aluminum tunnels for the array of 60 neurocages. The right image is a closeup of the aluminum tunnels for one neurocage.

for 5 minutes. A 4 μm thick layer of photoresist is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to define the areas where the aluminum etch stop will be deposited. Next, 0.2 μm of aluminum is thermally evaporated. The photoresist and the unwanted aluminum are lifted off in acetone with ultrasonic agitation, leaving only the aluminum etch stop (Fig. 5-9). The glass slide is also removed from the wafer in the acetone.

Once the glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes, the 4 μm thick layer of photoresist for the chimneys is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to define the chimneys (Fig. 5-10). The glass slide is not removed from the wafer at this step, as anything used to dissolve the photoresist between the glass slide and the wafer would also dissolve the chimney photoresist. Next, the 4 μm of Parylene-C to form the neurocage is deposited.

A 15 μm thick layer of photoresist is spun onto the wafer and soft-baked at 90°C for 40 minutes. (The glass slide is still attached to the wafer from the previous step.) The photoresist is exposed and developed to form the chimney openings. The Parylene-C is

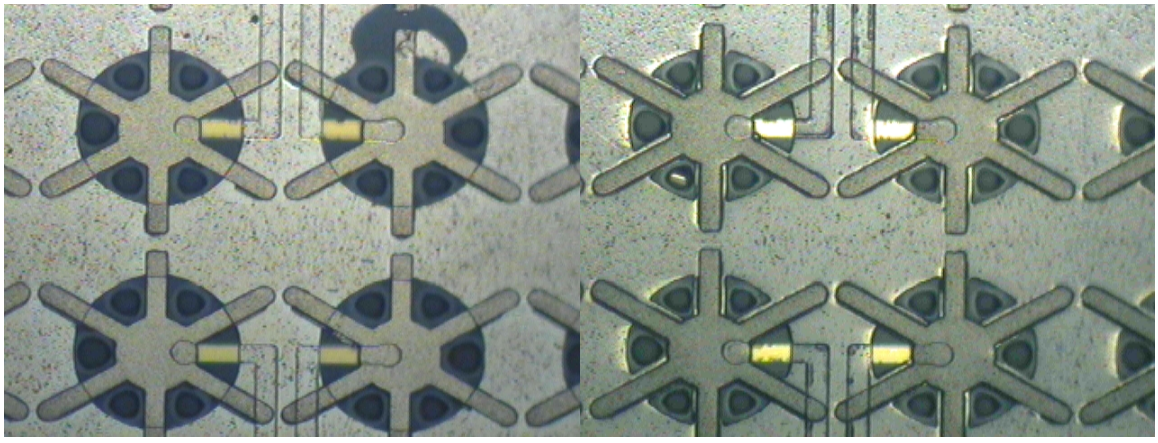


Fig. 5-9. Optical images of neurocages on glass with Parylene-C insulation. The left image shows neurocages with the aluminum tunnels and etch stop with 25 μm long tunnels. The right image shows neurocages with aluminum tunnels and etch stop with 4 μm long tunnels.

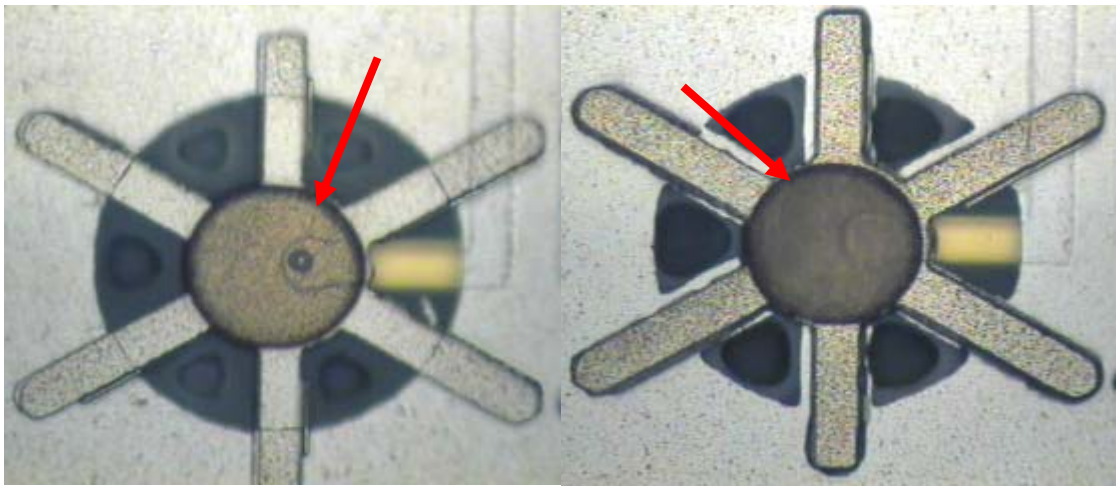


Fig. 5-10. Optical images of neurocages on glass with Parylene-C insulation. These images show the photoresist chimney (denoted by the red arrows) after deposition and patterning. The neurocage on the left has 25 μm long tunnels and the neurocage on the right has 4 μm long tunnels.

etched in O_2 plasma in the RIE to open the chimneys. The photoresist, including both the photoresist underneath the Parylene-C forming the chimneys and the photoresist attaching the glass slide to the wafer, is removed in ST-22 Stripper.

The glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes. 15 μm of photoresist is spun on and soft-baked at 85°C for 45 minutes. The photoresist is exposed and developed to create the tunnel openings. The Parylene-C is etched with O_2 plasma in the RIE to open the tunnels.

Finally, the photoresist is stripped and the glass slide is removed from the wafer in acetone. The aluminum for the tunnels and the etch stop layer is etched in Aluminum Etchant Type A at 60°C. Optical images and SEMs of the final neurocages are shown in Figs. 5-11 and 5-12, respectively.

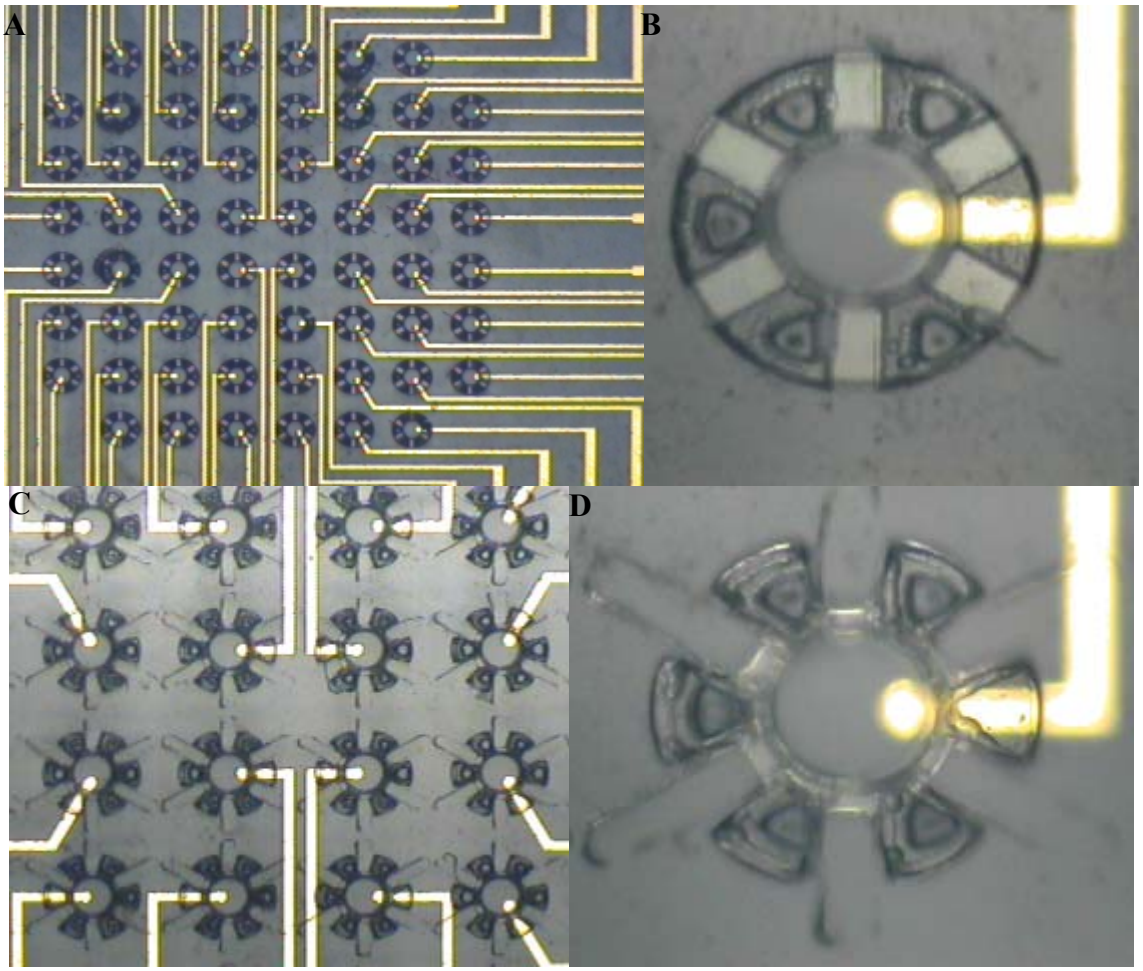
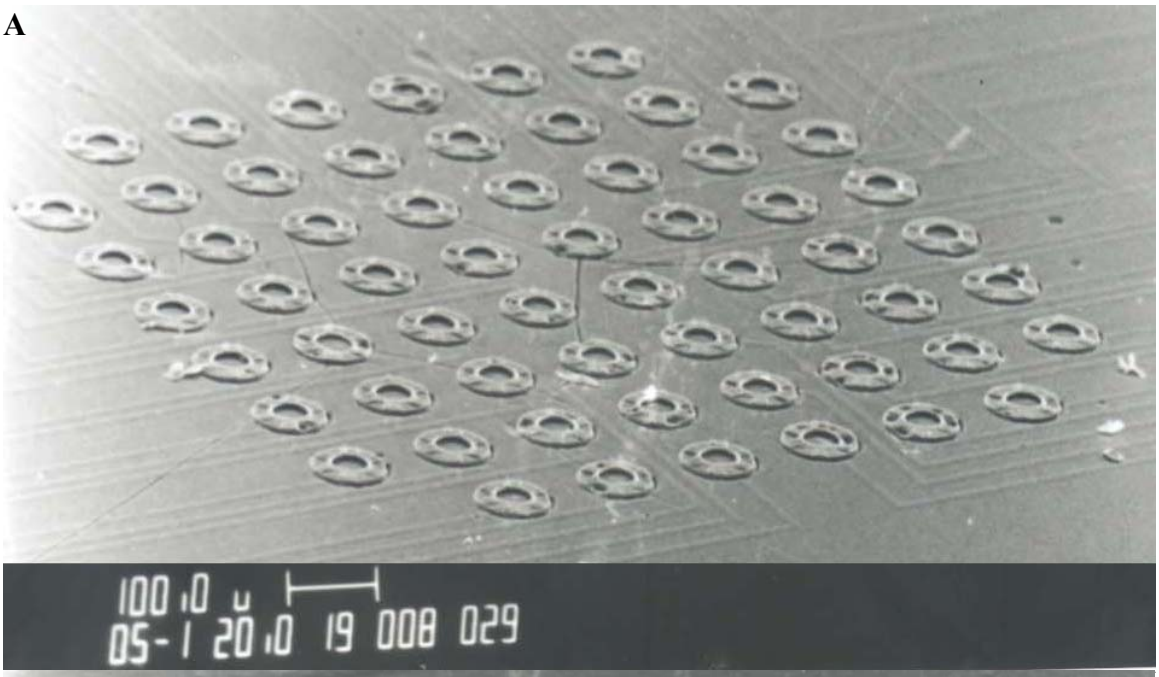
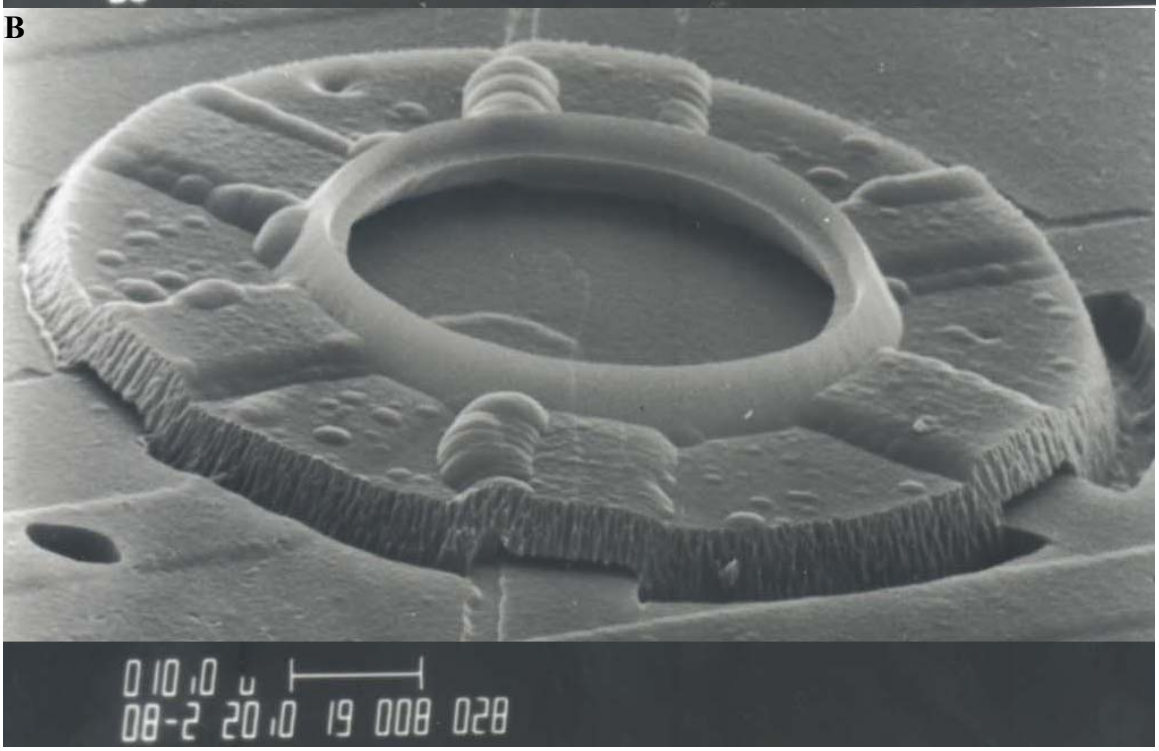


Fig. 5-11. Optical images of final cleaned neurocages on glass with Parylene-C insulation. Figs. **A** and **B** show neurocages with 25 µm long tunnels. Figs. **C** and **D** show neurocages with 4 µm long tunnels. Fig. **A** shows the entire array of 60 neurocages. Fig. **C** shows a closeup of the central neurocages within the array. Figs. **B** and **D** show close-ups of individual neurocages.

A



B



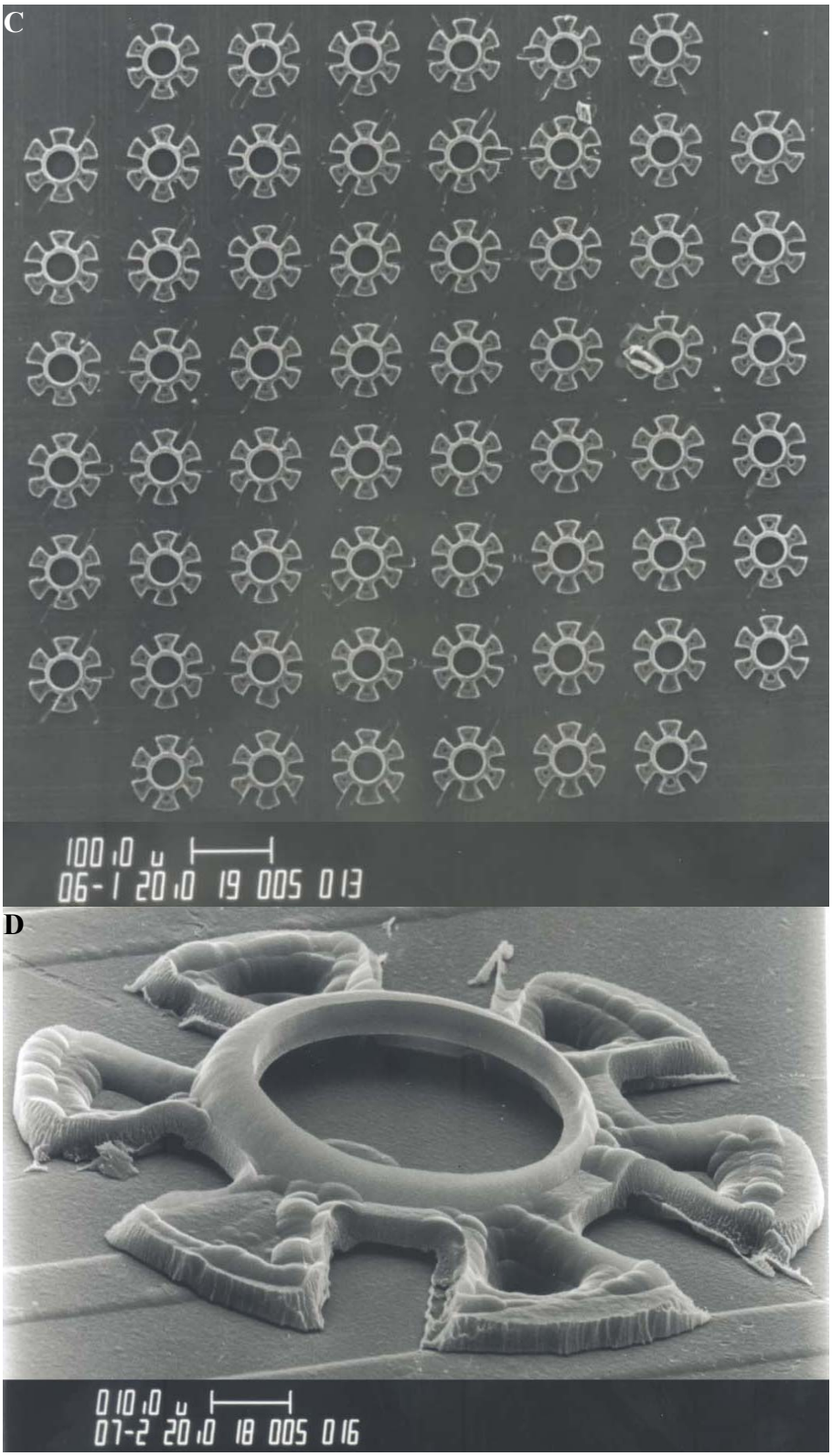


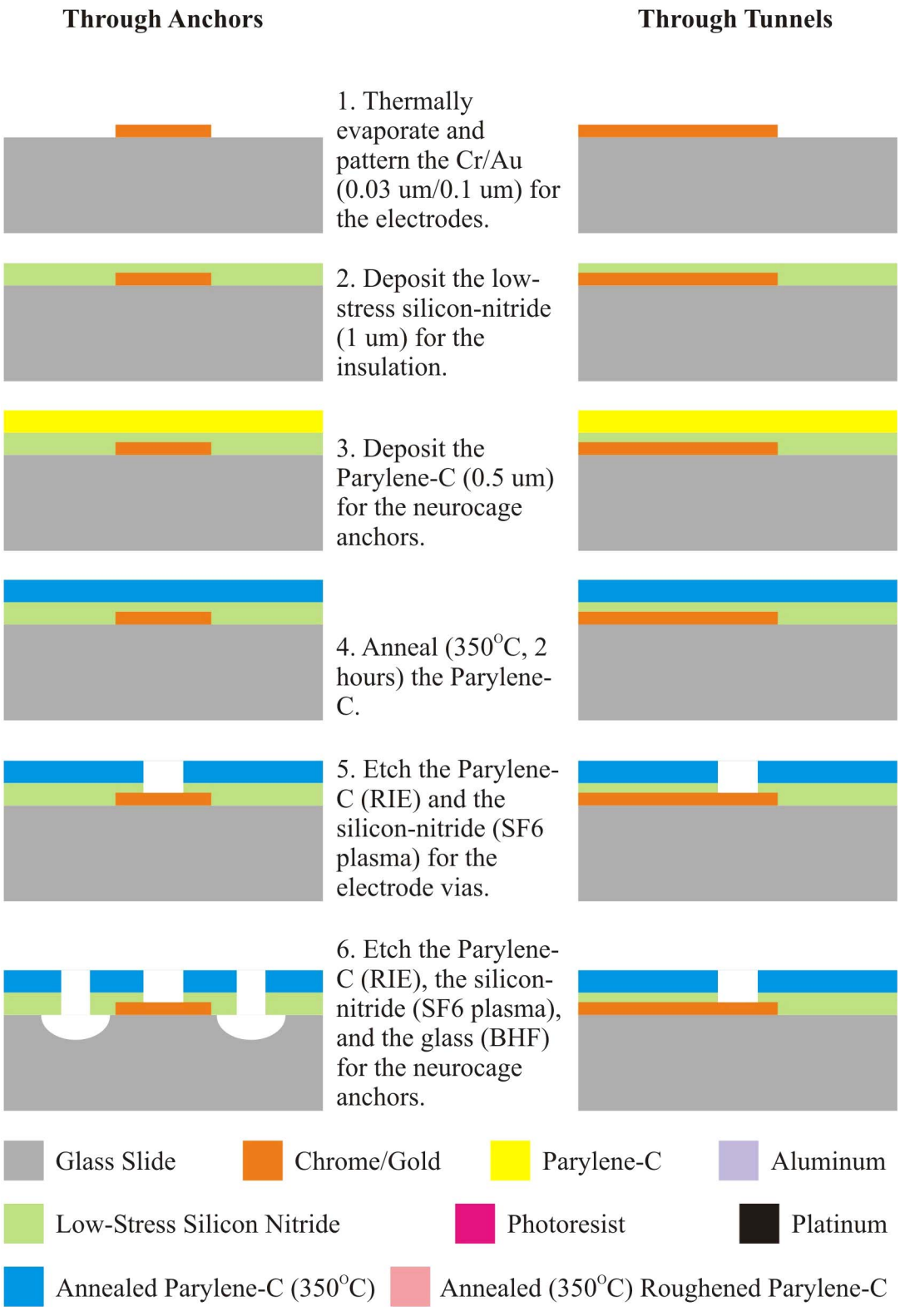
Fig. 5-12. SEMs of neurocage on glass with Parylene-C insulation. Figs. **A** and **B** show neurocages with 25 μm long tunnels. Figs. **C** and **D** show neurocages with 4 μm long tunnels.

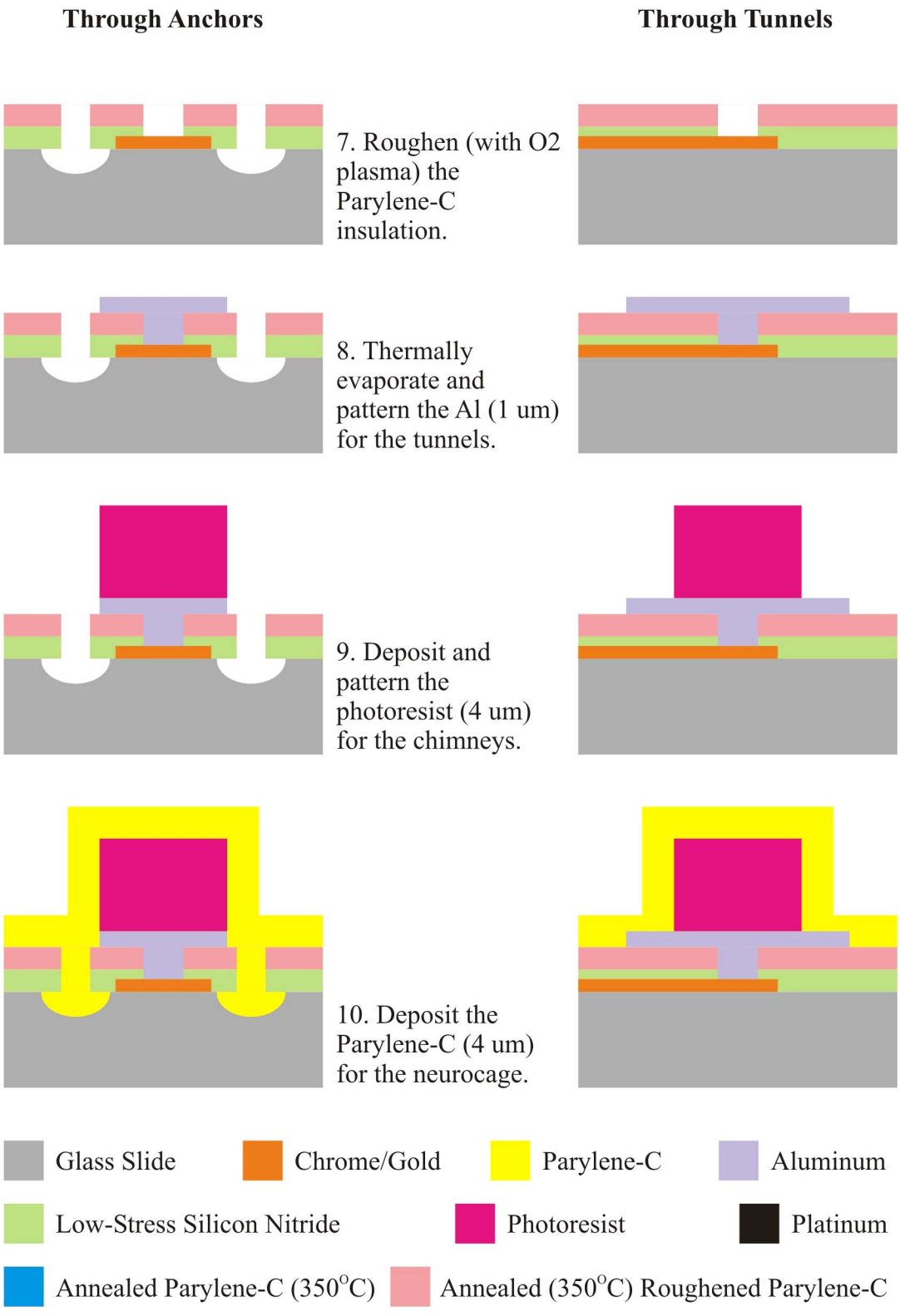
5.2.4 Fabrication with Low-Stress Silicon-Nitride Insulation

The fabrication process for using low-stress silicon-nitride as the insulation is similar to that for Parylene-C insulation, although several steps can be eliminated. The outline of the process flow can be found in Fig. 5-13 [48–50, 57]. (The complete details can be found in Appendix V.)

As described in the previous section, the glass slides are first cleaned and then the electrodes are thermally evaporated and patterned. Next, 1 μm of low-stress silicon-nitride is deposited using a plasma-enhanced chemical vapor deposition.

Ideally, the anchors would be created using the same procedure outlined in Section 5.2.2.2, with the low-stress silicon-nitride replacing melted Parylene-C layer. However, the BHF used to etch the glass out from underneath the Parylene-C to form the mushroom cap would also etch the silicon-nitride, destroying the mushroom stalk. One alternative for creating the anchors is to use a different etchant to etch the glass out from underneath the silicon-nitride, one that does not etch silicon-nitride. Another alternative, the one chosen for this process, is to use the melted Parylene-C layer on top of the silicon-nitride. With this technique, a 0.5 μm thick layer of Parylene-C is deposited and then annealed at 350°C for 2 hours in a N_2 atmosphere. (The glass slide does not need to be attached to the wafer for this step.) By the end of the fabrication process, however, the Parylene-C will have been removed everywhere except under the neurocage, where it serves as the structural mechanism for the anchors.


Through Anchors
Through Tunnels
1. Thermally evaporate and pattern the Cr/Au (0.03 um/0.1 um) for the electrodes.
2. Deposit the low-stress silicon-nitride (1 um) for the insulation.
3. Deposit the Parylene-C (0.5 um) for the neurocage anchors.
4. Anneal (350°C, 2 hours) the Parylene-C.
5. Etch the Parylene-C (RIE) and the silicon-nitride (SF6 plasma) for the electrode vias.
6. Etch the Parylene-C (RIE), the silicon-nitride (SF6 plasma), and the glass (BHF) for the neurocage anchors.
Glass Slide
Chrome/Gold
Parylene-C
Aluminum
Low-Stress Silicon Nitride
Photoresist
Platinum
Annealed Parylene-C (350°C)
Annealed (350°C) Roughened Parylene-C


Through Anchors
Through Tunnels
7. Roughen (with O2 plasma) the Parylene-C insulation.
8. Thermally evaporate and pattern the Al (1 um) for the tunnels.
9. Deposit and pattern the photoresist (4 um) for the chimneys.
10. Deposit the Parylene-C (4 um) for the neurocage.
Glass Slide
Chrome/Gold
Parylene-C
Aluminum
Low-Stress Silicon Nitride
Photoresist
Platinum
Annealed Parylene-C (350°C)
Annealed (350°C) Roughened Parylene-C

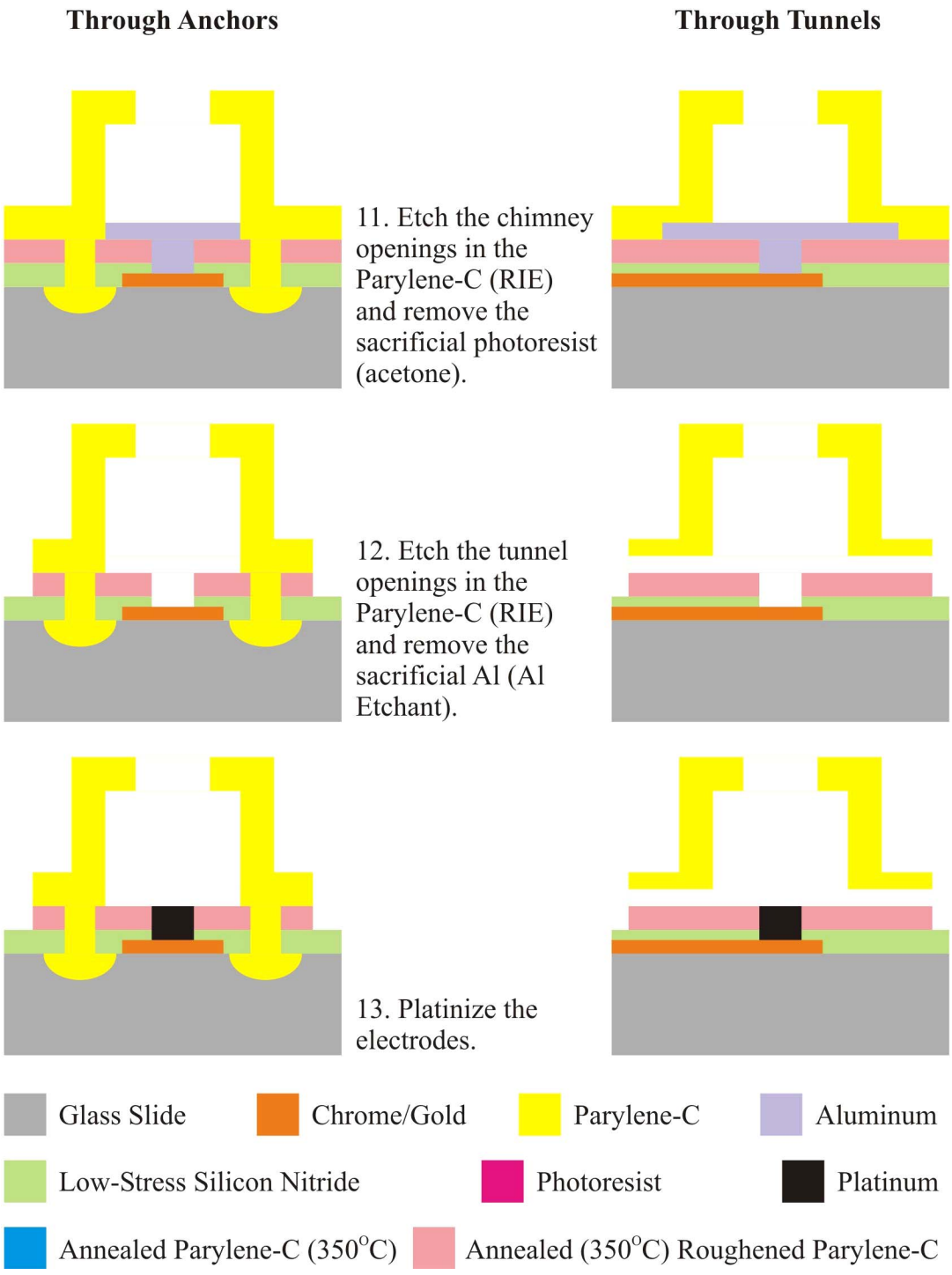


Fig. 5-13. Process flow for the neurocages on glass with low-stress silicon-nitride insulation, sacrificial aluminum for the tunnels, and sacrificial soft-baked photoresist for the chimneys. (Not drawn to scale)

Next, the glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes. A layer of photoresist, approximately 15 μm thick, is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the electrode vias. The electrode vias are first opened in the Parylene-C using O_2 plasma in the RIE. The vias are then opened in the silicon-nitride using SF_6 plasma in the RIE. Once the electrode vias are etched, the photoresist is stripped and the glass slide is removed from the wafer using heated ST-22 Stripper.

Once again, the glass slide is attached to the wafer with photoresist and baked at 100°C for 5 minutes. A layer of photoresist, approximately 15 μm thick, is spun on and soft-baked at 100°C for 30 minutes. The photoresist is exposed and developed to create the openings for the anchors. The neurocage anchors are first etched open in the Parylene-C with O_2 plasma and then etched open in the silicon-nitride with SF_6 plasma, both in the RIE. The glass underneath the Parylene-C is then etched out using BHF to create the inverted mushroom structure (Fig. 5-14). This BHF step also etches some of the silicon-nitride, however, the presence of the Parylene-C ensures the integrity of the inverted mushroom structure. The photoresist is stripped and the glass slide is removed in ST-22 Stripper.

The remaining fabrication steps continue as described in the previous section for the Parylene-C insulation (Fig. 5-15). The aluminum etch stop layer is not required, however, as the thin layer of Parylene-C for the anchors is not left on the surface except under the neurocage. Optical images and SEMs of the final neurocages are shown in Figs. 5-16 and 5-17, respectively.

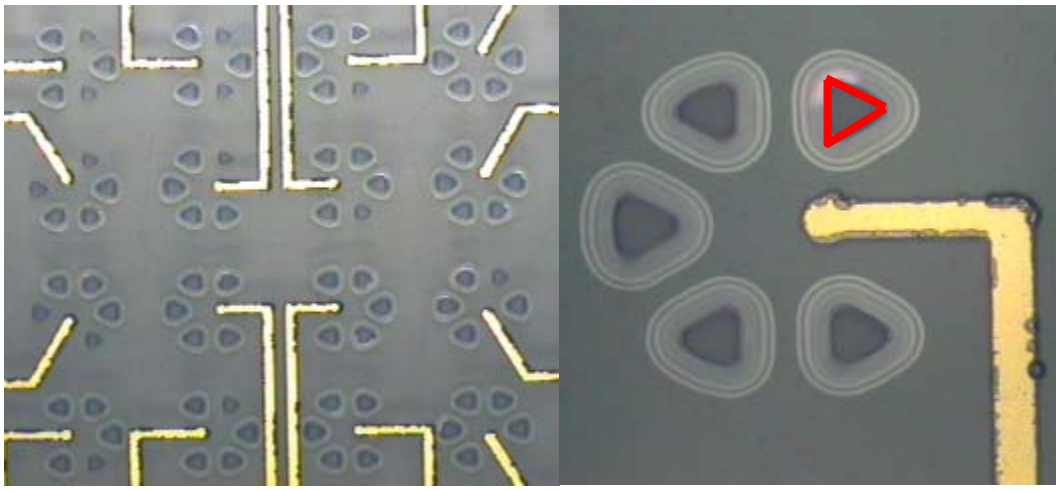


Fig. 5-14. Optical images of neurocages on glass with low-stress silicon-nitride insulation. These images show the neurocage anchors etched through the Parylene-C, the low-stress silicon-nitride, and the glass. The left image shows a closeup of the central neurocages in the array. The right image shows a closeup of a single neurocage. The triangles (one of which is outlined in red) are the openings in the Parylene-C and the low-stress silicon-nitride. The surrounding Newton rings indicate the glass underneath has been etched out to create the inverted mushroom structure.

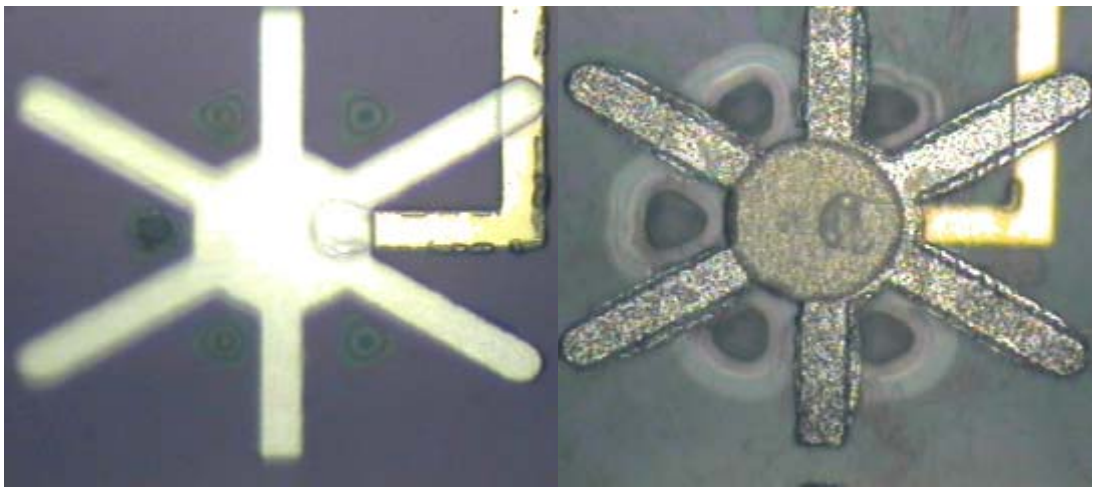


Fig. 5-15. Optical images of neurocages on glass with low-stress silicon-nitride insulation. The left image shows a closeup of the aluminum tunnels for a single neurocage. The right image shows a closeup of the soft-baked photoresist chimney for a single neurocage.

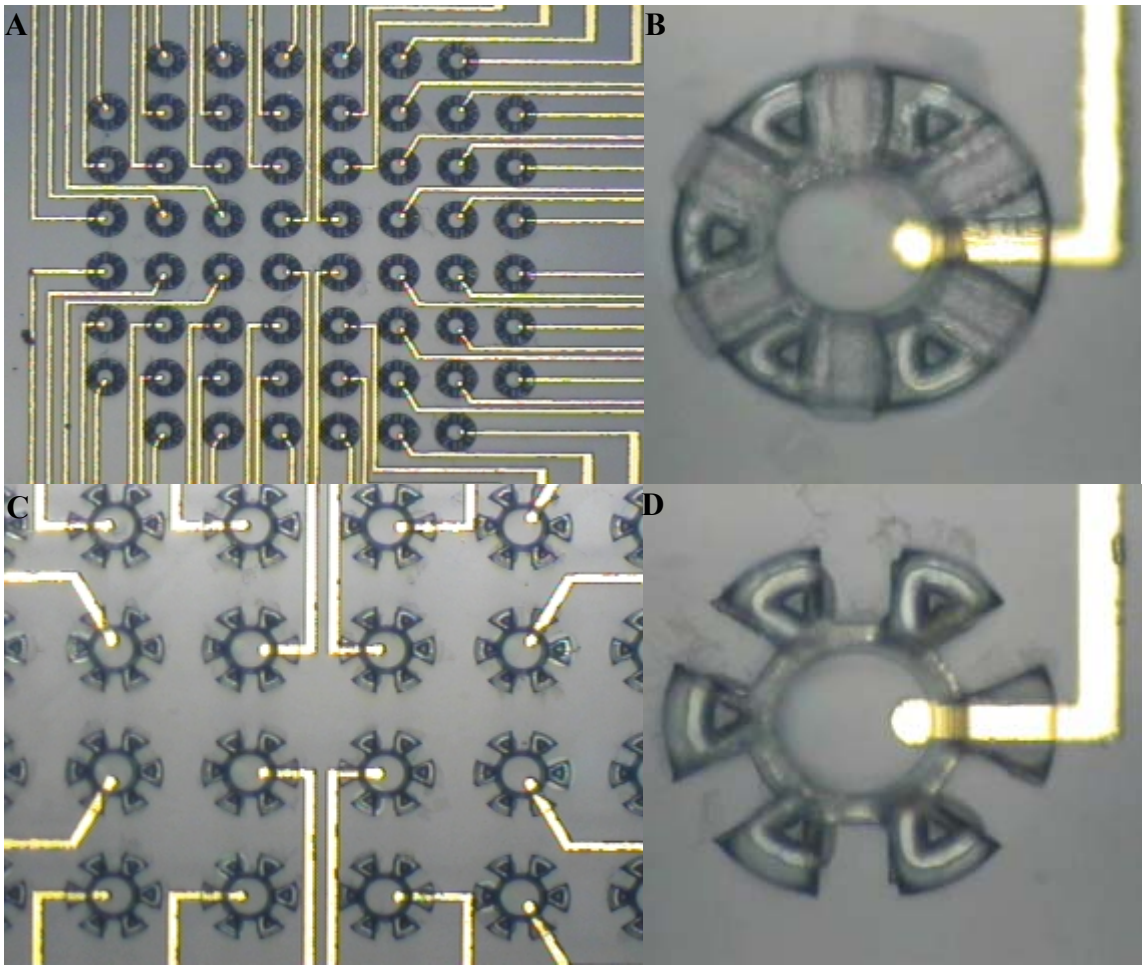
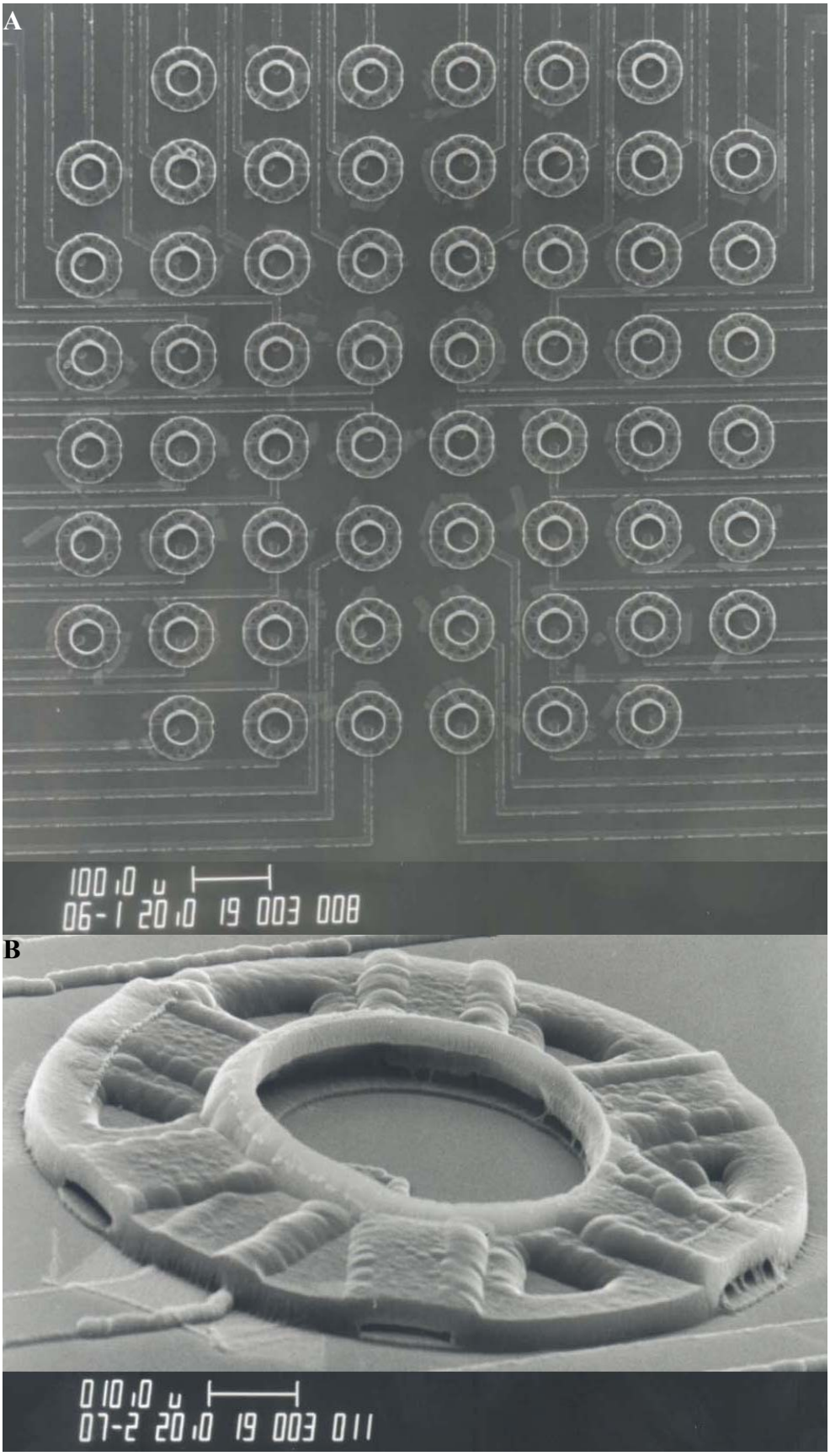


Fig. 5-16. Optical images of final cleaned neurocages on glass with low-stress silicon-nitride insulation. Figs. **A** and **B** show neurocages with 25 μm long tunnels. Figs. **C** and **D** show neurocages with 4 μm long tunnels. Fig. **A** shows the entire array of 60 neurocages. Fig. **C** shows a closeup of the central neurocages within the array. Figs. **B** and **D** show closeups of individual neurocages.


A
100.0 u
06-1 20.0 19 003 008
B
010.0 u
07-2 20.0 19 003 011

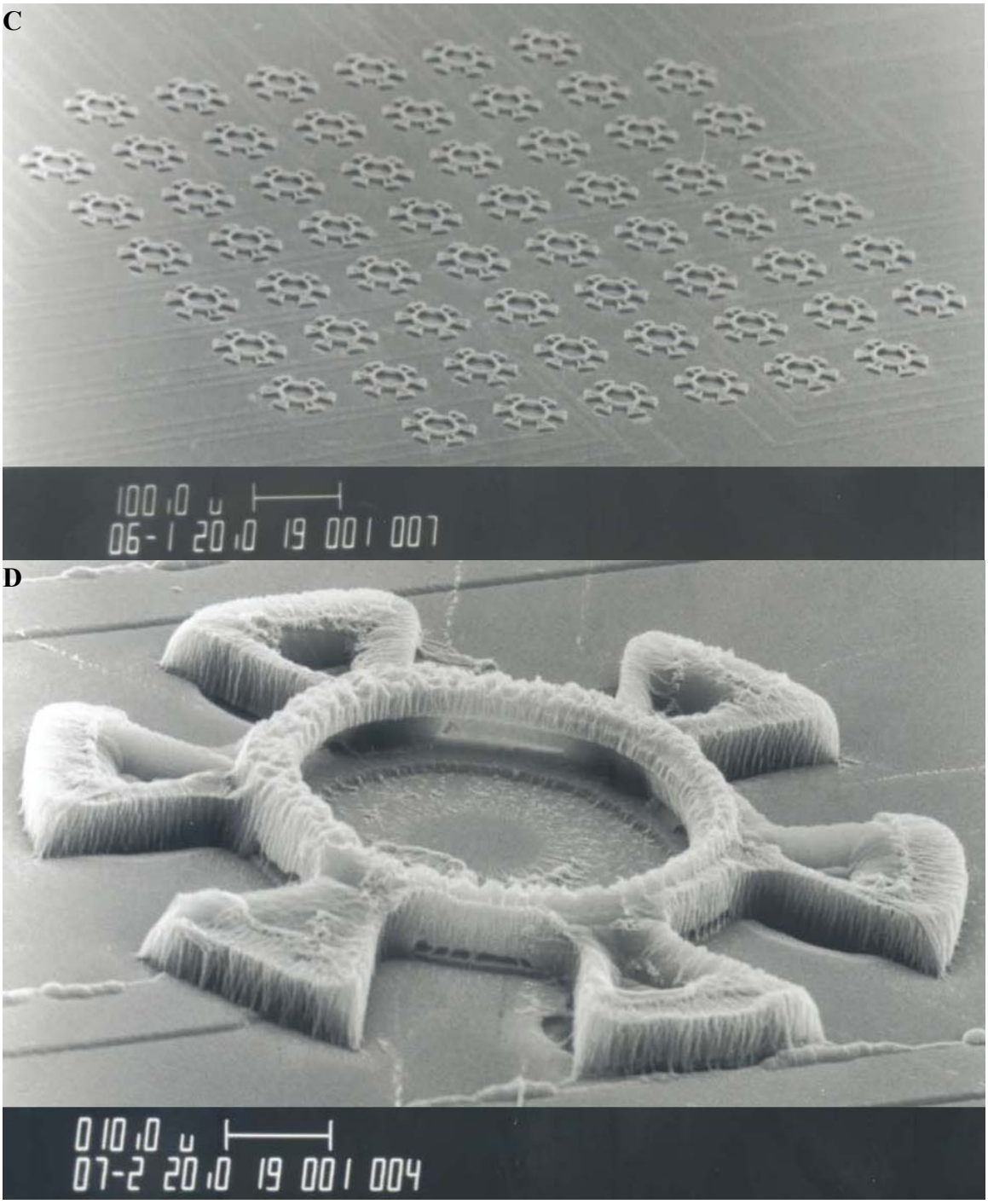


Fig. 5-17. SEMs of neurocage on glass with low-stress silicon-nitride insulation. Figs. **A** and **B** show neurocages with 25 µm long tunnels. Figs. **C** and **D** show neurocages with 4 µm long tunnels.

5.3 Neuron Loading and Culturing

Once fabricated, the neurochip is prepared for culturing by first gluing it to a culture dish. The neurochip is then prepared such that half of the surface containing the neurocages is treated with 0.5% PEI and the other half is treated with PolyHEMA (Fig. 5-18) [57]. The PEI creates a neurophilic surface to which the neurons adhere. The PolyHEMA creates a non-adhesive surface from which neurons can be easily lifted by the laser tweezers. The neurochip is then sterilized with UV light. After waiting one hour, a large group of neurons is plated at a density of 20 K/cm^2 on the PEI side near the neurocages. Another group of neurons is placed on the PolyHEMA side. Once the neurons on the PolyHEMA side are trapped and lifted by the laser tweezers, the mechanical stage moves the culture dish such that the neurocage is underneath the neuron. The neuron is then released into the neurocage. After waiting thirty minutes, the neurobasal media is added to the culture dish and the dish is moved to the incubator.

Neurons have been successfully loaded into the neurocages using the laser tweezers. Fig. 5-19 shows an image of neurons that have been cultured in the neurocages. The survival rate for neurons in these neurocages on glass (Fig. 5-20) is similar to the survival rate for neurons in neurocages on silicon (Fig. 4-34).

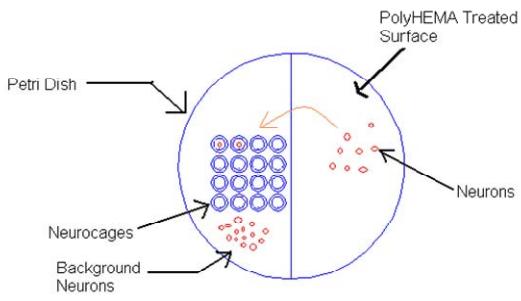


Fig. 5-18. Diagram depicting the culture dish with the neurochip attached. The side of the neurochip (and culture dish) with the neurocages is treated with PEI to ensure the neurons adhere to the surface. The other side of the neurochip is treated with PolyHEMA, a non-adhesive treatment so the laser tweezers can easily pick up the neurons for loading into the neurocages.

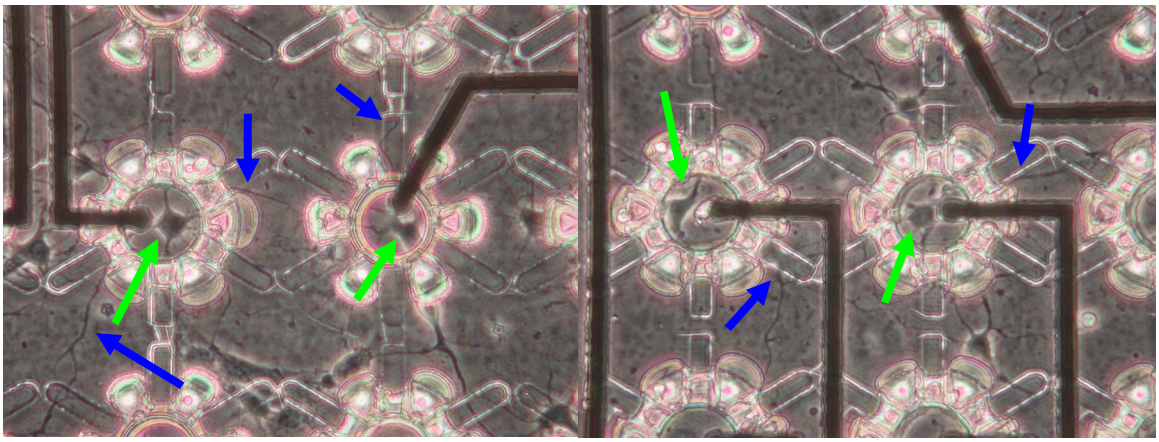


Fig. 5-19. Optical images of neurons cultured inside neurocages on glass. These neurocages have 4 μm long tunnels. The green arrows label neurons inside the neurocages. The blue arrows denote some of the neurites extending out through the tunnels.

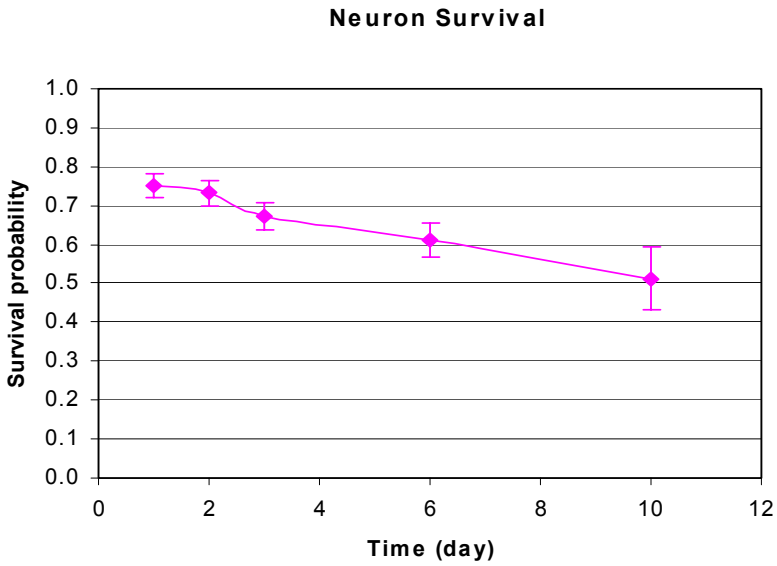


Fig. 5-20. Graph of the survival of the neurons in neurocages on glass. The survival rate is similar to that of the neurons in neurocages on silicon.

5.4 Future Work

The fabrication processes outlined in Sections 5.2.3 and 5.2.4 successfully create neurocages on a glass substrate with both Parylene-C and low-stress silicon-nitride insulation. Preliminary results indicate that the survival rate is similar to that for neurocages on silicon. Although the neurocages on glass have electrodes, neurons in these neurocages have not been stimulated and action potentials have not been recorded. As action potentials

were recorded from the neurons in neurocages on silicon (Section 4.8), however, it is reasonable to expect that action potentials can also be recorded using the neurocages on glass. Additional studies must be conducted, however, to further explore the neuronal survival rate and to use these neurocages on glass to stimulate and record action potentials.

CHAPTER 6
Conclusions

As shown in Sections 4.7 and 5.2, the fabrication processes presented here allow the creation of Parylene-C neurocages. These neurocages have nearly a 50% neuronal survival rate after 3 weeks, with less than a 1% neuronal escape rate. The electrical impedance of the electrodes with Parylene-C insulation was measured after soaking in saline at 81°C and after 4 weeks, no change was measured in the impedance. Thus, the electrodes in the neurocages should survive for more than 4 weeks when cultured, as the working temperature is only 37°C. The electrodes were also used to successfully stimulate neurons, and the resulting action potentials from the other neurons in the neural networks were recorded with the electrodes.

Although neural networks are created and action potentials are recorded from the neurons, this survival rate is low. Initial work, shown in Chapters 3 and 4, details the affect of the neurocage geometry on both the escape and survival rates. It is possible that further changes in the geometry of the cages, such as increasing the chimney diameter or increasing the number of tunnels, could increase the long-term survival rate, without affecting the neuronal escape rate. Other changes in the neurocage array structure, such as moving the neurocages closer together or further apart, could also affect the neuronal survival rate. In addition, it is also known that liquids have difficulty diffusing into and out of the neurocage, and it is been hypothesized that the low neuron survival is actually

due to limited diffusion of nutrients into and waste products out of the neurocages. One method to test this hypothesis would be to include a small microfluidic pump at the outlet of one of the tunnels for each neurocage. This could be used to create convection currents that would move nutrients into the neurocage and remove waste products. Ultimately, although it is unlikely, due to the nature of *in vitro* cell cultures, that the neurons would survive for two or three months, it should be possible to effect changes in the neurocage geometry which would increase the number of neurons surviving after two weeks. Thus, larger neural networks could be stimulated and recorded from.

The fabrication processes presented here, while not extremely complex, are quite lengthy and require significant expenditures of time. Although they have a high yield (> 90%), at least on silicon substrates, methods for reducing the number of steps within the processes should be explored. As is already seen here, simply substituting low-stress silicon-nitride for the Parylene-C insulation does reduce the number of fabrication steps. Other changes in material or neurocage geometry could lead to further reductions in the processing time.

As mentioned previously, the thin glass slides required by the use of the laser tweezers have a relatively low yield when fabricating the neurocages. Due to the fragility of the glass slides, only 75% of them survive the entire fabrication process intact. Furthermore, each glass slide only produces roughly one-third the number of devices as a standard silicon wafer used in producing the neurocages on silicon. Since each glass slide is mounted to a standard silicon wafer, this corresponds to a drastically reduced yield, especially when compared to the device yield for the neurocages on silicon. The fabrication on the glass substrate itself is not the limiting factor; rather it is the *thin* glass

slides that reduce the yield. Fabricating on thicker glass substrates would result in a device yield similar to that for fabricating on silicon. Thus, alternative methods for loading the neurons into the neurocages, ones that do not require thin substrates, should be explored. One option would be to use a combination of cell sorting chambers and microfluidics. By flowing culture media, containing neurons, down a channel, individual neurons could be sorted into small chambers. If each chamber was only large enough to hold one neuron, other neurons would be forced to simply pass by the filled chambers. Once these cell sorting chambers were filled, microchannels leading from the chambers to the neurocages could be opened and the neurons could be "pushed" from the cell sorting chambers into their individual neurocages. This method would allow the use of thicker substrates, either glass or silicon, as well as provide automatic neuron loading to ensure large numbers of neurons could be easily and quickly loaded.

Further impedance testing must also be completed for these neurocages. The data presented earlier shows that the neurocages themselves can be cleaned of all neuron debris and re-used. However, can the electrodes and insulation be re-used or will they degrade over time? Additional impedance testing, like that done in Section 4.10, would provide this information, as well as allow different insulation materials to be compared. Although Parylene-C and low-stress silicon-nitride are proven insulators, the Parylene-C insulation used on the glass substrates is actually slightly different. On the glass substrates, the Parylene-C insulation is comprised of two layers of Parylene-C, one of which has been melted. Melting the Parylene-C causes it to re-crystallize and become denser; we do not know if this will improve the insulating properties of the Parylene-C but we do not believe it will hurt. However, this hypothesis should be tested.

In conclusion, arrays of neurocages have been fabricated and action potentials have been successfully recorded. Now, with these arrays we can better study individual neuron function in response to various electrical and chemical stimuli, as well as the corresponding response for the associated neural networks. Other potential avenues for utilizing these devices include observing the details of neural network formation (Is it random or predictable?), determining the efficacy of drug treatments (on both the individual neurons and neural networks), and more. With these devices, we can gain a better understanding of how the brain functions, reveal causes and potential treatments for neurological disorders—such as multiple sclerosis and Alzheimer's—and examine neuronal recovery after infections like meningitis or encephalitis. With the information obtained using these *in vitro* neurocages, new and better *in vivo* devices (neural implants) can be designed. One of the major hurdles for neural implants, however, is the natural immune response of the body which causes the implant to be encapsulated by macrophages, severing the connection between the implanted electrodes and the brain and rendering the device useless. *In vitro* studies, using devices like the neurocages, can help us discover which neural implant materials and structures will enhance communication between peripheral nerves (or prosthetics) and the brain, while at the same time minimizing the immune response and rejection.

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APPENDIX I
Detailed Fabrication Process for Neurocages on Silicon without Electrodes

This is a detailed fabrication process for the neurocages on silicon without electrodes. Soft-baked photoresist is the sacrificial material for both the tunnels and the chimneys. The outline of the fabrication process is shown in Section 3.4.1.

A. Thermal Oxidation (Starting with prime silicon wafers)

1. Piranha
    a. 5:1:1 H_2SO_4:H_2O_2:DI H_2O
    b. Temperature: 120°C
    c. Time: 10 minutes
2. Rinse in DI H_2O
3. 10% HF dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds
4. Final rinse in DI H_2O (until > 8 MΩ)
5. Spin dry
6. Thermal oxidation
    a. Target Thickness: 0.5 μm
    b. Temperature: 1050°C
    c. Time: 1 hour
7. Measure the oxide thickness

B. Alignment Marks (Single-Side, Front-Side Only)

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ 1518 (AZ Electronic Materials, Charlotte, NC)
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the alignment marks—UV Cannon
    a. Time: 14 second exposure
6. Develop in AZ351 Developer (AZ Electronic Materials, Charlotte, NC)
    a. 4:1 DI H_2O:AZ351
    b. Time: 75 seconds
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the alignment marks
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 100 W
    c. Time: 2 minutes
11. Examine the alignment marks

12. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 μm/minute
    b. Time: ~ 6 minutes
13. Rinse in DI H_2O
14. Spin Dry
15. Examine the alignment marks
16. Etch the silicon—PEII
    a. Pressure: ~ 200 mTorr SF_6
    b. Power: 400 W
    c. Time: 3 minutes
17. Rotate the wafers 180°
18. Etch the silicon—PEII
    a. Pressure: ~ 200 mTorr SF_6
    b. Power: 400 W
    c. Time: 3 minutes
19. Examine the alignment marks
20. Strip the photoresist in ST-22 Stripper (ATMI, Danbury, CT)
    a. Temperature: 120°C
    b. Time: ~ 4 minutes
21. Rinse in Post-Solvent Rinse (ATMI, Danbury, CT)
22. Rinse in DI H_2O
23. Spin Dry
24. Examine the alignment marks

C. Anchors I

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes

2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400 (AZ Electronic Materials, Charlotte, NC)
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the anchors—Stepper
    a. MASK1B
    b. Time: 1.3 second exposure
6. Develop in AZ351
    a. 4:1 DI H_2O:AZ351
    b. Time: 2 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the anchors
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 100 W
    c. Time: 2 minutes
11. Etch the oxide with—BHF
    a. Etch rate: ~ 0.1 µm/minute
    b. Time: ~ 6 minutes
12. Rinse in DI H_2O
13. Spin Dry

14. Examine the anchors
15. Strip the photoresist in acetone
16. Rinse in isopropyl alcohol (IPA)
17. Rinse in DI H_2O
18. Spin Dry
19. Examine the anchors

D. Photoresist Chimneys and Tunnels

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 4 krpm
    c. Time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the tunnels—Stepper
    a. MASK2B
    b. Time: 0.8 second exposure
6. Expose the chimneys—Stepper
    a. MASK3B
    b. Time: 0.4 second exposure

7. Develop in AZ351 Developer
    a. 13:3 DI H_2O:AZ351
    b. Time: 3.5 minutes
8. Rinse in DI H_2O
9. Spin Dry
10. Examine
11. Measure the photoresist tunnel and chimney heights

E. Anchors II

1. 10% HF Dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds
2. Rinse in DI H_2O
3. Spin Dry
4. Examine
5. Etch the silicon—DRIE
    a. Anchors Process
    b. 50 loops (Bosch Process, Alternating SF_6 and C_4F_8 plasmas)
    c. 30 second isotropic etch (SF_6 plasma)
6. Examine
7. Measure the photoresist tunnel and chimney heights

F. Parylene-C

1. Cover the backside of wafer with dicing tape
2. Deposit Parylene-C (Specialty Coating Systems, Indianapolis, IN)
    a. Target thickness: 4 μm
    b. 4.6 g Parylene-C
    c. Approximate run time: 1.5 hours
    d. Actual thickness: 3.4 μm
3. Remove the dicing tape

4. Spin AZ 9260 (AZ Electronic Materials, Charlotte, NC)
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
5. Soft-Bake
    a. Temperature: 90°C
    b. Time: 40 minutes
6. Expose the Parylene-C tunnel and chimney openings—Stepper
    a. MASK 4B and MASK5B
    b. Time: 3.1 second exposure
7. Develop in AZ351 Developer
    a. 3:1 DI H_2O:AZ351
    b. Time: 12 minutes
8. Rinse in DI H_2O
9. Spin Dry
10. Examine
11. Etch the Parylene-C—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 400 W
    c. Etch Rate: ~ 0.17 μm/minute
    d. Time: ~ 15–20 minutes (rotating the wafer 180° every 4 minutes)
12. Examine the Parylene-C tunnel and chimney openings
13. Strip the photoresist tunnel and chimney sacrificial material in acetone
14. Rinse in IPA
15. Rinse in DI H_2O
16. Spin Dry
17. Examine

G. Dicing

1. Spin AZ 1518
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 15 minutes
3. Dice the wafer
4. Break the wafer
5. Strip the photoresist in acetone
6. Rinse in IPA
7. Rinse in DI H_2O

H. Final Cleaning

1. Piranha
    a. 5:1:1 H_2SO_4:H_2O_2:DI H_2O
    b. Temperature: 120°C
    c. Time: 10 minutes
2. Rinse in DI H_2O
3. 10% HF Dip
    a. 10:1 DI H_2O:HF
    b. 10 seconds
4. Rinse in DI H_2O
5. Dry
6. Examine the chips

APPENDIX II
Detailed Fabrication Process for Neurocages on Silicon with Electrodes and Parylene-C Insulation

This is a detailed fabrication process for the neurocages on silicon with electrodes and Parylene-C insulation. Aluminum is the sacrificial material for the tunnels and soft-baked photoresist is the sacrificial material for the chimneys. The outline of the fabrication process is shown in Section 4.7.

A. Thermal Oxidation (Starting with prime silicon wafers)

1. Piranha
    a. 5:1:1 H_2SO_4:H_2O_2:DI H_2O
    b. Temperature: 120°C
    c. Time: 10 minutes
2. Rinse in DI H_2O
3. 10% HF dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds
4. Final rinse in DI H_2O (until > 8 MΩ)
5. Spin dry
6. Thermal oxidation
    a. Target Thickness: 0.5 μm
    b. Temperature: 1050°C
    c. Time: 1 hour
7. Measure the oxide thickness

B. Alignment Marks and Electrodes

1. Spin LOR3B (MicroChem Corporation, Newton, MA)
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 3 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 190°C
    b. Time: 10 minutes
3. Spin AZ 1518
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 3 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the alignment marks and electrodes—Stepper
    a. ALIGNMENT MARK MASK and MASK 1A-M/1B-M
    b. Time: 0.48 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 1.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the alignment marks and electrodes
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes

11. Metal Deposition—Thermal Evaporator
    a. Chrome
        1) Target thickness: 100 Å
        2) 1 rod chrome
        3) Start pot setting: 1.8
        4) End pot setting: 1.9
        5) Average deposition rate: 0.3 Å/s
        6) Maximum deposition rate: 0.4 Å/s
        7) Time: 6 minutes
        8) Thickness: 104 Å
    b. Gold
        1) Target thickness: 3000 Å
        2) 2.70 g gold
        3) S22-010-W Boat (RD Mathis Company, Long Beach, CA)
        4) Start pot setting: 3.2
        5) End pot setting: 3.5
        6) Average deposition rate: 2.7 Å/s
        7) Maximum deposition rate: 3.3 Å/s
        8) Time: 20 minutes
        9) Thickness: 3000 Å
12. Metal lift-off in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 1–2 hours
13. Rinse in Post-Solvent Rinse
14. Rinse in DI H_2O
15. Metal lift-off in an ultrasonic bath in acetone
    a. Time: ~ 20–30 minutes
16. Rinse in IPA

17. Rinse in DI H_2O
18. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
19. Rinse in Post-Solvent Rinse
20. Rinse in DI H_2O
21. Spin Dry
22. Examine the alignment marks and electrodes

C. Insulation Anchors

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the insulation anchors—Stepper
    a. MASK 2M
    b. Time: 1.4 second exposure

6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the insulation anchors
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 μm/minute
    b. Time: ~ 5 minutes
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the insulation anchors
15. Etch the silicon—DRIE
    a. Anchors Process
    b. 60 loops (Bosch Process, Alternating SF_6 and C_4F_8 plasmas)
    c. 30 second isotropic etch (SF_6 plasma)
16. Examine the insulation anchors
17. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 400 W
    c. Time: 4 minutes
18. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes

19. Rinse in Post Solvent Rinse
20. Rinse in DI H_2O
21. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes
22. Rinse in IPA
23. Rinse in DI H_2O
24. Spin Dry
25. Examine the insulation anchors

D. Neurocage Anchors I

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the neurocage anchors—Stepper
    a. MASK 3M
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes

7. Rinse in DI H_2O
8. Spin Dry
9. Examine the neurocage anchors
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 µm/minute
    b. Time: ~ 5 minutes
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the neurocage anchors
15. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
16. Rinse in Post Solvent Rinse
17. Rinse in DI H_2O
18. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes
19. Rinse in IPA
20. Rinse in DI H_2O
21. Spin Dry
22. Examine the neurocage anchors

E. Parylene-C Insulation I

1. Piranha
    a. 5:1:1 H_2SO_4:DI H_2O:H_2O_2
    b. Temperature: 120°C
    c. Time: 5 minutes
2. Rinse in DI H_2O
3. Spin Dry
4. Examine
5. Soak in A-174 Adhesion Promoter (Specialty Coating Systems, Indianapolis, IN)
    a. 100:100:1 DI H_2O:IPA:A-174, mixed 2–24 hours prior
    b. Time: 30 minutes
6. Air dry
    a. Time: 30 minutes
7. Clean with IPA
    a. Time: 15 seconds
8. Drain and blow dry
9. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
10. Cover the backside of the wafer with dicing tape
11. Deposit Parylene-C
    a. Target thickness: 4 μm
    b. 6.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.9 μm
12. Remove the dicing tape

F. Electrode Vias

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
3. Expose the electrode vias—Stepper
    a. MASK 4A-M/4B-M
    b. Time: 7.0 second exposure
4. Develop in AZ Developer (AZ Electronic Materials, Charlotte, NC)
    a. Time: 7 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the electrode vias
8. Etch the Parylene-C—DRIE
    a. Aprtest2 Process
    b. 30 loops (Alternating O_2 and C_4F_8 plasmas)
    c. Etch rate: ~ 0.4 µm/minute = ~ 0.13 µm/loop
9. Examine the electrode vias
10. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
11. Rinse in Post Solvent Rinse
12. Rinse in DI H_2O
13. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes

14. Rinse in IPA
15. Rinse in DI H_2O
16. Spin Dry
17. Examine the electrode vias

G. Neurocage Anchors II

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
3. Expose the neurocage anchors—Stepper
    a. MASK 3M
    b. Time: 7.0 second exposure
4. Develop in AZ Developer
    a. Time: 7 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine
8. Etch the Parylene-C—DRIE
    a. Aprtest2 Process
    b. 30 loops (Alternating O_2 and C_4F_8 plasmas)
    c. Etch rate: ~ 0.4 µm/minute = ~ 0.13 µm/loop
9. Examine the neurocage anchors
10. 10% HF Dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds

11. Rinse in DI H_2O
12. Spin Dry
13. Examine the neurocage anchors
14. Etch the silicon—DRIE
    a. Anchors Process
    b. 60 loops (Bosch Process, Alternating SF_6 and C_4F_8 plasmas)
    c. 30 second isotropic etch (SF_6 plasma)
15. Examine the neurocage anchors
16. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
17. Rinse in Post Solvent Rinse
18. Rinse in DI H_2O
19. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes
20. Rinse in IPA
21. Rinse in DI H_2O
22. Spin Dry
23. Examine the neurocage anchors

H. Parylene-C Insulation II

1. Parylene-C Anneal—Vacuum Oven/Mini-Brute
    a. Temperature: 200°C
    b. Time: 48 hours
    c. N_2 backfill
2. Parylene-C Roughening—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 50 W
    c. Time: 30 seconds

I. Aluminum Tunnels

1. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
3. Expose the tunnels—Stepper
    a. MASK 5L-M/5N-M/5H-M
    b. Time: 1.4 second exposure
4. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the tunnels

8. Metal Deposition I—Thermal Evaporator
    a. Target thickness: 5000 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat (RD Mathis Company, Long Beach, CA)
    d. Start pot setting: 2.9
    e. End pot setting: 3.1
    f. Average deposition rate: 3.7 Å/s
    g. Maximum deposition rate: 4.7 Å/s
    h. Time: 24 minutes
    i. Thickness: 5374 Å
    j. Heat B12B Basket (RD Mathis Company, Long Beach, CA) in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
9. Metal Deposition II—Thermal Evaporator
    a. Target thickness: 4626 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.0
    f. Average deposition rate: 4.2 Å/s
    g. Maximum deposition rate: 5.1 Å/s
    h. Time: 18.75 minutes
    i. Thickness: 4689 Å
10. Metal lift-off in an ultrasonic bath in acetone
11. Rinse in IPA
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the tunnels
15. Measure the aluminum tunnel height

J. Aluminum Etch Stop

1. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
3. Expose the etch stop—Stepper
    a. MASK 6L-M/6SW-M/6SN-M/6SH-M
    b. Time: 2.0 second exposure
4. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 5 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the etch stop

8. Metal Deposition—Thermal Evaporator
    a. Target thickness: 2000 Å
    b. ~0.8 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.0
    f. Average deposition rate: 3.3 Å/s
    g. Maximum deposition rate: 4.3 Å/s
    h. Time: 10.5 minutes
    i. Thickness: 2057 Å
    j. Heat B12B Basket in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
9. Metal lift-off in an ultrasonic bath in acetone
10. Rinse in IPA
11. Rinse in DI H_2O
12. Spin Dry
13. Examine the etch stop
14. Measure the aluminum tunnel height

K. Photoresist Chimneys
1. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes

3. Expose the chimneys—Stepper
    a. MASK 7-M and BLANK MASK
    b. Time: 2.0 second exposure
4. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 5 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the chimneys
8. Measure the aluminum tunnel and photoresist chimney heights

L. Neurocage Parylene-C
1. Cover the backside of wafer with dicing tape
2. Deposit Parylene-C
    a. Target thickness: 4 μm
    b. 6.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.9 μm
3. Remove the dicing tape

M. Parylene-C Chimneys
1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 90°C
    b. Time: 40 minutes

3. Expose the Parylene-C chimney openings—Stepper
    a. MASK 8-M
    b. Time: 6.0 second exposure
4. Develop in AZ Developer
    a. Time: 6 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C chimney openings
8. Etch the Parylene-C—DRIE
    a. Aprtest2 Process
    b. 24 loops (Alternating O_2 and C_4F_8 plasmas)
    c. Etch rate: ~ 0.5 µm/minute = ~ 0.16 µm/loop
9. Examine the Parylene-C chimney openings
10. Strip the photoresist in acetone
11. Rinse in IPA
12. Rinse in DI H2O
13. Spin Dry
14. Examine the Parylene-C chimney openings

N. Parylene-C Tunnels

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2. Soft-Bake
    a. Temperature: 85°C
    b. Time: 45 minutes

3. Expose the Parylene-C tunnel openings—Stepper
    a. MASK 9L-M/9SW-M/9SN-M/9SH-M and BLANK MASK
    b. Time: 7.0 second exposure
4. Develop in AZ Developer
    a. Time: 8 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C tunnel openings
8. Etch the Parylene-C—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 300 W
    c. Etch rate: ~ 0.14 μm/minute
    d. Time: 28 minutes (etching 2 minutes at a time and rotating the wafer 90° every 4 minutes)
9. Examine the Parylene-C tunnel openings

O. Parylene-C Oxide

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 80°C
    b. Time: 50 minutes
3. Expose the Parylene-C—Stepper
    a. BLANK MASK
    b. Time: 7.0 second exposure
4. Develop in AZ Developer
    a. Time: 8 minutes

5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C
8. Etch the Parylene-C—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 300 W
    c. Etch rate: ~ 0.18 μm/minute
    d. Time: 16 minutes (rotating the wafer 90° every 4 minutes
9. Examine the Parylene-C
10. Strip the photoresist in acetone
11. Rinse in IPA
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the Parylene-C

P. Final Cleaning and Dicing

1. Etch the aluminum in Aluminum Etchant Type A (Transene Company, Danvers, MA)
    a. Temperature: 60°C
    b. Time: 30 minutes
2. Rinse in DI H_2O
3. Spin Dry
4. Examine
5. Ultrasonic cleaning in acetone
    a. Time: 20 minutes
6. Rinse in IPA
7. Rinse in DI H_2O
8. Spin Dry
9. Examine

10. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
11. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
12. Dice the wafer
13. Strip the photoresist in acetone
14. Rinse in IPA
15. Rinse in DI H_2O
16. Dry
17. Break the wafer
18. Examine the chips

APPENDIX III
Detailed Fabrication Process for Neurocages on Silicon with Electrodes and Low-Stress Silicon-Nitride Insulation

This is a detailed fabrication process for the neurocages on silicon with electrodes and low-stress silicon-nitride insulation. Aluminum is the sacrificial material for the tunnels and soft-baked photoresist is the sacrificial material for the chimneys. The outline of the fabrication process is shown in Section 4.7.

A. Thermal Oxidation (Starting with prime silicon wafers)

1. Piranha
    a. 5:1:1 H_2SO_4:H_2O_2:DI H_2O
    b. Temperature: 120°C
    c. Time: 10 minutes
2. Rinse in DI H_2O
3. 10% HF dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds
4. Final rinse in DI H_2O (until > 8 MΩ)
5. Spin dry
6. Thermal oxidation
    a. Target Thickness: 0.5 μm
    b. Temperature: 1050°C
    c. Time: 1 hour

7. Measure the oxide thickness

B. Alignment Marks and Electrodes

1. Spin LOR3B
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 3 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 190°C
    b. Time: 10 minutes
3. Spin AZ 1518
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 3 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the alignment marks and electrodes—Stepper
    a. ALIGNMENT MARK MASK and MASK 1A-M/1B-M
    b. Time: 0.48 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 1.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the alignment marks and electrodes

10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Metal Deposition—Thermal Evaporator
    a. Chrome
        1) Target thickness: 100 Å
        2) 1 rod chrome
        3) Start pot setting: 1.8
        4) End pot setting: 1.9
        5) Average deposition rate: 0.3 Å/s
        6) Maximum deposition rate: 0.4 Å/s
        7) Time: 6 minutes
        8) Thickness: 104 Å
    b. Gold
        1) Target thickness: 3000 Å
        2) 2.70 g gold
        3) S22-010-W Boat
        4) Start pot setting: 3.2
        5) End pot setting: 3.5
        6) Average deposition rate: 2.7 Å/s
        7) Maximum deposition rate: 3.3 Å/s
        8) Time: 20 minutes
        9) Thickness: 3000 Å
12. Metal lift-off in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 1–2 hours
13. Rinse in Post-Solvent Rinse

14. Rinse in DI H_2O
15. Metal lift-off in an ultrasonic bath in acetone
    a. Time: ~ 20–30 minutes
16. Rinse in IPA
17. Rinse in DI H_2O
18. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
19. Rinse in Post-Solvent Rinse
20. Rinse in DI H_2O
21. Spin Dry
22. Examine the alignment marks and electrodes

C. Neurocage Anchors I

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes

5. Expose the neurocage anchors—Stepper
    a. MASK 3M
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the neurocage anchors
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 µm/minute
    b. Time: ~ 5 minutes
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the neurocage anchors
15. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
16. Rinse in Post Solvent Rinse
17. Rinse in DI H_2O
18. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes
19. Rinse in IPA
20. Rinse in DI H_2O

21. Spin Dry
22. Examine the neurocage anchors

D. Low-Stress Silicon-Nitride

1. Deposit Low-Stress Silicon-Nitride Deposition—PECVD
    a. Gases: N_2 (1960 sccm) + NH_3 (40 sccm) + SiH_4 (56 sccm)
    b. Pressure: 500 mTorr
    c. Temperature: 300 °C
    d. Power: 80 W (13.56 MHz)
    e. Stress: 2 MPa
    f. Deposition Rate: 0.02 μm/minute
    g. Deposition Time: 50 minutes
    h. Thickness: 1 μm

E. Electrode Vias

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes

5. Expose the electrode vias—Stepper
    a. MASK 4A-M/4B-M
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the electrode vias
10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Etch the low-stress silicon-nitride—PEII
    a. Pressure: ~ 200 mTorr SF_6
    b. Power: 300 W
    c. Etch rate: ~ 0.12 μm/minute
    d. Time: 8 minutes (rotating the wafer 180° every 4 minutes)
12. Examine the electrode vias
13. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
14. Rinse in Post Solvent Rinse
15. Rinse in DI H_2O
16. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes
17. Rinse in IPA
18. Rinse in DI H_2O

19. Spin Dry
20. Examine the electrode vias

F. Neurocage Anchors II

1. Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the neurocage anchors—Stepper
    a. MASK 3M
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine

10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 200 W
    c. Time: 2 minutes
11. Etch the low-stress silicon-nitride—PEII
    a. Pressure: ~ 200 mTorr SF_6
    b. Power: 300 W
    c. Etch rate: ~ 0.1 μm/minute
    d. Time: 10 minutes (rotating the wafer 180° every 5 minutes)
12. Examine the neurocage anchors
13. 10% HF Dip
    a. 10:1 DI H_2O:HF
    b. Time: 10 seconds
14. Rinse in DI H_2O
15. Spin Dry
16. Examine the neurocage anchors
17. Etch the silicon—DRIE
    a. Anchors Process
    b. 60 loops (Bosch Process, Alternating SF_6 and C_4F_8 plasmas)
    c. 30 second isotropic etch (SF_6 plasma)
18. Examine the neurocage anchors
19. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 5 minutes
20. Rinse in Post Solvent Rinse
21. Rinse in DI H_2O
22. Rinse in an ultrasonic bath in acetone
    a. Time: 5 minutes

23. Rinse in IPA
24. Rinse in DI H_2O
25. Spin Dry
26. Examine the neurocage anchors

G. Aluminum Tunnels

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the tunnels—Stepper
    a. MASK 5L-M/5N-M/5H-M
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the tunnels

10. Descum—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 100 W
    c. Time: 2 minutes
11. Metal Deposition I—Thermal Evaporator
    a. Target thickness: 5000 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.2
    f. Average deposition rate: 3.2 Å/s
    g. Maximum deposition rate: 4.8 Å/s
    h. Time: 30 minutes
    i. Thickness: 5800 Å
    j. Heat B12B Basket in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
12. Metal Deposition II—Thermal Evaporator
    a. Target thickness: 4200 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 2.9
    f. Average deposition rate: 2.8 Å/s
    g. Maximum deposition rate: 4.2 Å/s
    h. Time: 25.5 minutes
    i. Thickness: 4230 Å
13. Metal lift-off in an ultrasonic bath in acetone
14. Rinse in IPA

15. Rinse in DI H_2O
16. Spin Dry
17. Examine the tunnels
18. Measure the aluminum tunnel height

H. Photoresist Chimneys

1. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
2. HMDS
    a. 2 mL
    b. Time: 1 minute
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the chimneys—Stepper
    a. MASK 7-M and BLANK MASK
    b. Time: 2.0 second exposure
6. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the chimneys
10. Measure the aluminum tunnel and photoresist chimney heights

I. Neurocage Parylene-C

1. Cover the backside of wafer with dicing tape
2. Deposit Parylene-C
    a. Target thickness: 4 μm
    b. 6.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.75 μm
3. Remove the dicing tape

J. Parylene-C Chimneys

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 90°C
    b. Time: 40 minutes
3. Expose the Parylene-C chimney openings—Stepper
    a. MASK 8-M
    b. Time: 6.0 second exposure
4. Develop in AZ Developer
    a. Time: 6 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C chimney openings

8. Etch the Parylene-C—DRIE
    a. Aprtest2 Process
    b. 19 loops (Alternating O_2 and C_4F_8 plasmas)
    c. Etch rate: ~ 0.6 µm/minute = ~ 0.2 µm/loop
9. Examine the Parylene-C chimney openings
10. Strip the photoresist in acetone
11. Rinse in IPA
12. Rinse in DI H2O
13. Spin Dry
14. Examine the Parylene-C chimney openings

K. Parylene-C Tunnels

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Time: 40 seconds
2. Soft-Bake
    a. Temperature: 85°C
    b. Time: 45 minutes
3. Expose the Parylene-C tunnel openings—Stepper
    a. MASK 9L-M/9SW-M/9SN-M/9SH-M and BLANK MASK
    b. Time: 7.0 second exposure
4. Develop in AZ Developer
    a. Time: 8 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C tunnel openings

8. Etch the Parylene-C—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 300 W
    c. Etch rate: ~ 0.13 μm/minute
    d. Time: 32 minutes (etching 2 minutes at a time and rotating the wafer 90° every 4 minutes)
9. Examine the Parylene-C tunnel openings
10. Strip the photoresist in acetone
11. Rinse in IPA
12. Rinse in DI H_2O
13. Spin Dry
14. Examine the Parylene-C tunnel openings

L. Final Cleaning and Dicing

1. Etch the aluminum in Aluminum Etchant Type A
    a. Temperature: 60°C
    b. Time: 30 minutes
2. Rinse in DI H_2O
3. Spin Dry
4. Examine
5. Ultrasonic cleaning in acetone
    a. Time: 20 minutes
6. Rinse in IPA
7. Rinse in DI H_2O
8. Spin Dry
9. Examine

10. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
11. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
12. Dice the wafer
13. Strip the photoresist in acetone
14. Rinse in IPA
15. Rinse in DI H_2O
16. Dry
17. Break the wafer
18. Examine the chips

APPENDIX IV
Detailed Fabrication Process for Neurocages on Glass with Electrodes and Parylene-C Insulation

This is a detailed fabrication process for the neurocages on glass with electrodes and Parylene-C insulation. Aluminum is the sacrificial material for the tunnels and soft-baked photoresist is the sacrificial material for the chimneys. The outline of the fabrication process is shown in Section 5.2.3.

A. Glass Slide Preparation

1. Bake—Mini-Brute
    a. Temperature: 400°C
    b. Time: 2 hours
    c. No N_2 backfill
2. O_2 Plasma Clean—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 400 W
    c. Time: 5 minutes
3. Piranha
    a. 5:1:1 H_2SO_4:DI H_2O:H_2O_2
    b. Temperature: 120°C
    c. Time: 10 minutes
4. Rinse in DI H_2O
5. Dry

B. Alignment Marks and Electrodes

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
3. HMDS
    a. 2 mL
    b. Time: 1 minute
4. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
5. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
6. Expose the alignment marks and electrodes—Stepper
    a. ALIGNMENT MARK MASK and MASK 1A-D/1B-D
    b. Time: 1.4 second exposure
7. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
8. Rinse in DI H_2O
9. Spin Dry
10. Examine the alignment marks and electrodes

11. Descum—RIE
    a. Process #2
    b. Gas 3 (O_2): 50%
    c. Gas 4 (O_2): 0%
    d. Power: 40%
    e. Pressure: 120 mTorr
    f. Time: 3 minutes
12. Metal Deposition—Thermal Evaporator
    a. Chrome
        1) Target thickness: 100 Å
        2) 1 rod chrome
        3) Start pot setting: 1.8
        4) End pot setting: 1.9
        5) Average deposition rate: 0.3 Å/s
        6) Maximum deposition rate: 0.4 Å/s
        7) Time: 5.5 minutes
        8) Thickness: 102 Å
    b. Gold
        1) Target thickness: 3000 Å
        2) 2.70 g Au
        3) S22-010-W Boat
        4) Start pot setting: 3.2
        5) End pot setting: 3.5
        6) Average deposition rate: 2.9 Å/s
        7) Maximum deposition rate: 3.7 Å/s
        8) Time: 17.5 minutes
        9) Thickness: 3014 Å
13. Metal lift-off and glass slide release in an ultrasonic bath in acetone

14. Rinse in IPA
15. Rinse in DI H_2O
16. Dry
17. Examine the alignment marks and electrodes

C. Parylene-C Insulation I

1. Deposit Parylene-C I
    a. Target thickness: 0.5 μm
    b. 0.65 g Parylene-C
    c. Approximate run time: 1 hour
    d. Actual thickness: 0.62 μm
2. Parylene-C Annealing I—Mini-Brute
    a. Temperature: 350°C
    b. Time: 2 hours
    c. N_2 backfill
3. Deposit Parylene-C II
    a. Target thickness: 3.38 μm
    b. 4.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.54 μm
4. Parylene-C Annealing II—Vacuum Oven/Mini-Brute
    a. Temperature: 200°C
    b. Time: 48 hours
    c. N_2 backfill

D. Electrode Vias

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer

2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the electrode vias—Stepper
    a. MASK 3A-D/3B-D
    b. Time: 7.0 second exposure
6. Develop in AZ Developer
    a. Time: 7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the electrode vias
10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 65%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.2 µm/minute
    g. 21 minutes (Rotate the wafer/glass slide 180° every 3 minutes)
11. Examine the electrode vias
12. Release the glass slide in acetone

13. Rinse in IPA
14. Rinse in DI H_2O
15. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
16. Rinse in Post-Solvent Rinse
17. Rinse in DI H_2O
18. Rinse in IPA
19. Rinse in DI H_2O
20. Dry
21. Examine the electrode vias

E. Neurocage Anchors

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the neurocage anchors—Stepper
    a. MASK 2-D
    b. Time: 7.0 second exposure

6. Develop in AZ Developer
    a. Time: 7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the neurocage anchors
10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 65%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.23 µm/minute
    g. Time: 15 minutes (Rotate the wafer/glass slide 180° every 3 minutes)
11. Examine the neurocage anchors
12. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 µm/minute
    b. Time: 18 minutes
13. Rinse in DI H_2O
14. Spin Dry
15. Examine the neurocage anchors
16. Release the glass slide in acetone
17. Rinse in IPA
18. Rinse in DI H_2O
19. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
20. Rinse in Post-Solvent Rinse
21. Rinse in DI H_2O

22. Rinse in IPA
23. Rinse in DI H_2O
24. Dry
25. Examine the neurocage anchors

F. Parylene-C Insulation II

1. Parylene-C Roughening—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 50 W
    c. Time: 30 seconds

G. Aluminum Tunnels

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the tunnels—Stepper
    a. MASK 4-D
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O

8. Spin Dry
9. Examine the tunnels
10. Metal Deposition I—Thermal Evaporator
    a. Target thickness: 5000 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.1
    f. Average deposition rate: 3.6 Å/s
    g. Maximum deposition rate: 5.6 Å/s
    h. Time: 30 minutes
    i. Thickness: 6463 Å
    j. Heat B12B Basket in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
11. Metal Deposition II—Thermal Evaporator
    a. Target Thickness: 3537 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.0
    f. Average deposition rate: 3.8 Å/s
    g. Maximum deposition rate: 5.0 Å/s
    h. Time: 15.5 minutes
    i. Thickness: 3555 Å
12. Metal lift-off and glass slide release in an ultrasonic bath in acetone
13. Rinse in IPA
14. Rinse in DI H_2O
15. Dry

16. Examine the tunnels
17. Measure the aluminum tunnel height

H. Aluminum Etch Stop

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the etch stop—Stepper
    a. MASK 5AN-D/5AT-D/5B-D
    b. Time: 2.0 second exposure
6. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 6 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the etch stop

10. Metal Deposition—Thermal Evaporator
    a. Target thickness: 2000 Å
    b. ~0.8 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.1
    f. Average deposition rate: 3.5 Å/s
    g. Maximum deposition rate: 4.2 Å/s
    h. Time: 10 minutes
    i. Thickness: 2015 Å
    j. Heat B12B Basket in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
11. Metal lift-off and glass slide release in an ultrasonic bath in acetone
12. Rinse in IPA
13. Rinse in DI H_2O
14. Dry
15. Examine the etch stop
16. Measure the aluminum tunnel height

I. Photoresist Chimneys
    1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
    2. Bake
        a. Temperature: 100°C
        b. Time: 5 minutes
    3. Spin AZ P4400
        a. Ramp rate: 0.5 krpm
        b. Spin speed: 2 krpm
        c. Hold time: 40 seconds

4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the chimneys—Stepper
    a. MASK 6O-D and BLANK MASK
    b. Time: 2.0 second exposure
6. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 6.5–7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the chimneys
10. Measure the aluminum tunnel and photoresist chimney heights

J. Neurocage Parylene-C
1. Cover the backside of wafer with dicing tape
2. Deposit Parylene-C
    a. Target thickness: 4 μm
    b. 6.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.79 μm
3. Remove the dicing tape

K. Parylene-C Chimneys
1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds

2. Soft-Bake
    a. Temperature: 90°C
    b. Time: 40 minutes
3. Expose the Parylene-C chimney openings—Stepper
    a. MASK 7-D
    b. Time: 6.0 second exposure
4. Develop in AZ Developer
    a. Time: 6 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C chimney openings
8. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 50%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.38 μm/minute
    g. Time: 10–11 minutes (Rotating the wafer/glass slide 180° every 3 minutes)
9. Examine the Parylene-C chimney openings
10. Release the glass slide and strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
11. Rinse in Post-Solvent Rinse
12. Rinse in DI H_2O
13. Rinse in IPA
14. Rinse in DI H_2O
15. Dry

16. Examine the Parylene-C chimney openings

L. Parylene-C Tunnels

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 85°C
    b. Time: 45 minutes
5. Expose the Parylene-C tunnel openings—Stepper
    a. MASK 8N-D/8T-D and BLANK MASK
    b. Time: 8.0 second exposure
6. Develop in AZ Developer
    a. Time: 3.75 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the Parylene-C tunnel openings

10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 50%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.18 µm/minute
    g. Time: 21 minutes (Rotating the wafer/glass slide 180° every 3 minutes)
11. Examine the Parylene-C tunnel openings

M. Final Cleaning and Dicing

1. Strip the photoresist and release the glass slide in acetone
2. Rinse in IPA
3. Rinse in DI H_2O
4. Dry
5. Examine
6. Etch the aluminum in Aluminum Etchant Type A
    a. Temperature: 60°C
    b. Time: 30 minutes
7. Rinse in DI H_2O
8. Dry
9. Examine
10. Spin AZ 9260 onto wafer and gently press glass slide onto wafer
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
11. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes

12. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
13. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
14. Dice glass slide
15. Strip the photoresist in acetone
16. Break the glass slide
17. Rinse in IPA
18. Rinse in DI H_2O
19. Dry
20. Examine

APPENDIX V
Detailed Fabrication Process for Neurocages on Glass with Electrodes and Low-Stress Silicon-Nitride Insulation

This is a detailed fabrication process for the neurocages on glass with electrodes and low-stress silicon-nitride insulation. Aluminum is the sacrificial material for the tunnels and soft-baked photoresist is the sacrificial material for the chimneys. The outline of the fabrication process is shown in Section 5.2.4.

A. Glass Slide Preparation

1. Bake—Mini-Brute
    a. Temperature: 400°C
    b. Time: 2 hours
    c. No N_2 backfill
2. O_2 Plasma Clean—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 400 W
    c. Time: 5 minutes
3. Piranha
    a. 5:1:1 H_2SO_4:DI H_2O:H_2O_2
    b. Temperature: 120°C
    c. Time: 10 minutes
4. Rinse in DI H_2O
5. Dry

B. Alignment Marks and Electrodes

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 10 minutes
3. HMDS
    a. 2 mL
    b. Time: 1 minute
4. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
5. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
6. Expose the alignment marks and electrodes—Stepper
    a. ALIGNMENT MARK MASK and MASK 1A-D/1B-D
    b. Time: 1.4 second exposure
7. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
8. Rinse in DI H_2O
9. Spin Dry
10. Examine the alignment marks and electrodes

11. Descum—RIE
    a. Process #2
    b. Gas 3 (O_2): 50%
    c. Gas 4 (O_2): 0%
    d. Power: 40%
    e. Pressure: 120 mTorr
    f. Time: 3 minutes
12. Metal Deposition—Thermal Evaporator
    a. Chrome
        1) Target thickness: 100 Å
        2) 1 rod chrome
        3) Start pot setting: 1.8
        4) End pot setting: 1.9
        5) Average deposition rate: 0.3 Å/s
        6) Maximum deposition rate: 0.4 Å/s
        7) Time: 5.5 minutes
        8) Thickness: 102 Å
    b. Gold
        1) Target thickness: 3000 Å
        2) 2.70 g Au
        3) S22-010-W Boat
        4) Start pot setting: 3.2
        5) End pot setting: 3.5
        6) Average deposition rate: 2.9 Å/s
        7) Maximum deposition rate: 3.7 Å/s
        8) Time: 17.5 minutes
        9) Thickness: 3014 Å
13. Metal lift-off and glass slide release in an ultrasonic bath in acetone

14. Rinse in IPA
15. Rinse in DI H_2O
16. Dry
17. Examine the alignment marks and electrodes

C. Low-Stress Silicon-Nitride Insulation

1. Deposit Low-Stress Silicon-Nitride Deposition—PECVD
    a. Gases: N_2 (1960 sccm) + NH_3 (40 sccm) + SiH_4 (56 sccm)
    b. Pressure: 500 mTorr
    c. Temperature: 300°C
    d. Power: 80 W (13.56 MHz)
    e. Stress: 2 MPa
    f. Deposition Rate: 0.02 μm/minute
    g. Deposition Time: 50 minutes
    h. Thickness: 1 μm

D. Parylene-C Anchors I

1. Parylene-C Deposition I
    a. Target thickness: 0.5 μm
    b. 0.65 g Parylene-C
    c. Approximate run time: 1 hour
    d. Actual thickness: 0.60 μm
2. Parylene-C Annealing I—Mini-Brute
    a. Temperature: 350°C
    b. Time: 2 hours
    c. N_2 backfill

E. Electrode Vias

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer

2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the electrode vias—Stepper
    a. MASK 3A-D/3B-D
    b. Time: 7.0 second exposure
6. Develop in AZ Developer
    a. Time: 7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the electrode vias
10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 65%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.23 μm/minute
    g. Time: 4 minutes

11. Etch the low-stress silicon-nitride—RIE
    a. Process #4
    b. Gas 2 (SF_6): 50%
    c. Gas 3 (O_2): 10%
    d. Power: 65%
    e. Pressure: 120 mTorr
    f. Etch rate: ~ 0.1 µm/minute
    g. Time: 10 minutes (Rotating the wafer/glass slide 180° every 5 minutes)
12. Examine the electrode vias
13. Release the glass slide in acetone
14. Rinse in IPA
15. Rinse in DI H_2O
16. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
17. Rinse in Post-Solvent Rinse
18. Rinse in DI H_2O
19. Rinse in IPA
20. Rinse in DI H_2O
21. Dry
22. Examine the electrode vias

F. Neurocage Anchors
    1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
    2. Bake
        a. Temperature: 100°C
        b. Time: 5 minutes

3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the neurocage anchors—Stepper
    a. MASK 2-D
    b. Time: 7.0 second exposure
6. Develop in AZ Developer
    a. Time: 7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the neurocage anchors
10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 65%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.23 μm/minute
    g. Time: 4 minutes
11. Examine the neurocage anchors

12. Etch the low-stress silicon-nitride—RIE
    a. Process #4
    b. Gas 2 (SF_6): 50%
    c. Gas 3 (O_2): 10%
    d. Power: 65%
    e. Pressure: 120 mTorr
    f. Etch rate: ~ 0.1 µm/minute
    g. Time: 12 minutes (Rotating the wafer/glass slide 180° every 6 minutes)
13. Examine the neurocage anchors
14. Etch the oxide—BHF
    a. Etch rate: ~ 0.1 µm/minute
    b. Time: 6–8 minutes
15. Rinse in DI H_2O
16. Spin Dry
17. Examine the neurocage anchors
18. Release the glass slide in acetone
19. Rinse in IPA
20. Rinse in DI H_2O
21. Strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
22. Rinse in Post-Solvent Rinse
23. Rinse in DI H_2O
24. Rinse in IPA
25. Rinse in DI H_2O
26. Dry
27. Examine the neurocage anchors

G. Parylene-C Anchors II

1. Parylene-C Roughening—PEII
    a. Pressure: ~ 200 mTorr O_2
    b. Power: 50 W
    c. Time: 30 seconds

H. Aluminum Tunnels

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the tunnels—Stepper
    a. MASK 4-D
    b. Time: 1.4 second exposure
6. Develop in AZ351 Developer
    a. 4:1 DI H_2O:AZ351
    b. Time: 2.5 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the tunnels

10. Metal Deposition I—Thermal Evaporator
    a. Target Thickness: 5000 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.1
    f. Average deposition rate: 3.6 Å/s
    g. Maximum deposition rate: 5.6 Å/s
    h. Time: 30 minutes
    i. Thickness: 6463 Å
    j. Heat B12B Basket in other electrode (Pot setting: 4.0) for 20 minutes prior to deposition
11. Metal Deposition II—Thermal Evaporator
    a. Target Thickness: 3537 Å
    b. ~1.2 g aluminum
    c. S38A-A0-W Boat
    d. Start pot setting: 2.9
    e. End pot setting: 3.0
    f. Average deposition rate: 3.8 Å/s
    g. Maximum deposition rate: 5.0 Å/s
    h. Time: 15.5 minutes
    i. Thickness: 3555 Å
12. Metal lift-off and glass slide release in an ultrasonic bath in acetone
13. Rinse in IPA
14. Rinse in DI H_2O
15. Dry
16. Examine the tunnels
17. Measure the aluminum tunnel height

I. Photoresist Chimneys

1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
4. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
5. Expose the chimneys—Stepper
    a. MASK 6O-D and BLANK MASK
    b. Time: 2.0 second exposure
6. Develop in AZ Developer
    a. 1:1 DI H_2O:AZ Developer
    b. Time: 6.5–7 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the chimneys
10. Measure the aluminum tunnel and photoresist chimney heights

J. Neurocage Parylene-C

1. Cover the backside of wafer with dicing tape

2. Deposit Parylene-C
    a. Target thickness: 4 μm
    b. 6.0 g Parylene-C
    c. Approximate run time: 2 hours
    d. Actual thickness: 3.79 μm
3. Remove the dicing tape

K. Parylene-C Chimneys

1. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
2. Soft-Bake
    a. Temperature: 90°C
    b. Time: 40 minutes
3. Expose the Parylene-C chimney openings—Stepper
    a. MASK 7-D
    b. Time: 6.0 second exposure
4. Develop in AZ Developer
    a. Time: 6 minutes
5. Rinse in DI H_2O
6. Spin Dry
7. Examine the Parylene-C chimney openings

8. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 50%
    e. Pressure: 350 mTorr
    f. Etch rate: ~ 0.34 μm/minute
    g. 11–12 minutes (Rotating the wafer/glass slide 180° every 3 minutes)
9. Examine the Parylene-C chimney openings
10. Release the glass slide and strip the photoresist in ST-22 Stripper
    a. Temperature: 100°C
    b. Time: 10–15 minutes
11. Rinse in Post-Solvent Rinse
12. Rinse in DI H_2O
13. Rinse in IPA
14. Rinse in DI H_2O
15. Dry
16. Examine the Parylene-C chimney openings

L. Parylene-C Tunnels
1. Put AZ P4400 onto wafer and gently press glass slide onto wafer
2. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
3. Spin AZ 9260
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds

4. Soft-Bake
    a. Temperature: 85°C
    b. Time: 45 minutes
5. Expose the Parylene-C tunnel openings—Stepper
    a. MASK 8N-D/8T-D and BLANK MASK
    b. Time: 8.0 second exposure
6. Develop in AZ Developer
    a. Time: 3.75 minutes
7. Rinse in DI H_2O
8. Spin Dry
9. Examine the Parylene-C tunnel openings
10. Etch the Parylene-C—RIE
    a. Process #3
    b. Gas 3 (O_2): 100%
    c. Gas 4 (O_2): 60%
    d. Power: 50%
    e. Power: 350 mTorr
    f. Etch rate: ~ 0.27 μm/minute
    g. Time: 16 minutes (Rotating the wafer/glass slide 180° every 3 minutes)
11. Examine the Parylene-C tunnel openings

M. Final Cleaning and Dicing

1. Strip the photoresist and release the glass slide in acetone
2. Rinse in IPA
3. Rinse in DI H_2O
4. Dry
5. Examine

6. Etch the aluminum in Aluminum Etchant Type A
    a. Temperature: 60°C
    b. Time: 30 minutes
7. Rinse in DI H_2O
8. Dry
9. Examine
10. Spin AZ 9260 onto wafer and gently press glass slide onto wafer
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 1 krpm
    c. Hold time: 40 seconds
11. Bake
    a. Temperature: 100°C
    b. Time: 5 minutes
12. Spin AZ P4400
    a. Ramp rate: 0.5 krpm
    b. Spin speed: 2 krpm
    c. Hold time: 40 seconds
13. Soft-Bake
    a. Temperature: 100°C
    b. Time: 30 minutes
14. Dice glass slide
15. Strip the photoresist in acetone
16. Break the glass slide
17. Rinse in IPA
18. Rinse in DI H_2O
19. Dry
20. Examine