Chapter 1

Thesis overview

1.1 Nanotechnology and nanoelectronics

The rapidly expanding fields of nanoscience and nanotechnology are within the midst of an extraordinary period of scientific and technological productivity, due in no small part to the unprecedented collaboration of researchers from across the physical, chemical, biological, and life sciences. The promise of functional systems at the nanometer (nm) length scale (1–100 nm) has spurred researchers in diverse disciplines to engage in fruitful collaborations across traditional academic boundaries and between academia, industry, and government[1]. The result has been a modern-day scientific renaissance as the talents of chemists, physicists, biologists and engineers are simultaneously leveraged to understand and exploit novel phenomena and functionality particular to the nanometer size regime. Emerging applications of nanotechnology range from ultra-dense information storage[2] to sustainable water purification[3], to *in-vivo* biological sensors and intelligent drug delivery systems[4], to 'smart materials' capable of sensing changes to their external environment and responding accordingly[5].

An exciting sub-field of nanotechnology is nanoelectronics and, in particular, molecular electronics[6]. Interest in this field has been fueled by the realization that the

technologies and materials systems currently in use by the semiconductor microelectronics industry cannot sustain the forty-year-old trend of device miniaturization into the coming decades. Indeed, the microelectronics industry had to overcome significant technical barriers to achieve the sub-100-nanometer dimensions of today's transistors, and such barriers are becoming increasingly numerous and more difficult to overcome as device dimensions continue to shrink. This is highlighted by a recent assessment[7] of the technology requirements for future generations of integrated circuits, which forewarns the emergence of insurmountable technical barriers (either physical or economical) by as early as the year 2010.

This has led to a growing consensus that continued improvements in computational technology will likely occur through the development of alternative materials, patterning methods, and architectures[7, 8]. To that end, the Heath group began a research program with the intent to develop the required materials, methods, and circuit architecture to construct an ultra-dense molecular electronic computer. The Heath group 'vision' for such an integrated circuit is shown in Figure 1-1. The dominant theme of this circuit is the crossbar architecture[6], which consists of two perpendicularly overlaid arrays of high-density nanowires. These nanowires tile together the various computational elements of the circuit (logic, memory, etc.), which are themselves derived from unique electrically active thin-film materials sandwiched between the nanowires at the locations shown in the figure.

My research has focused on a number of the components shown in Figure 1-1 for realizing this multifunctional computational architecture. These have included the development of techniques for patterning ultra-high-density arrays of silicon nanowires

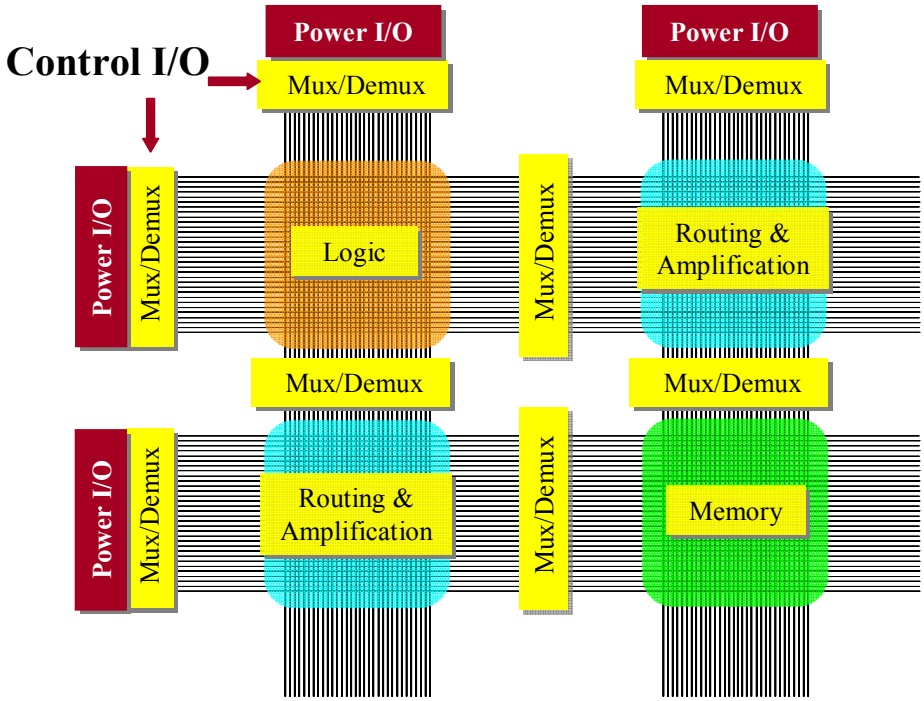

Figure 1-1. Schematic diagram of a nanoelectronic crossbar architecture. The various computational elements such as memory, logic, and routing are shown tiled together through nanowire arrays. Multiplexers (Mux) and/or demultiplexers (Demux) control signals within the circuit and to outside electronics (power I/O).

with precisely controlled electronic properties (Chapter 2), the demonstration of a field-effect transistor (FET)-based demultiplexer capable of bridging from the sub-micrometer length scales of conventional silicon microelectronic technology to the nanometer length scales of molecular electronics (Chapter 3), the integration of sub-lithographic patterning techniques and molecular materials for the fabrication of ultra-dense molecular electronic memory circuits (Chapter 4), and molecular-level control over nanoelectronic device surfaces (Chapter 5).

1.2 Organization of the thesis

To accommodate the largely independent, but closely related, projects which have comprised my graduate research in the Heath group at Caltech, I have chosen to organize this thesis into chapters—with each chapter completely self-contained and with its own background and references. The following sections will provide a brief overview the chapters in this thesis, summarizing the main results of the research described in each chapter and (hopefully) providing some overall unity to the topics discussed individually in the chapters.

1.2.1 Fabrication of ultra-dense nanowire arrays

In Chapter 2, I describe research directed towards the development of high-quality arrays of silicon and metallic nanowires. One-dimensional nanostructures such as nanowires are useful in a wide variety of applications in nanotechnology[9], and have emerged as the fundamental building blocks of novel nanoelectronic circuits. Such structures can be fabricated using highly parallel techniques and assembled into ultra-dense crossed-nanowire (crossbar) circuits such as shown in Figure 1-1. Nanowires not only propagate electrical signals throughout the circuit, but can also serve as the active components within the circuit. This dual functionality results in significant savings in wiring overhead, and enables crossed-nanowire circuits to be fabricated at the incredible densities I describe in Chapter 4.

There are a number of methods for the fabrication of silicon nanowires, with most based on the catalytic growth of nanowires from molecular precursors[9]. However, this technique has a number of significant drawbacks for application to large-scale nanoelectronic circuitry. For one, crossbar circuits fabricated from catalytically-grown nanowires are usually limited in size to around 10 micrometers, and to date have contained at most 100 junctions[10]. Additionally, the techniques required to align catalytically-grown nanowires are rather complicated and generally imperfect. This makes their integration with lithographically-defined structures such as binary tree decoder circuits (discussed in Chapter 3) awkward and difficult. Dr. Nick Melosh, a former post-doc in the Heath group, developed a method in which high-density arrays of silicon or metal nanowires could be patterned without such a limitation. This method is called the superlattice nanowire pattern transfer, or SNAP, technique and allows the fabrication of dense arrays of nanowires aligned over millimeter length scales.

Chapter 2 describes my efforts to systematically remove much of the phenomenology that had previously plagued the SNAP technique and the extension of SNAP to higher-density and larger-element arrays of nanowires. In addition, Chapter 2 will describe my efforts in developing reliable doping protocols and eliminating fabrication-induced nanowire defects to achieve bulk-like conductivity characteristics from narrow-width silicon nanowires.

1.2.2 Demultiplexing ultra-dense nanowire arrays

The SNAP technique is capable of producing arrays of metal and silicon nanowires with dimensions (width and pitch) beyond the capabilities of conventional lithographic techniques. However, such dense circuitry provides a new challenge for the field of nanoelectronics, namely, how to electrically address circuits that have characteristic wire dimensions and pitches that are smaller than the resolution achievable through lithographic patterning. The selective addressing of, and interaction with, individual nanostructures at high densities is one of the central challenges of both nanoscience and nanotechnology—in the absence of a resolution to this problem, many of the potential benefits of these emerging fields will remain unrealized. For instance, the nanowire-based molecular electronic memory circuit described Chapter 4 is nearly two orders of magnitude denser than conventional circuitry. However, the lack of a robust technology to selectively address individual nanowires from within an ultra-dense array reduces the effective density of such a circuit to that of conventional (lithographically-defined) circuitry.

Chapter 3 describes research by my co-workers (Dr. Robert Beckman, Dr. Ezekiel Johnston-Halperin and Dr. Yi Luo) and me to demonstrate a FET-based nanowire demultiplexing architecture that can be patterned with significantly larger dimensions than the nanowires it addresses, and with wide alignment tolerances. Its shown that this architecture successfully interfaces with high-density SNAP-fabricated nanowires to bridge the dimensional gap between nanometer-scale circuitry and conventional patterning technology[11].

1.2.3 Ultra-dense crossbar molecular electronic circuits

In 2002, the Heath group reported on the use of bistable [2]rotaxane molecules as the active elements within a 64-bit molecular electronic random access memory (RAM) circuit that utilized micrometer-scale wiring[12]. Although this work successfully demonstrated that molecules could be used store information within a solid-state crossbar circuit, it did not take advantage of the unique scalability offered by molecular components.

Chapter 4 is devoted to what has comprised the majority of my research efforts in the Heath group, namely, the integration of SNAP-fabricated arrays of silicon and metal nanowires with molecular materials for the fabrication of an ultra-dense, 160,000-bit molecular electronic crossbar memory circuit patterned at a record density of 100 gigabits per square centimeter (1×10^{11} bits cm^{-2})[13]. The construction of this memory circuit was a true *tour de force* in nanofabrication that would not have been possible without the efforts my colleague, Jang Wook Choi. In addition, numerous other members of the Heath and Stoddard group (at UCLA) made important contributions to this effort[13].

Beginning with a description of the rich science underlying the switching mechanism of bistable [2]rotaxane molecules and their integration into high-density crossbar architectures, Chapter 4 covers, in depth, the fabrication and operation of the memory circuit. The work described in this chapter shows that molecules *can* be used as scale-invariant components in solid state circuitry and, moreover, that functional circuitry *can* be assembled at macromolecular dimensions. A false-colored image of a typical molecular memory circuit is shown in Figure 1-2.

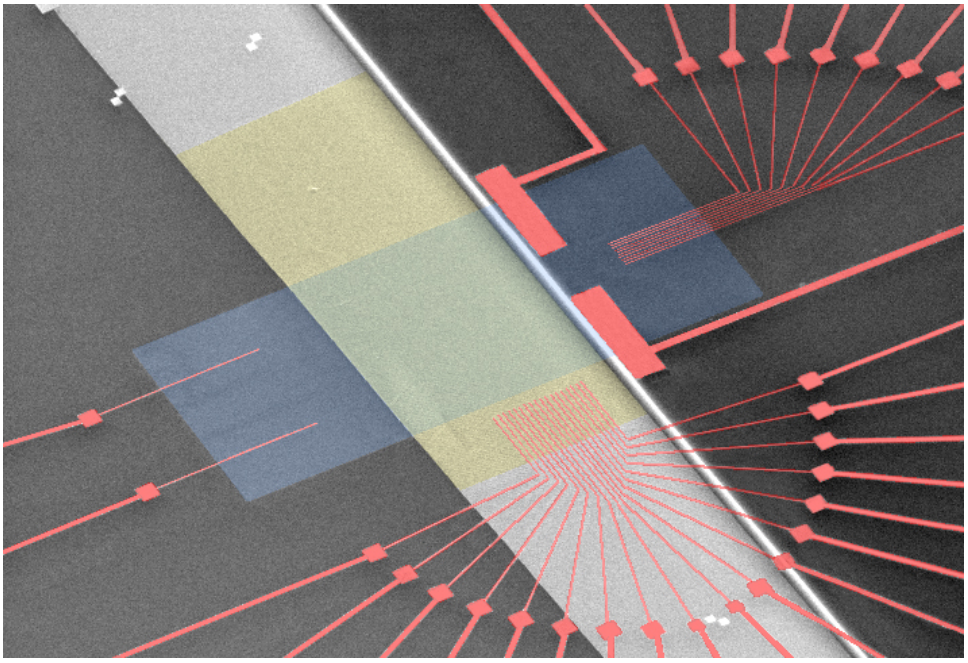

Figure 1-2. A false-colored scanning electron micrograph of a molecular electronic memory circuit fabricated from [2]rotaxane molecular materials and SNAP-fabricated silicon and titanium nanowires. The memory region is defined by the intersection of 400 silicon nanowires (light blue) and 400 titanium nanowires (light yellow), and contains 160,000 bits in an area of 13×13 square micrometers (or 1×10^{11} bits per square centimeter).

1.2.4 Covalent modification and electrical characterization of silicon-on-insulator devices

As the feature sizes of silicon devices continue to be scaled towards nanometer dimensions, the physical and chemical properties of the surface play an increasingly prominent role in determining the overall device behavior. This has presented significant challenges, and opportunities, to the nanotechnology community, where surface effects manifest over a range of applications from nanoelectromechanical systems (NEMs)[14] to electrical transport in thin silicon-on-insulator (SOI) films[15].

Covalent alkyl passivation of silicon surfaces is attractive for a variety of nanoelectronic applications, such as FET-based demultiplexing and molecular electronics. However, the majority of work with alkyl-passivated, (111)-oriented silicon surfaces has utilized bulk wafers. While such wafers are convenient for surface characterization studies, they are less useful for the nanoelectronic applications of interest to us, where SOI structures are generally required. This last chapter of my thesis describes ongoing work to obtain high-quality methyl passivation of ultra-thin (111)-oriented SOI devices and their subsequent electrical characterization using variable-temperature conductivity and mobility measurements. Using an optimized (for SOI devices) version of the surface methylation protocols developed by the Lewis group at Caltech[16], robust methyl passivation of silicon surfaces was achieved with devices as thin as 20 nanometers thick. Chapter 5 presents data showing that this passivation is resistant to oxidation for extended periods of time in ambient air, and after exposure to an assortment of common nanofabrication procedures and chemical treatments. Additionally, temperature-dependent mobility data shows that methylated ultra-thin surfaces can be prepared with bulk-like mobility characteristics.

1.3 References

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