SILICON NANOWIRES AND SILICON/MOLECULAR INTERFACES FOR NANOSCALE ELECTRONICS

Thesis by

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In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

CALIFORNIA INSTITUTE OF TECHNOLOGY

Pasadena, California

2009

(Defended June 11, 2008)

To my best friend and husband,

Bryan

Acknowledgements

I am so grateful to the many people who enriched my experiences at Caltech. First, I would like to thank my advisor, Professor Jim Heath, whose dedication to the pursuit of scientific understanding has been truly inspirational. I am indebted to his support and guidance over the last 5 years. I also would like to thank my thesis committee for their support and insights into my graduate research: Prof. Mitchio Okumura, Prof. Pat Collier, and Prof. Bill Goddard.

I was blessed to be surrounded by many excellent colleagues. I would like to acknowledge the support and assistance of several current and past Heath group members: Dunwei Wang, whom I learned so much from; Yi Luo, a true mentor for so many; and Johnny Green, Erica DeIonno, Gabe Kwong, Rosemary Rohde, Heather Agnew Akram Boukai, Habib Ahmad, Kris Beverly, Ryan Bailey, Mike McAlpine, and John Nagarah, for their friendship, guidance, and for making going to work so much fun. I also would like to thank Rosemary Rohde and Heather Agnew for their help with surface chemistry techniques and acknowledge Will Dichtel, Jason Spruell, and Dorota Rozkiewicz for their contributions with the microcontact printing project. Thanks to Ruo-Gu Huang, Peigen Cao, and Clara Ji-Hyun Cho for continuing the logic and microcontacting printing projects. I owe a big thanks to Diane Clark-Robinson for running the group efficiently and for keeping things interesting, and Kevin Kan, the guardian of the cleanroom and its equipment.

When I was an intern at Intel, I had the pleasure of working with several friendly and extremely helpful colleagues. In particular, I would like to thank Juanita Kurtin,

Janice Lee, Keith Bowman, Ravi Pillarisetty, and Tanay Karnik. I would also like to acknowledge the Intel Foundation for providing financial support during the last two years here in the form of a Ph.D. Fellowship.

I would like to acknowledge my friends at Caltech who made my experiences here so much better. In particular, I would like to thank Heather Wiencko, Christina Vizcarra, and Amie Boal for their support and friendship.

Finally, I would like to thank my husband, Bryan, who has been a source of unlimited love, friendship, laughter, support, and motivation.

Abstract of the thesis

The thesis describes the realization of high-performance silicon nanowire (Si NW) logic circuits and a novel surface modification technique for nanoscale electronics applications. First, doped Si NWs were generated via the superlattice nanowire pattern transfer (SNAP) process, forming aligned, uniform, ultra-dense NW arrays. The NWs served as the channel material for field-effect transistors. NWs could be doped n- or p-type using a diffusion doping process and both n-FETs and p-FETs could be fabricated simultaneously on the same substrate.

Individual p-FETs exhibited excellent performance metrics compared to other NW and carbon nanotube (CNT) transistors, including high on/off ratios, low off currents, high mobilities, and low subthreshold swings. The n-type devices also had good characteristics, although they did not perform as well as the p-FETs. A comparison of nanowire and microwire device performance revealed that the NW FET performance was dominated by the high surface-area-to-volume ratio. These devices were integrated into complementary symmetry (CS) inverter circuits, which showed a consistent performance and a gain (a measure of performance) of ~ 5.

Circuit performance was optimized by utilizing a methodology that combined prototype devices with circuit simulations. First, prototype devices were fabricated and their DC and AC characteristics were tabulated into a look-up-table model. This model was accessed by a circuit simulator, which could predict the performance of arbitrary circuits utilizing these devices and provide feedback into the device design. Circuits could then be fabricated from the optimized devices resulting in increased performance.

This methodology was demonstrated by optimizing the gain of the CS inverter circuit from an initially measured value of 8 to a gain of 45.

A novel microcontact printing method was developed to functionalize gold and silicon surfaces. The copper^{I}-catalyzed azide-alkyne cycloaddition (CuAAC) reaction was used to covalently attach molecules containing an alkyne functional group to azide-terminated monolayers on gold or silicon. The copper^{I} catalyst in the ink solution (homogeneous catalyst) was replaced by coating the elastomer stamp with copper metal (heterogeneous catalyst). The copper-coated stamp was shown to catalyze the reaction to completion within 1 hour with a zero-order reaction rate. In comparison, the homogeneous catalyzed stamp reaction took ~ 30 minutes to complete with a pseudo first-order reaction rate. No pattern diffusion was observed, suggesting that free copper ions are not responsible for the catalysis. It is proposed that this method can be used to sequentially synthesize electronically active molecules directly onto gold or silicon electrodes.

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