THE APPLICATION OF TUNNEL DIODES TO SWITCHING AND LOGICAL CIRCUITS

Thesis by

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PART 1

In this thesis the tunnel diode is considered as an active device having an equivalent electrical circuit of figure 1.1. Even though this equivalence has been accepted for some time now some simple tests were made and comparisons between theoretical and experimental results are in good agreement. The theoretical results were obtained by integration of the non linear differential equations. The Burroughs 220 computer was employed and a special compiler was developed to simplify the analysis. The compiler was also used for subsequent analysis which was often resorted to when the construction of the circuits became a difficult and time consuming task. It can be employed for any planar, and many non planar, tunnel diode circuits and a complete description is given in Appendix 1.

Measurement of Parameters

The techniques employed to measure the four parameters of figure 1.1 were:

1) R_s, the equivalent series resistance, is determined by back biasing the diode heavily and measuring the slope of the V-I characteristic. While this may not be a very accurate method it does put an upper bound on the value of R_s. In the great majority of cases R_s was so small that it could have little effect on the performance of the diode as a circuit element.[1] As an example the value of R_s for an experimental germanium diode produced by Bell Laboratories (GO 1032 -- peak current 10 mA) was 2 ohms.

2) R, the equivalent nonlinear resistance is obtained from the V-I characteristic. In the negative resistance range the diode must be stabilized and the conventional method of shunt resistance and compensation for the shunt resistance current was employed.

3) L_s and C, the equivalent series inductance and shunt capacity, were determined by calculation from slotted line measurements. L_s and C were found to be independent of frequency.

The capacity C closely followed the analytical expression

$$C = \frac{Co}{\sqrt{1 - (V/V_g)}} \qquad (1.1)$$

where C_o, V and V_g are the capacity at zero bias, the diode voltage and the energy gap of the intrinsic material respectively. (e. g. V_g = 720 mV for germanium) Figures 1. 2, and 1. 3 and 1. 4 show experimental results for the variation of C with V for three diodes together with the corresponding theoretical values derived from equation 1. 1. The values of L_s obtained were rarely greater than 2mμHenries.

A Switching Experiment

The behavior of the diode under switching conditions was examined experimentally for correlation with predicted behavior. A first attempt using a step input as the driving function was abandoned because the diode switched so rapidly that the sampling scope's rise time limitations obscured the diode's true behavior. A more meaningful test was finally performed in which the diode was driven by a ramp input and permitted to oscillate during the transient response. The frequency and amplitude of the oscillations are directly related to the diode parameters. The test circuit is shown schematically in figure 1. 5 which can be reduced to the equivalent circuit of figure 1. 6. In figure 1. 6

R_t = Thevenin equivalent resistance of the test circuit = 40. 18 ohms (measured).

C_t = Lumped parasitic capacity of the test circuit = 10 pF (estimated). The value of C_t had essentially no effect on the analytic solution over an extremely wide range of values .

L_t = Lumped parasitic inductance of the test circuit = 5 - 6 mμH.

L_m = Lumped parasitic inductance of the diode mount = 2 mμH.

R_L and C_L = An approximation to the scope delay.

R_L = 800 ohms C_L = 0.5 pf. (Load on circuit negligible).

The diode (V-I characteristic on figure 1.7) was represented by its equivalent circuit and the diode capacity was assumed constant at 2.5 pf. A comparison of experimental and analytical results is shown on figure 1.8 and clearly good agreement was obtained. The deviation at the higher values of the voltage was attributed to the increase in the diode capacity (equation 1.1).

Even though the diode capacity is voltage dependent (figure 1.4) for the analysis it was assumed constant and equal to the valley capacity. The compiler operates on this assumption and since the diode voltage will rarely exceed this value by more than 50 mV the rise and fall times of the diode will be overestimated thus guaranteeing an error (if any) on the conservative side and making a certain allowance for diode to diode variation of the capacity.

Other results given in the following sections of this thesis will provide further support for the validity of the equivalent circuit.

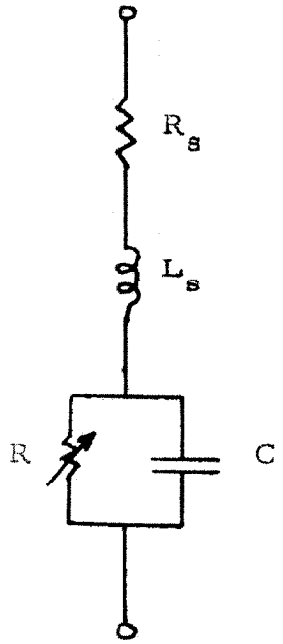

Figure 1.1:- The equivalent circuit of the tunnel diode

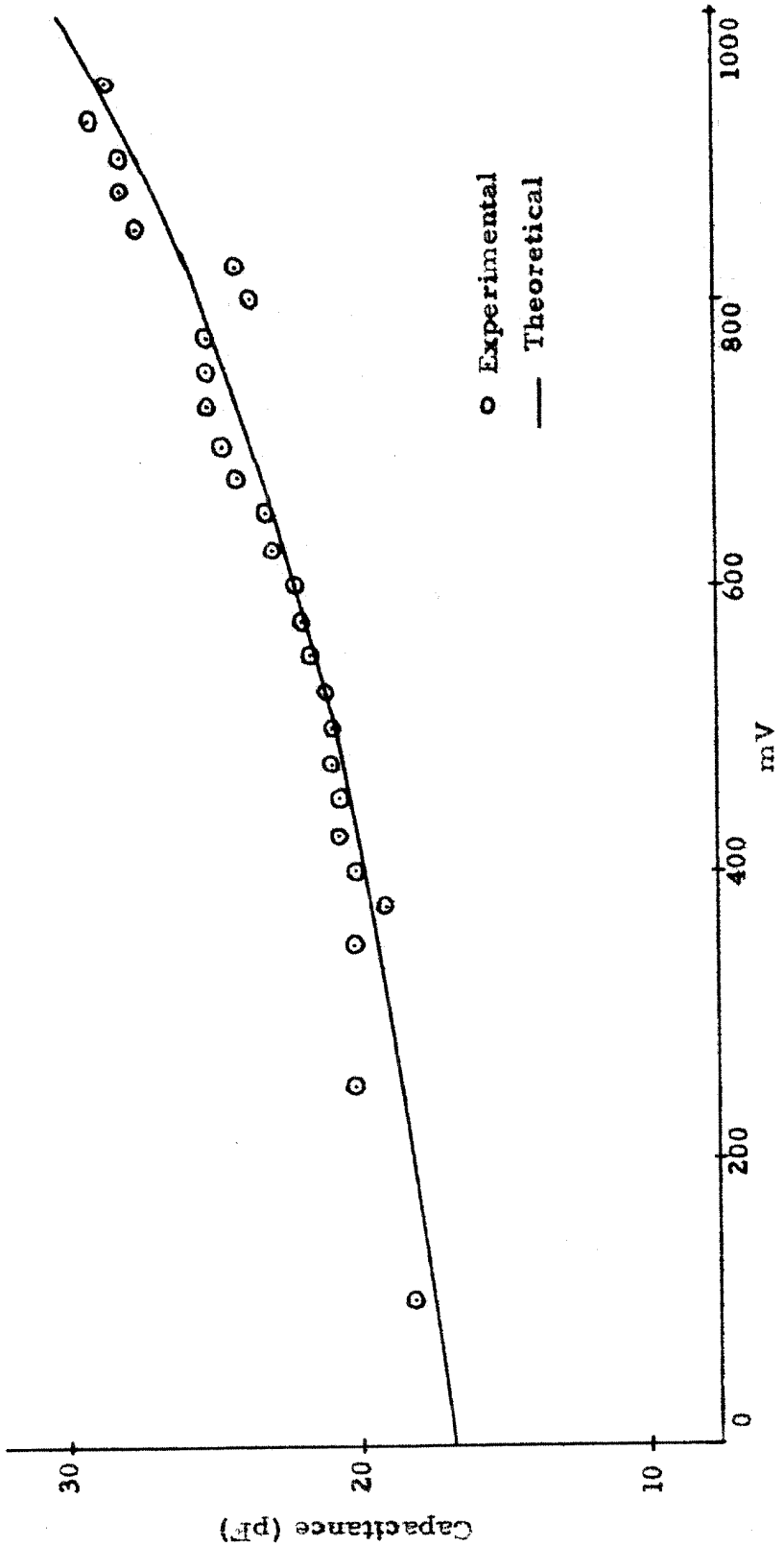

Figure 1. 2;- Capacitance vs. Voltage - Texas Instruments GaAs Diode

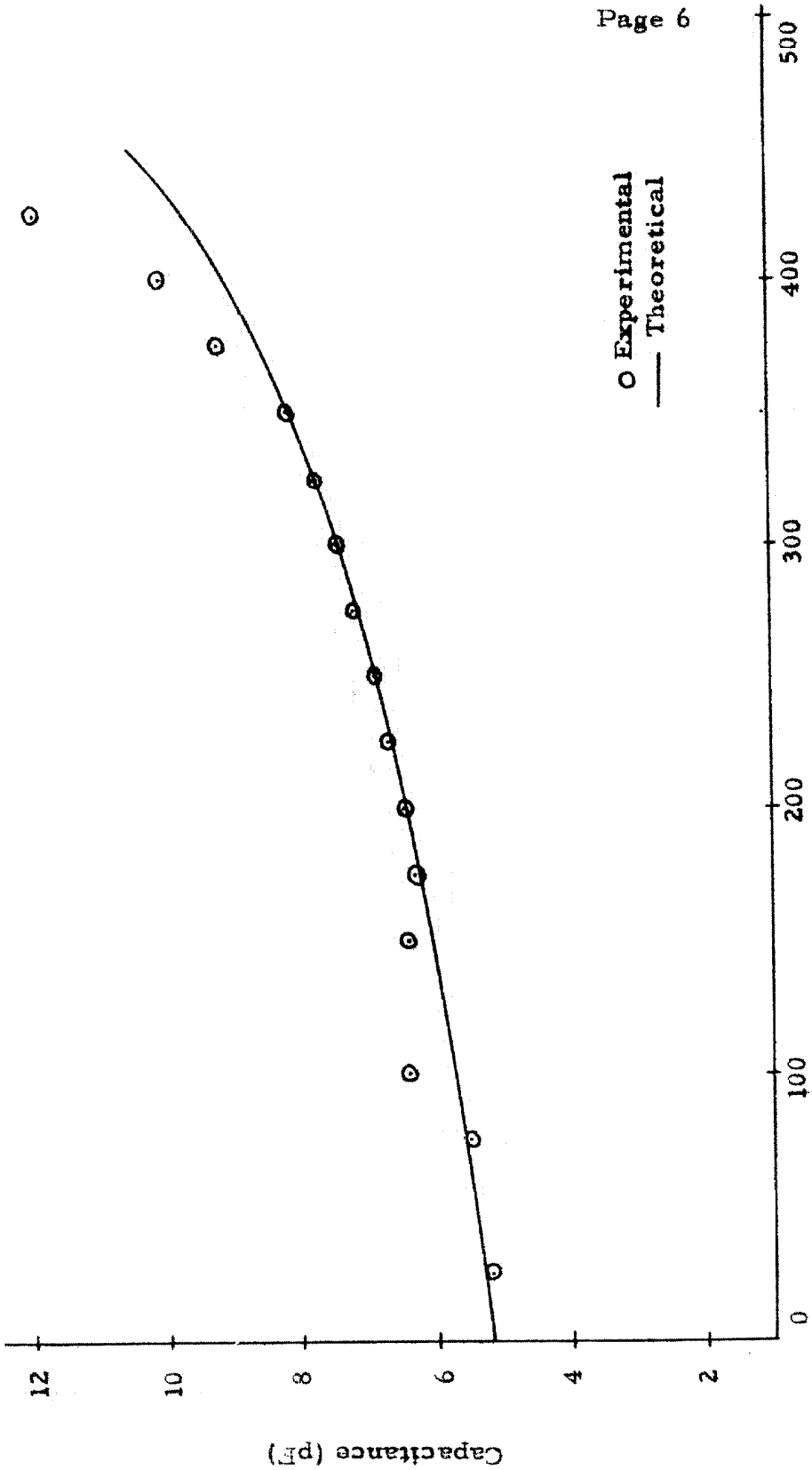

Figure 1.3:- Capacitance vs. Voltage - GE Germanium diode 2J56

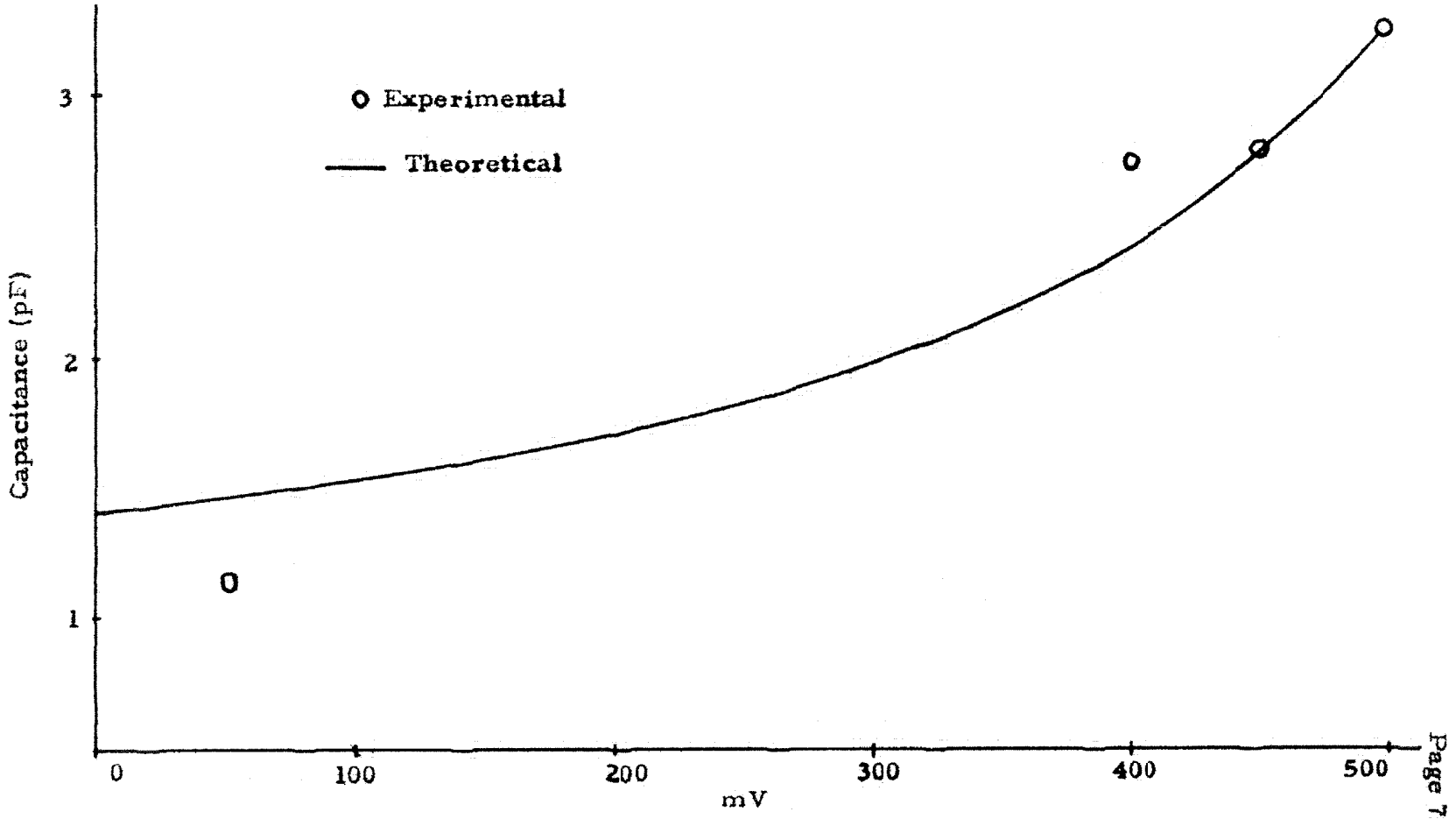

Figure 1.4:- Capacitance vs. Voltage - Bell GO 1032

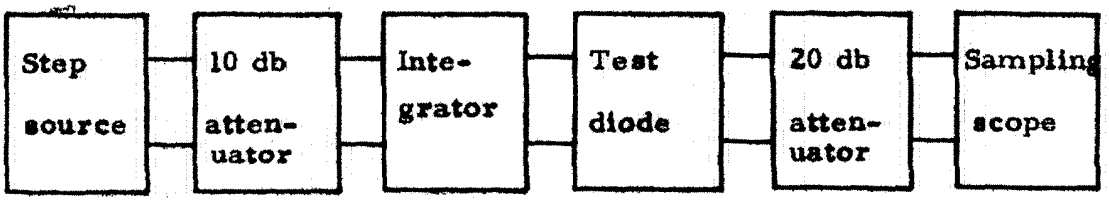

Figure 1.5:- Test circuit for a ramp input

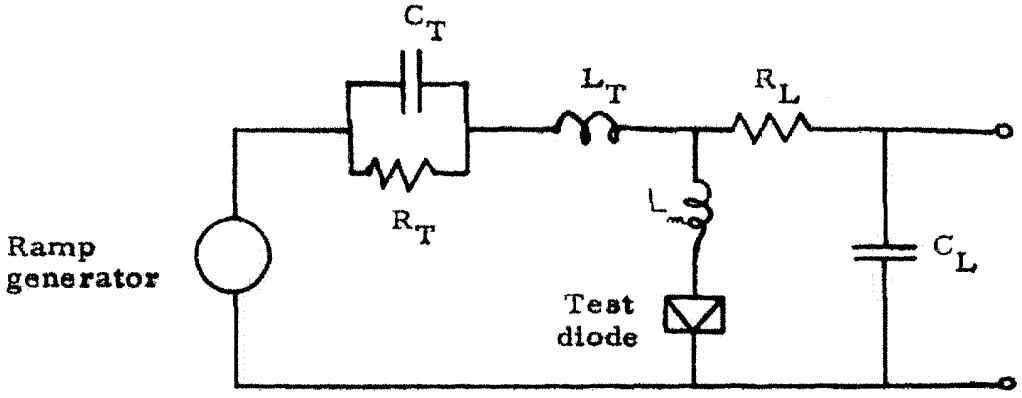

Figure 1.6:- The electrical equivalent of figure 1.5

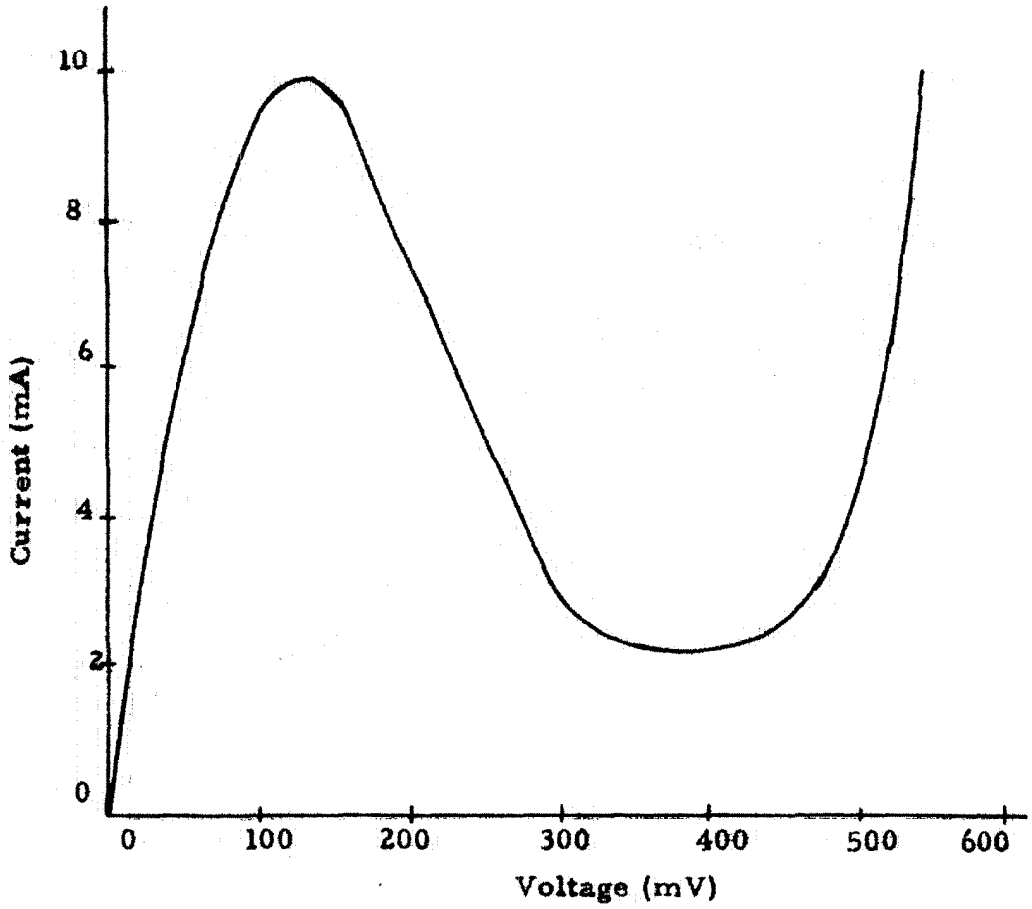

Figure 1.7:- V-I Characteristic of Bell GO1032

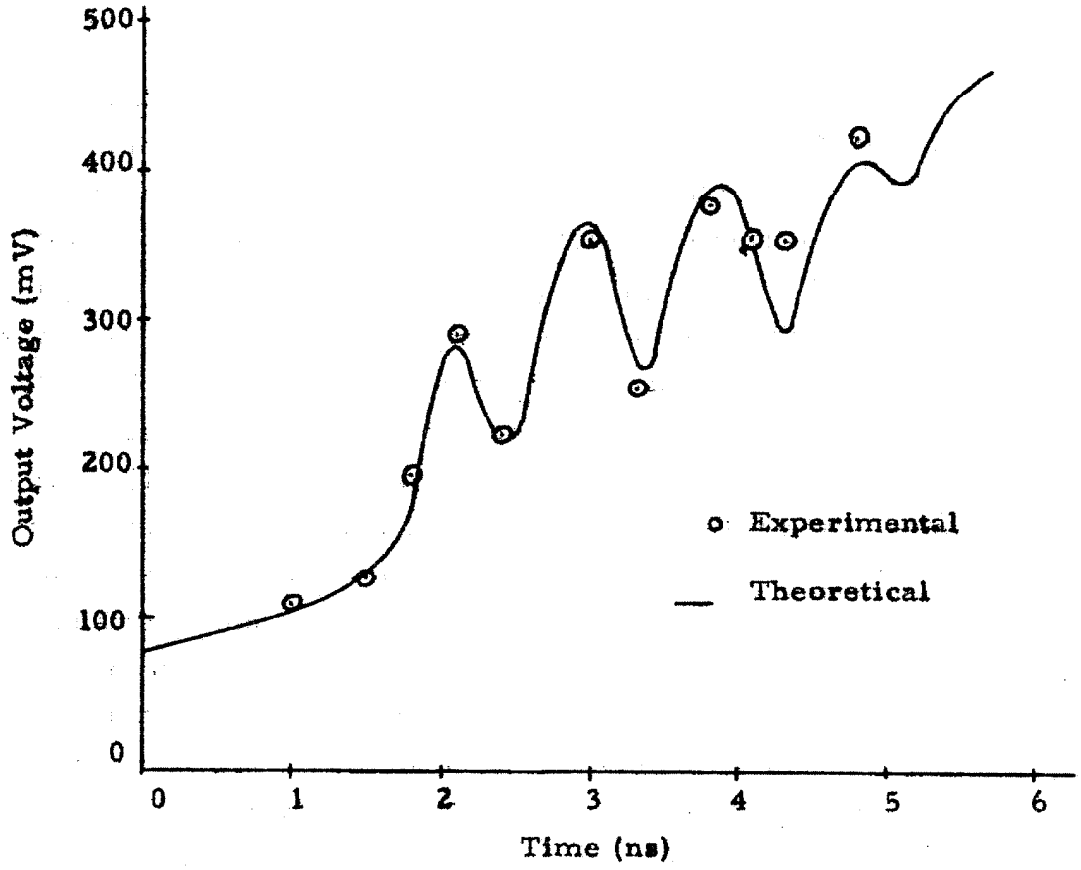

Figure 1.8:- Bell GO 1032 response to a ramp input

PART 2

TUNNEL DIODE SWITCHING CIRCUITS

(A) Basic Considerations

Consider a tunnel diode in series with a linear impedance Z(s) and driven by an ideal voltage generator as shown in figure 2.1. Suppose now that Z(0) = R. Static load lines can be drawn for different values of R and for different values of the supply voltage E (considered as a D.C. supply). These will usually result in either one or three points of intersection with the diode characteristic. At any voltage between the peak and valley voltages of the T.D. the dynamic diode resistance R_D is negative. Let Rmin be the minimum value of $/R_D/$ in this range. Clearly if R < Rmin only one point of intersection is obtained which may be stable as in (2) and (2B) of figure 2.3. (The stability or instability in case (2A) cannot be determined from static considerations.) If R > Rmin there will be one stable intersection point as in (1A) and (1B) of figure 2.2 or two stable and one unstable point as in (1) of figure 2.2.

Following a disturbance the locus of the diode current can be plotted against the capacitor voltage by solving the non-linear differential equations. This locus will be called the dynamic trajectory. Much information can be obtained about this trajectory without directly solving the differential equations if Z(s) has a simple form. Suppose $Z(s) = R + L_m S$ as shown on figure 2.4 and let the disturbance be introduced in the form of a step increase in E from E_0 to E_1 as shown on figure 2.5. With this step increase in E the current and the voltage of the dynamic trajectory increase from their initial values (Point N) to those at Q. Once Q is reached the voltage will continue to increase but the current will decrease monotonically until R is reached. Afterwards the current and voltage will approximately follow the diode characteristic towards S.

For any point A on the dynamic trajectory between N and S the following equations can be written.

$$\frac{dV}{dt} = \frac{I - I_d}{C} \qquad (2.1)$$

$$\frac{dI}{dt} = \frac{V_I - V}{L_m + L_s} \qquad (2.2)$$

Equations 2.1 and 2.2 are the parametic equations of the dynamic trajectory. At N, R and S $\frac{dV}{dt} = 0$ but at S $\frac{dI}{dt}$ is also zero. Accordingly at N and R the dynamic trajectory has an infinite slope but the same is not usually true at S. The current is a maximum at Q and from equation 2.2 once the trajectory passes through the load line (at Q) the current will always exceed the load line current for any value of the voltage.

The dynamic trajectory has associated with it, a third variable, namely time. Let (V, I, t) be any point on this trajectory. At time t the output voltage (i.e. that between A and B in figure 2.4)is given by the equation

$$Vout = V + R_s I + \Delta V \frac{L_s}{L_m + L_s} \qquad (2.3)$$

where

$$\Delta V = E - (R + R_s) I - V \qquad (2.4)$$

Note that ΔV is the horizontal distance between the dynamic trajectory and the load line ($\Delta V = V_I - V$ on figure 2.5) and is accordingly divided between the inductors L_m and L_s in proportion to their magnitudes. Note also the ΔV has a positive maximum at N (figure 2.4) is zero at Q and is negative between Q and R.

A diode, whose parameters and characteristics are given in figure 2.6 in series with a 34 ohm resistor and an inductor L_m and

operating at the point N (see figure 2.6) has its driving voltage E increased at t = 0 from 700 to 800 mv. Some computed dynamic trajectories and their corresponding output voltages are shown on figures 2.7 and 2.8 respectively.

The output voltage has the peculiar property of decreasing after the initial positive output step (output step is equal to $\frac{L_s}{L_m + L_s}$ that of the input). The explanation lies in the fact that

$\Delta V \frac{L_s}{L_m + L_s}$ at first decreases more rapidly than $V + R_s I$ increases (see equation 2.3). Mathematically it can be shown that

$$\frac{dVout}{dt} = \left[\left(\frac{dV}{dI} + R_s\right)\left(1 - \frac{L_s}{L_m + L_s}\right) - R\right]\frac{dI}{dt} + \frac{L_s}{L_m + L_s}\frac{dE}{dt} \qquad (2.5)$$

For $t > 0$ $\frac{dE}{dt} = 0$ so $\frac{dVout}{dt}$ will have opposite sign to $\frac{dI}{dt}$ unless

$$\frac{dV}{dI} > R\,(1 + L_s/L_m) - R_s \qquad (2.6)$$

Since $\frac{dV}{dI}$ is the reciprocal of the slope of the dynamic trajectory at $t = 0$, $\frac{dV}{dI} = 0$ and since $\frac{dI}{dt} = \frac{\Delta V}{L + L_s} > 0$, $\frac{dVout}{dt}$ is negative ($R >> R_s$) and will remain negative until equation 2.6 is satisfied by equality. Suppose that equation 2.6 is satisfied by equality at time $\bar{t}$ i.e. that Vout $(\bar{t})$ is a minimum point.

The two important characteristics of the "oscillation" are:-

1. The amplitude of the "oscillation" A. (A = Vout (0 +) - Vout $(\bar{t})$).*
2. The time it takes the output voltage to reach a minimum (i.e. the time $\bar{t}$).

* See figure 2.8

For values of R >> Rmin the minimum output voltage will occur at a point very close to point Q (figure 2.5) of the dynamic trajectory. Calling ΔE the input step for R >> Rmin

$$A \doteq \frac{L_s}{L_m + L_s} \Delta E$$

and $\bar{t}$ will, for a given ΔE and values of the diode parameters except L_s, depend on the sum of the inductors L_m and L_s. Consequently for values of R >> Rmin and a step input it should be possible to match theory and experiment to determine the values of the inductors L_m and L_s.

However, when R is not so large the minimum value of voltage deviates considerably from that of Q (figure 2.5) and depends on the dynamic trajectory and hence on the sum of the inductors as well as on their ratio (equation 2.6). The time $\bar{t}$ will then depend on the ratio of the inductors as well as on their sum. Furthermore if the input step has a rise time the amplitude of the oscillation (A) will be reduced by a factor depending on the sum of the inductors.

Since in practise the input step must have a rise time and from bias voltage and gain considerations R should not be greater than 4 or 5 times Rmin the values of L_m and L_s will in most cases be indeterminate from the amplitude of the oscillation and the time $\bar{t}$. Indeed in most cases the circuit parameters will be such that there will be no such oscillation in the output pulse.

To illustrate the occurrence of such an oscillation in practise an experiment was set up where Z(s) (figure 2.1) was a purely resistive delay line and L_s could be artificially increased. The circuit and diode mount are shown in figures 2.9 and 2.10. The extent to which L_s is incremented depends on x and d (figure 2.10) and output pulses for different values of the effective value of L_s are shown on figure 2.11. A 20 mA R.C.A. stripline tunnel diode was used with zero d.c. bias.

(B) The Switching Time

1. The Effect of the Load Line and the Percentage Bias.

If inductance and stray capacitance are negligible the dynamic trajectory follows the load line as is illustrated in figure 2.12 for a switch from the low to the high state when the driving voltage experiences a step increase from E_0 to E_1 at t = 0. At any point (V, I, t) on the dynamic trajectory the equation

$$\frac{dV}{dt} = \frac{I_c}{C_D}$$

is valid where I_c is dependent on V as shown on figure 2.12.** Consequently the time (t_{1-2}) required for the voltage to increase from V_1 to V_2 is

$$t_{1-2} = C_D \int_{V_1}^{V_2} \frac{dV}{I_c} \qquad (2.6a)$$

In general the selected values of V_1 and V_2 will depend on the application of the switch. V_1 and V_2 might for instance be the 10 and 90% points if the switch is used as a pulse generator. However in logical circuits the initial delay (0 to 10% say) is also important and numerically we shall consider only the 0 to 90% time.* (i.e. figure 2.12 $V_1 = V_N$ and $V_2 = V_N + 0.9\ (V_H - V_N)$.

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* Strictly speaking we shall consider the 0 to 90% rise time of the diode capacitor voltage but since R_s is much less than R_L this will be very close to 0 to 90% rise of the output voltage.

** Other symbols appearing later in the text (some illustrated in figure 2.12) are defined in the "Partial Table of Symbols" (Pages 140-142).

Equation 2.6a can be written in the form

$$t_{1-2} = \frac{C_D}{I_p} \int_{V_1}^{V_2} \frac{dV}{(I_c/I_p)}$$

i.e.
$$\frac{t_{1-2}\, I_p}{C_D} = \int_{V_1}^{V_2} \frac{dV}{(I_c/I_p)} \qquad (2.7)$$

Since the characteristics of a given type of tunnel diodes (e.g. germanium diodes) can be expressed in the form

$$I = I_p\, f(V)$$

where $f(V)$ is independent of I_p the integral on the right of equation 2.7 is independent of I_p and for fixed limits depends only on E_0, E_1 and the % bias. (See footnote on Page 17)

Defining the parameter τ by the equation

$$\tau = \int_{V_N}^{V_2} \frac{dV}{(I_c/I_p)} \qquad (2.8)$$

where

$$V_2 = 0.9\, V_{II} + 0.1\, V_N$$

the zero to 90% rise time (t) then is

$$t = \tau\, \frac{C}{I_p} \qquad (2.9)$$

Also from equation 2.8 and figure 2.12 it is easily seen that

$$\tau = f\,(E_0,\ E_1,\ \%\ \text{Bias}).$$

Furthermore if the gain G is defined by the equation

$$G = \frac{V_H - V_N}{E_1 - E_0} \qquad (2.10)$$

then

$$\tau = \phi\ (E_0,\ G,\ \%\ \text{Bias}) = \int_{V_N}^{0.9\ V_H + 0.1 V_N} \frac{dV}{(I_c/I_p)} \qquad (2.11)$$

By performing the integration τ can be evaluated for various values of the % Bias,* E_0 and G. The percentage bias and E_0 determine the load line since

$$R_L = \frac{E_0 - V_N}{I_N} = R_s + R \qquad (2.11a)$$

where R and R_s are the external load and the series resistance of the diode respectively. V_H can then be determined graphically or analytically and then

$$I_c = I - I_d = (E_1 - V) / R_L - I_p f\ (V)$$

or

$$I_c / I_p = \frac{1}{I_p R_L} (E_0 + \frac{V_H - V_N}{G} - V) - f\ (V)$$

i. e.

$$I_c/I_p = \frac{I_N}{I_p} \quad \frac{1}{E_0 - V_N} (E_0 + \frac{V_H - V_N}{G} - V) - f\ (V) \qquad (2.12)$$

By dividing the V axis into a number of intervals and approximating f (V) in each interval by a quadratic or linear function of V the intergration of equation (2. 11) can be performed analytically. Using four regions as illustrated in figure 2. 13, a very good approximation to f (V) is obtained in the range of interest.

Using the notation of figure 2. 13 it will be assumed that f(V) has the form

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* The % Bias is defined as $100\ I_N/I_p$ where I_N and I_p are the bias current and tunnel diode peak current respectively.

$$f(V) = \begin{cases} a_1 + b_1 (V - V_p)^2 , & V_1 \le V \le V_1^1 \\ I_2 + m (V_2 - V) , & V_1^1 \le V \le V_2 \\ a_2 + b_2 (V - V_v)^2 , & V_2 \le V \le V_v \\ a_3 + b_3 (V - V_v)^2 , & V_v \le V \le V_3 \end{cases} \tag{2.13}$$

where

$$a_1 = 1, \quad a_2 = a_3 = I_v, \quad b_1 = - \frac{1 - I_1}{(V_p - V_1)^2}, \quad m = \frac{I_1 - I_2}{V_2 - V_1^1},$$

$$b_2 = \frac{I_2 - Iv}{(V_v - V_2)^2} \quad \text{and} \quad b_3 = \frac{I_3 - I_v}{(V_v - V_3)^2}.$$

The integration of (11) then gives

$$\begin{aligned} \tau = & \frac{1}{b_1(\alpha_{11} - \alpha_{21})} \log_e \left| \frac{V_1^1 - \alpha_{11}}{V_1^1 - \alpha_{21}} \cdot \frac{V_N - \alpha_{21}}{V_N - \alpha_{11}} \right| \\ & + \frac{1}{A} \log_e \left(\frac{V_2 + B/A}{V_1^1 + B/A} \right) \\ & + \frac{1}{b_2(\alpha_{12} - \alpha_{22})} \log_e \left| \frac{V_v - \alpha_{12}}{V_v - \alpha_{22}} \cdot \frac{V_2 - \alpha_{22}}{V_2 - \alpha_{12}} \right| \\ & + \frac{1}{b_3(\alpha_{13} - \alpha_{23})} \log_e \left| \frac{V_f - \alpha_{13}}{V_f - \alpha_{23}} \cdot \frac{V_v - \alpha_{23}}{V_v - \alpha_{13}} \right| \end{aligned} \tag{2.13a}$$

where α_{1i} and α_{2i} are the roots of the quadratics

$$\begin{cases} a_i + b_i (V - V_p)^2, & i = 1 \\ a_i + b_i (V - V_v)^2, & i = 2, 3 \end{cases},$$

$$A = m - \frac{I_N}{E_0 - V_N},$$

$$B = \frac{I_N}{G(E_0 - V_N)} \quad (GE_0 + V_H - V_N),$$

and $V_f = 0.9V_H + 0.1V_N$ if $V_f \geq V_v$.

If $V_f < V_v$ then the 4th term in equation 2.13 is omitted and in the 3rd term of the same equation V_v is replaced by V_f. Finally V_H is determined from the expression

$$V_{Hi} = V_v - \frac{I_N}{2_{bi}(E_0 - V_N)} + \sqrt{\left(V_V - \frac{I_N}{2_{bi}(E_0 - V_N)}\right)^2 - \frac{I_v}{b_i} + \frac{E_0 I_N}{b_i(E_0 - V_N)}} \quad (2.14)$$

In equation 2.14 if $V_{H3} > V_v$ then $V_H = V_{H3}$ but if $V_{H3} < V_v$ then $V_H = V_{H2}$.

The values of τ as given by equation 2.13a were evaluated for a germanium diode whose V - I characteristic was approximated by equation 2.13 with the parameter values given in figure 2.13. The computation was performed on the Burroughs 220 computer for three different values of the % bias (92.5, 95 and 97.5%) and the results are plotted on figures 2.14a, 2.14b, and 2.14c. These results quantatively express the dependence of τ on E_o and the percentage bias. They show that the minimum value of τ is obtained with a unique value of E_o when the % bias and gain G are fixed. This value of τ and the corresponding value of E_o can be read or interpolated from figures 14 when the gain G and % bias are known. As an example the minimum value of τ is 1.5 mμ secs/pF/ mA when G = 6 and 95% bias is employed. This minimum value of τ occurs when E_o = 500 mV and using this result in conjunction with equation 2.9 the minimum zero to 90% rise time for a 20 mA, 10 pF tunnel diode with a gain of 6 and 95% bias is equal to $1.5 \frac{10}{20} = 0.75$ mμ secs.

On figure 2.12 as E_1 decreases and consequently as G increases the value of τ increases and eventually approaches infinity

when the dynamic trajectory becomes tangent to the diode characteristic. The value of G corresponding to this infinite value of τ will be called Gmax and it is dependent on the percentage bias and E_0.

The results of figures 2.14 can be applied to any single diode circuit with linear resistive elements. Using Thevenin's theorem the circuits of figure 2.15a and b are equivalent if

$$\frac{1}{R} = \frac{1}{R_o} + \frac{1}{R_1} + \frac{1}{R_2} \qquad (2.16a)$$

and

$$E_o = E_1 \frac{(R_2R_o) \;/\; (R_2 + R_o)}{R_1 + (R_2R_o)/(R_2 + R_o)} + E \frac{(R_1R_2) \;/\; (R_1 + R_2)}{R_o + (R_1R_2)/(R_1 + R_2)} \qquad (2.15)$$

so that an input step ΔE_o in E_o corresponds to an input step

$$\Delta E_1 = \frac{\Delta E_o}{(R_2R_o)/(R_2 + R_o) \;/\; [R_1 + (R_2R_o) \;/\; (R_2 + R_o)]}$$

in E_1 if E is maintained constant. Accordingly calling G^1 the gain in figure 2.15a this is related to the gain G of equation 2.10 and of figures 2.14 by the equality

$$\frac{G^1}{G} = \frac{\Delta E_o}{\Delta E_1} = \frac{R_2R_o \;/\; (R_2 + R_o)}{R_1 + (R_2R_o) \;/\; (R_2 + R_o)}$$

or

$$G = \frac{R_1}{R} G^1 \qquad (2.16)$$

where R is given by equation 2.16a. Also from equation 2.15 if $E_1 = 0$

$$E = \frac{R_o}{R} E_o \qquad (2.17)$$

and from equation 2.11a

$$E_o = (R + R_s)I_N + V_N \qquad (2.18)$$

Example:

Suppose it is necessary to design the circuit of figure 2.15a to have a gain (G^1) of 3 at 95% bias and have a minimum zero to 90% rise time for this gain when using a 20 mA tunnel diode* with a load (R_2) of 50 ohms and a D. C. supply voltage E of 5 volts. A easy approach is to start by assuming E_0 and from figure 14b if E_0 = 500 mV τ should be close to its minimum for all possible values of G. Using this value of E_0 equation 2.17 gives

$$\frac{R}{R_0} = \frac{500}{5000} = \frac{1}{10}.$$

and equation 2.18 then becomes

$$500 = (R + R_s)I_N + V_N$$

$$= (R + 1)19 + 48.7$$

Accordingly

$$R = 22.8 \text{ ohms}$$

and

$$R_0 = 228 \text{ ohms}$$

Then from equation 2.16a R_1 = 41.7 and from equation 2.16 G = 5.5.

Therefore the assumption that E_0 = 500 mV is good (see figure 2.14b) and τ = 1.375 mμ s/pF/mA. If the tunnel diode has a capacity of 10 pF then the minimum zero to 90% rise time for a gain of 3 is $\tau\ C/I_p = 1.375 \frac{10}{20} \doteq 0.7$ mμ secs.

From equation 2.16a $R_1 > R$ and then from equation 2.16 $G > G^1$. Clearly from these equations for a given value of G^1 it is necessary to make R_0 as large as possible to minimize G and accordingly τ for a given load resistor R_2 i. e. the d. c. supply should be a current source. Equations 2.15 through 2.18 are transcendental since the optimum value of E_0 is a function of G but

* Tunnel diode of figure 2.6

on the other hand this optimum value is only weakly dependent on G so that not many trials have to be made (in the previous example the first trial was successful) if a reasonable value of E_0 is first selected.

This method of analysis will be later employed in connection with multiple inputs, fan out ratios and diode tolerances. However the effects of series inductance will be now investigated.

2. Parasitic Series Inductance.

Equations 2.1 and 2.2 when combined give

$$\frac{dV}{dI} = \frac{I - I_d}{C} \cdot \frac{(L_m + L_s)}{V_I - V}$$

i.e.

$$\frac{dV}{dI} = \frac{LI_p}{C} \left[I/I_p - f(V) \right] / \left[E_0 - RI - V \right] \qquad (2.19)$$

where

$$L = L_m + L_s.$$

Since I/I_p and RI are independent of I_p the effect of series inductance on the dynamic trajectory and accordingly on the zero to 90% rise time parameter τ is from 2.19 dependent on the product LI_p/C and on E_0. Figure 2.16 shows the dependence of τ on the gain G for fixed values of the percentage bias (95%) and E_0 (500 mv) and for various values of the parameter LI_p/C where L is measured in $m\mu H$, I_p in mA and C in pF. On the other hand figure 2.17 shows the dependence of τ on E_0 for a fixed gain (4) the same % bias (95%) for the same values of the parameter LI_p/C. These results were obtained using the circuit analyser and the same approximation to the tunnel diode characteristic as in part (1) of this section.

The results clearly indicate that the zero value of LI_p/C does not always give the fastest zero to 90% rise across the diode capacitator. However as figure 2.8 shows the effect of inductance is to produce overshoot and a large increase in recovery time so that

the maximum repetition rate will invariably be obtained with zero or extremely low values of LI_p/C when some type of a reset pulse is employed.

Consequently the d. c. power line and especially the input resistor should be as noninductive as possible. The output resistor should be also of low inductance to supply a sharp input pulse to the next stage. This naturally leads to the idea of input and output transmission lines (figure 2.18 with r = 0). A transmission line input has the added advantage that the gain G^1 is halved with a consequent decrease in τ and the characteristic impedance is almost entirely resistive. However, due to reflection problems it may be necessary to insert a resistance in series with the input line as in figure 2.18 and then while the gain G^1 is still halved the input impedance is now the sum of the characteristic impedance of the line and this resistor.

3. The Impedance Level.

Since the parameter τ is independent of the impedance level the rise time can be minimized by selecting the tunnel diode with the maximum value of I_p/C providing the value of LI_p/C is not too large. Of the tunnel diodes presently available the quantity I_p/C increases with I_p and since their series inductance (L_s) is low (about 0.4 mμH) and could be further decreased by direct deposition, faster switching occurs with higher value of I_p. The only limit is that imposed by power considerations the latter being proportional to I_p.

4. A. C. Bias.

Using A. C. superimposed on the D. C. bias the switches can be synchronized and the A. C. can also act as the reset pulse in a return to zero circuit. The single diode circuit will be considered as operating in this way. If the driving voltage E_0 is replaced by E where

$$E = (E_0 - e_1) + e_1 \sin\omega t$$

then the maximum value of E would give about the same % bias as the D. C. voltage E_0.

The load line would than vary with time between the limits shown on figure 2.19. Due to time variation of the input and E switching will occur under the influence of a varying load line. The parameter τ in addition to its dependence on the % bias, the Gain and E_0 is now also dependent on ω and the amplitude of the A. C. clock. If ω is sufficiently low the switch will be completed with a virtually static load line. As ω or the A. C. amplitude increases the load line will drop more and more during the rise time of the diode which leads to incomplete switching and eventually to complete suppression of the output. The analytical solution of this problem now becomes extremely difficult so that it is necessary to resort to a qualitative discussion and experimental justification.* Basically the A. C. amplitude must be kept as low as possible to minimize its effect on the rise time but at the same time sufficiently large to guarantee the reset. An inspection of figures 2.6 and 2.14 indicates that the maximum value of the bias should be about 500 mv and an A. C. peak to peak amplitude of 300 mv should be sufficient to guarantee reset. Denoting the clock period by T, the origin of time when the clock reaches its peak, and using an input that is some fraction of the output then except for marginal cases which must at all times be avoided switching will be initiated at a slightly negative time if the input reaches its maximum value at t = 0. Since switching should be completed before the A. C. component of the bias goes through zero the zero to 90% rise time cannot be greater than T/4. With these restrictions the rise time should be fairly close to that predicted by the parameter τ and the

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* This problem is further discussed in Chapter 3 in the section titled "A. C. Bias Amplitude."

maximum operating frequency would approximately be

$$f_{max} = \frac{1}{4\tau\, C/I_p} \qquad (2.20)$$

An experiment shown schematically on figure 2.20 was set up to justify these statements. A 20 mA tunnel diode (10pf) which was essentially operating into a 25 ohm load was used. The peak A. C. bias was 150 mv and the D. C. was about 350 mv the latter being adjusted to give 95% bias. The trigger was also supplied by the A. C. generator the amplitude of the trigger being the excess over that necessary to give bias amplitude. The gain was computed from the ratio of the output amplitude to the trigger amplitude and the measured marginal gain at 300 megacyles was about 7.5 which is in reasonable agreement with the theoretical figure of 8 on figure 2.14b. Some oscillographs of the results obtained are shown in figure 2.20b. In these oscillographs the lower trace is a marker indicating the clock and input phase. The experimental values of τ are compared with their theoretical counterparts in Table 2.1 and good agreement is evident.

TABLE 2.1

300 Megacycle Clock

Input Amplitude	Output Amplitude	Gain	τ Experimental	τ (Theoretical)
55	380	7	1.8	1.9
76	400	5.25	1.4	1.3
100	420	4.2	1.2	1.1
125	430	3.4	1.0	0.9

Hence, even though the τ parameter is slightly artificial when A. C. bias is employed it can be used as a useful guide to design and equation 2.20 will supply a good approximation to the maximum operating frequency.

(C) Multiple Inputs and Diode Tolerance, OR, AND and Compliment Circuits

Here the effect of parasitic inductance and capacity will be again neglected except for a few qualitative comments. Defining the parallel impedance of all the output impedances as equal to R_2 then for $R_0 >> R$ the parallel impedance of all the inputs is R_1 where

$$R_1 = \frac{RR_2}{R_2 - R} \qquad (2.21)$$

and from equation 2.18

$$R = (E_0 - V_N) / I_N - R_s \qquad (2.21a)$$

Suppose the input and output circuits are transmission lines and for the time being let us eliminate reflection problems by using sufficiently long lines. Then if the parallel impedance of the input lines in the high voltage state is R_3 ($R_3 > R_1$) and G^1 is defined by the equation

G^1 = output line voltage/input line voltage

corresponding to equation 2.16 we now have

$$G = \frac{R_3}{2R} G^1 \qquad (2.22)$$

where the 2 in the denominator results from the fact that the equivalent input circuit for the transmission line is a voltage source of twice the transmission line voltage with an output impedance equal to the characteristic impedance of the line as is illustrated in figure 2.18. The input line voltage will in general be some fraction of the output voltage of a similar circuit and so G^1 will be known. Then depending on the value of R_3/R the gain G will be > Gmax in which case the diode

will not switch or $<$ Gmax in which case it will switch if the correct value of E_0 is used. The value of Gmax maximized with respect to E_0 is the $\tau = \infty$ curve on figure 2.21. Due to diode tolerance this Gmax varies between some limits for any % bias. In tunnel diode circuits where the diodes are biased near the peak current the most important diode tolerance is the percentage variation of this peak current and to a high degree of accuracy this % tolerance is equivalent to a similar variation in the % bias. This will result in upper and lower limits in the above value of Gmax which we shall call G_H and G_L ($G_H > G_L$). Then for values of $G > G_H$ the diode will not switch, for $G < G_L$ the diode will switch and if $G_L < G < G_H$ the outcome is indeterminate.

Example: Suppose the nominal bias is 95% and the peak current variation is guaranteed between $\pm$ 1%. Then from figure 2.21

$$G_H = 10.6 \text{ and } G_L = 7.7$$

In general G_H and G_L depend on the percentage bias and diode tolerance and we must be careful to select R_3 so that G does not ever fall in the indeterminate region ($G_L < G < G_H$) to insure logical operation of circuit. Keeping this in mind together with the fact that as low a value of the parameter τ as possible is desired some logical circuits will now be considered.

1) The Logical OR Circuit.

Consider a logical OR circuit with n inputs and m outputs all of the same characteristic impedance. When i of the inputs are high equation 2.22 becomes

$$G_i = \frac{m+n}{2i} G^1 \qquad (2.23)$$

Since the maximum value of G_i occurs for i = 1 the only requirements are that

$$G_1 = \frac{m+n}{2} G^1 < G_L \qquad (2.24)$$

and that the bias % plus the % tolerance of the peak current will be less than 100. In practise a certain allowance should be made for circuit noise, drift in the power supplies, etc., the net effect being to lower G_L.

All the tolerances including that of the diode peak current tolerance will result in a fixed tolerance in the % bias. Let this tolerance be $\pm \delta\%$. A practical method of approach consists of putting an upper limit in the permissible value of τ and then making an allowance for δ. If this upper limit of τ is τmax then equation (2.24) becomes

$$G_1 = \frac{m+n}{2} G^1 < \bar{G} \qquad (2.24a)$$

where $\bar{G}$ is the gain at $\tau = \tau_{max}$. For any value of τ_{max} the value of $\bar{G}$ can be plotted against the % bias by means of a crossplot from figure 2.14. If on this crossplot $\bar{G} = X$ when the % bias is Y then to guarantee $G < \bar{G}$ the percentage bias must be equal to $Y + \delta$. In addition $Y + 2\delta$ must be less than 100%.

The maximum operating frequency fmax as given by equation 2.20 now becomes

$$f_{max} = \frac{1}{4 \tau_{max} c/I_p} \qquad (2.20a)$$

so that higher values of τ_{max} lead to lower values of f_{max}. On the other hand higher values of τ_{max} will lead to higher values of the gain and by equation 2.24a to higher values of m and n. An inspection of figures 2.14 shows that very little additional gain can be achieved for values of $\tau > 2$. Consequently this value of τ will give the approximate upper limit of the sum of the fan in and fan out integers m + n.

On figure 2.21 the curve marked $\tau = 2$ is the plot of $\bar{G}$ against the % bias for $\tau_{max} = 2$. Using this plot and proceeding as outlined above Table 2.2 was constructed. It shows the maximum

permissible values of the % bias and the corresponding minimum values of the gain G for various values of the percentage bias tolerance δ.

TABLE 2.2

δ	Maximum % Bias	Minimum G for $\tau < 2$
1	99	12.2
2	98	8.2
3	97	6.2
4	96	5.2
5	95	4

With the tunnel diodes presently available the minimum practical value of δ is about 1.5. Hence a value of G of about 10 is attainable. In part 3 it will be shown that the minimum value of G^1 is 2 so from equation 2.24 the maximum value of sum of the fan in and fan out integers is about 10. It will be also shown that due to power supply consideration this number must be slightly reduced so that the upper limit of m + n is 8 or 9.

From the above considerations the simple tunnel diode circuit will operate effectively as an OR gate and the sum of the fan in and fan out integers can at least be as high as 8. This brings the OR gate well within the range of practical application.

2) The Logical AND Gate.

Equation 2.23 is also applicable to the AND gate where i is the number of high inputs. Since the circuit must switch for i = n and must not switch for i = n-1 equation 2.23 gives

$$G_n = \frac{m+n}{2n} G^1 < G_L$$

and (2.25)

$$G_{n-1} = \frac{m+n}{2(n-1)} G^1 > G_H$$

one consequence of the relations 2.25 is that

$$\frac{n}{n-1} > \frac{G_H}{G_L} \qquad (2.26)$$

From equation 2.26 it is easily seen by inspecting figure 2.21 that, for a given % tolerance in the peak current, as n increases the nominal % bias must decrease.

Example: For a peak current tolerance of $\pm$ 1 1/2% we obtain Table 2.3 where some of the values of τ nominal and τ max

TABLE 2.3

% Bias	G_L	G_H	n_{max}	n	G^1	$\tau_{nominal}$	τ_{max}
97.5	10.5	25	1	-	-	-	-
95	6.2	11.9	2	2	6.0	1.5	2.4
92.5	5.5	7.7	3	3	5.2	1.8	2.2
92.5	5.5	7.7	3	2	3.9	1.15	1.25

were obtained by interpolation from figures 2.14. Even at 95% bias the maximum permissible value of n is only two and the spread in the value of τ due to diode tolerance is about 100% of the nominal value. Also a value of G^1 of 6 is so high that the noise level would have to be very low. On the other hand at 92.5% bias and n = 2 a lower value of τ is possible with much less % variation but G^1 is probably still a little too high. The solution then is to retreat to lower values of the % bias and this is justified diagrammatically for n = 2 in figure 2.22.

There are however, many objections to this approach:

a) The inductive effect may lead to false switching as is illustrated if figure 2.23 for n = 3 where for 2 inputs high the inductance causes the dynamic trajectory to deviate sufficiently from the load line to cause the circuit to switch if the diode peak current was less than its nominal value.

b) If we use a A. C. bias superimposed on D. C. where the A. C. acts as a synchronizing and reset clock then the load line and the input pulse will be time variant. Presumably the clock and input should reach their peak values at about the same time to initiate switching and then the load line will fall off as the input and A. C. bias decrease. The lower the % bias the more dependent the load line becomes on the input signal and the greater the tendency towards incomplete switching.

Accordingly tunnel diode circuits reducible by the Thevinin theorem to that of figure2.4are not directly suitable as AND gates. However since OR circuits operate best at high % bias and the problem of false switching due to inductive overshoot in the neighbourhood of Vp does not apply the same circuit is suitable as an OR gate.

3) The Modified AND Circuit.

Consider the circuit shown in figure 2.24a with the negative bias E (figure 2.24b) where the circuit switches when /E/ is a maximum unless a positive pulse is applied at the input. This circuit operation is similar to that of the positively biased circuit except that the percentage bias will be (100 + δ) instead of (100 - δ)% and the presence of a positive pulse at the input hinders switching instead of causing it. The output will then be the mirror image of the compliment of the input. For simplicity we shall designate the symbol $\underline{\overline{A}}$ to the mirror image of the compliment of A.

Suppose now it is desired to construct an AND gate for the signals A, B, C, D, ---. The procedure is to generate the mirror image of the compliments of all but one of these inputs - say $\overline{B}$, $\overline{C}$, $\overline{D}$, ---, and then apply the latters and A to an OR gate. Since the absence of one or more of the signals B, C, D, ---, will lead to a negative input to cancel the effect of A if the latter is high it is easily seen that the circuit now operates electrically like an OR circuit and is accordingly not subject to the disadvantages of the direct AND gate.

4) The Complement Circuit.

The Complement of the signal can be obtained by applying its mirror image about the low d. c. bias point to an over biased OR circuit. This is illustrated diagrammatically in figure 2. 25. At the frequency of interest (about 300 to 500 M'c's) it is doubtful that conventional inductive coupling could be employed in the -1 box. An inverting circuit which can be integrated with microstrip delay lines and whose response is fairly close to $-\alpha(\alpha < 1)$ is shown in figure 2. 26. The conductor is insulated from the ground plane except at points A, B and C where it is connected to it. Clearly the microstrip transmission lines are coupled to give inversion but each one is terminated in a short circuit except for the inductance introduced by the holes. A very approximate equivalent circuit is shown in figure 2. 27 the capacity being mostly that across the slit of width b and breadth t as shown in figure 2. 26. While it should be possible to adjust the parameters r_1, r_2, t and b (see figure 2. 26) to make the d. c. short resonant at high frequencies the analytical determination of the values of these parameters as a function of the frequency is a very difficult if not impossible problem.

To ascertain the applicability of this inverting device to the output pulses of a logic gate it was accordingly decided to experimentally determine its response to a spike shaped pulse. The experiment was set up with t = 0. 2", b = 0. 2" and some selected values of r_1 and r_2. The source spike had a base width of

approximately 1.6 mμ secs and the circuit is shown schematically in figure 2.28. The length of the microstrip line was 6-1/2" and its characteristic impedance was 50 ohms.[2] (Using a 10 mill teflon insulating sheet the corresponding conductor width was 32 mills.) Preliminary tests showed that the direct microstrip line and the coaxial to microstrip connectors had a negligible effect on the spike pulse but the 15 mμ sec coaxial delay did alter the amplitude of the spike as shown in figure 2.29a. Then the microstrip line was adapted to become an inverter as shown in figure 2.26 and the results shown in figures 2.29b, 2.29c, 2.29d, and 2.29e were obtained for the different values of r_1 and r_2. The inverter transmission coefficient (T) and the negative reflection coefficient (R) are shown on Table 2.4 for these various values of r_1 and r_2. Clearly it is not difficult to obtain up to 80% transmission which is more than adequate to serve as an input to the overbiased OR gate.

TABLE 2.4

r_1 (inches)	r_2 (inches)	Transmission Coefficient (T)	Reflection Coefficient (R)
0.5	0.5	0.38	0.76
1.0	1.0	0.55	0.55
1.8	1.8	0.725	0.41
2.3	2.3	0.76	0.34
2.3	∞	0.85	0.25
∞	∞	0.87	0.13

The reflected pulse will tend to inhibit the source from switching (assuming this is a tunnel diode) but it is possible to compensate for this effect by inserting an open circuited lossy stub

line there so that the positive reflection from this stub returns at the same time as the negative reflection from the inverter. It is also necessary to include resistance in series with the input and output lines of the inverter to control the circulating current due to the D. C. bias.

Summary: A complete set of logic elements namely the OR, AND and COMPLEMENT circuits were developed. The circuits are very simple and their switching speeds are as fast as can be obtained with the tunnel diode device. Essentially the modification of the AND gate resulted in a circuit configuration most suitable to the tunnel diode device and effectively made the sensitivity of the AND gate equal to that of the OR gate. The method of analysis is independent of the diode capacity and peak current. It can also be applied for any shape of the normalized V-I tunnel diode characteristic. However, the numerical results are only applicable to germanium tunnel diodes.

The circuit design incorporates the null effect to give increased sensitivity and minimize the effects of parasitics. Furthermore, the parasitics themselves can be kept to very low values by means of input, output and power supply transmission lines.

In Part 3 the interaction between logic elements is discussed and a method of connection is developed. A distinction between input and output lines is obtained by means of phase techniques and subject to certain restrictions the elements can be connected to perform any logical operation.

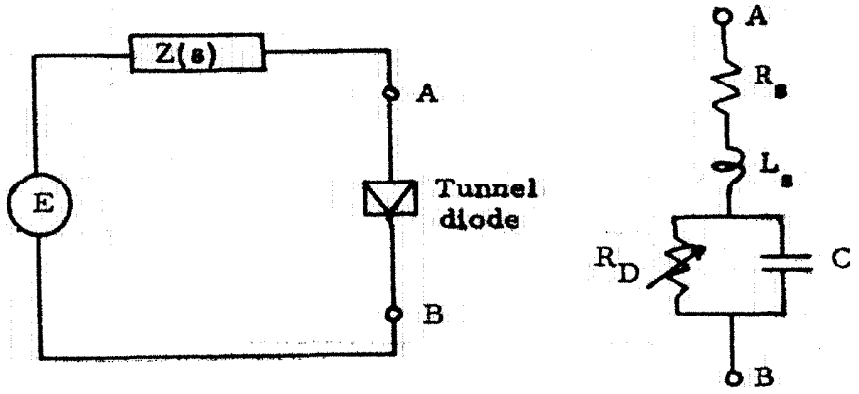


Figure 2.1

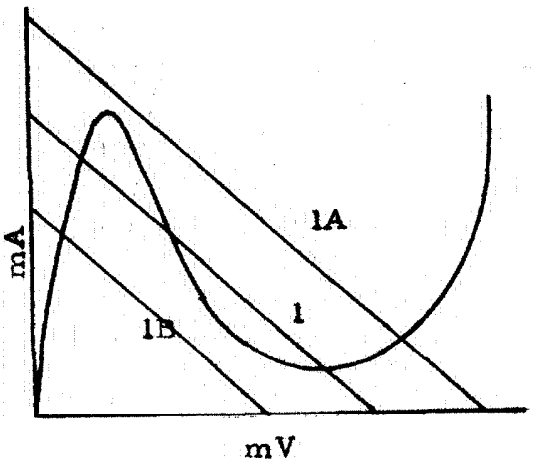


Figure 2.2

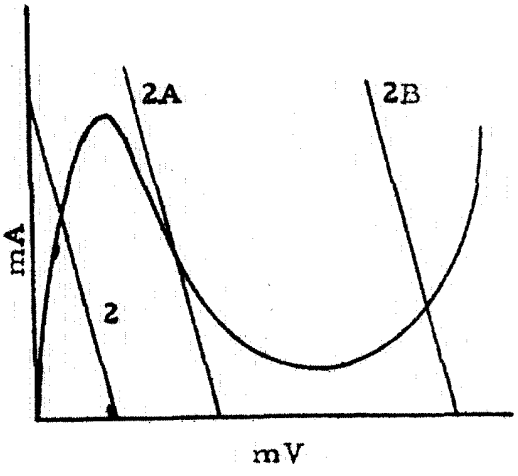


Figure 2.3

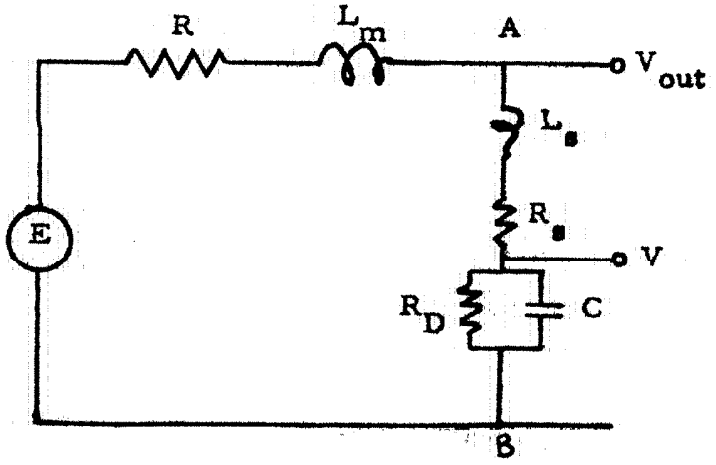


Figure 2.4

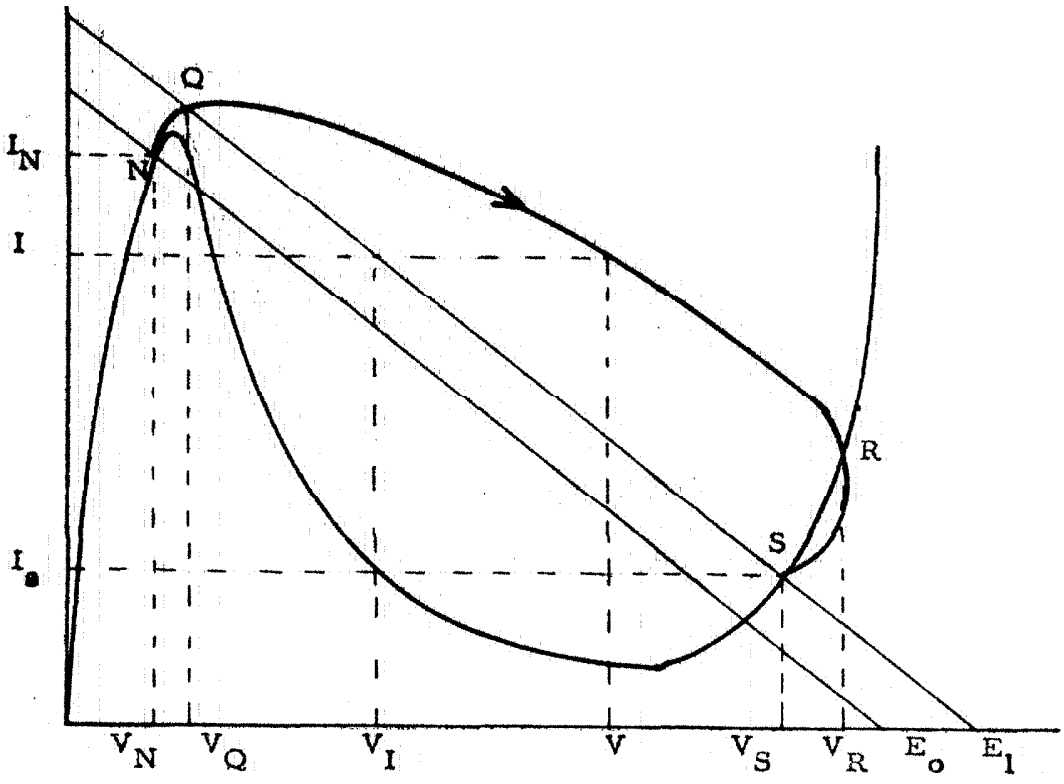


Figure 2.5:- The dynamic trajectory

T. D. 182 Characteristics

L_s = 0.4 nH

R_s = 1 ohm

C = 10pF

R_D ___ Given by curve

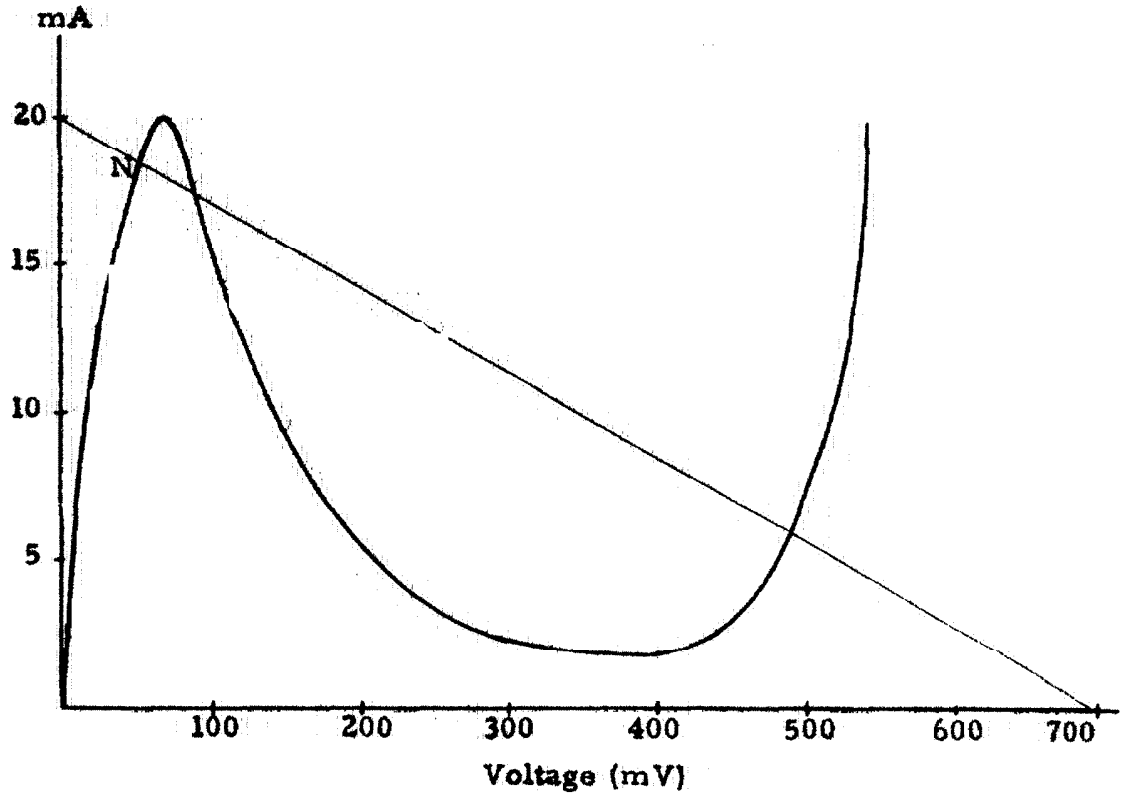


Figure 2. 6;- V-I characteristic of R. C. A. 's T. D. 182

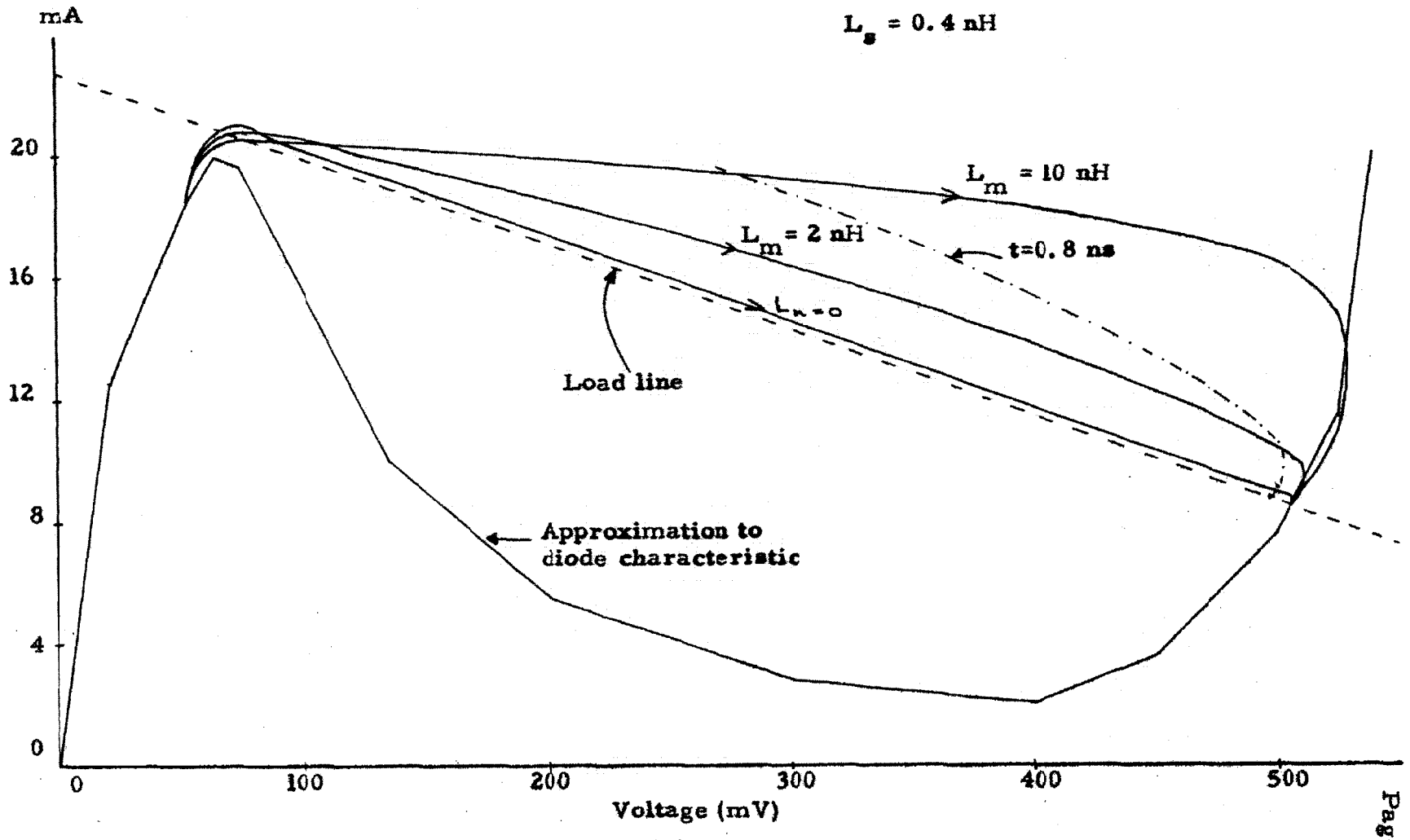


Figure 2.7:- Computed dynamic trajectories

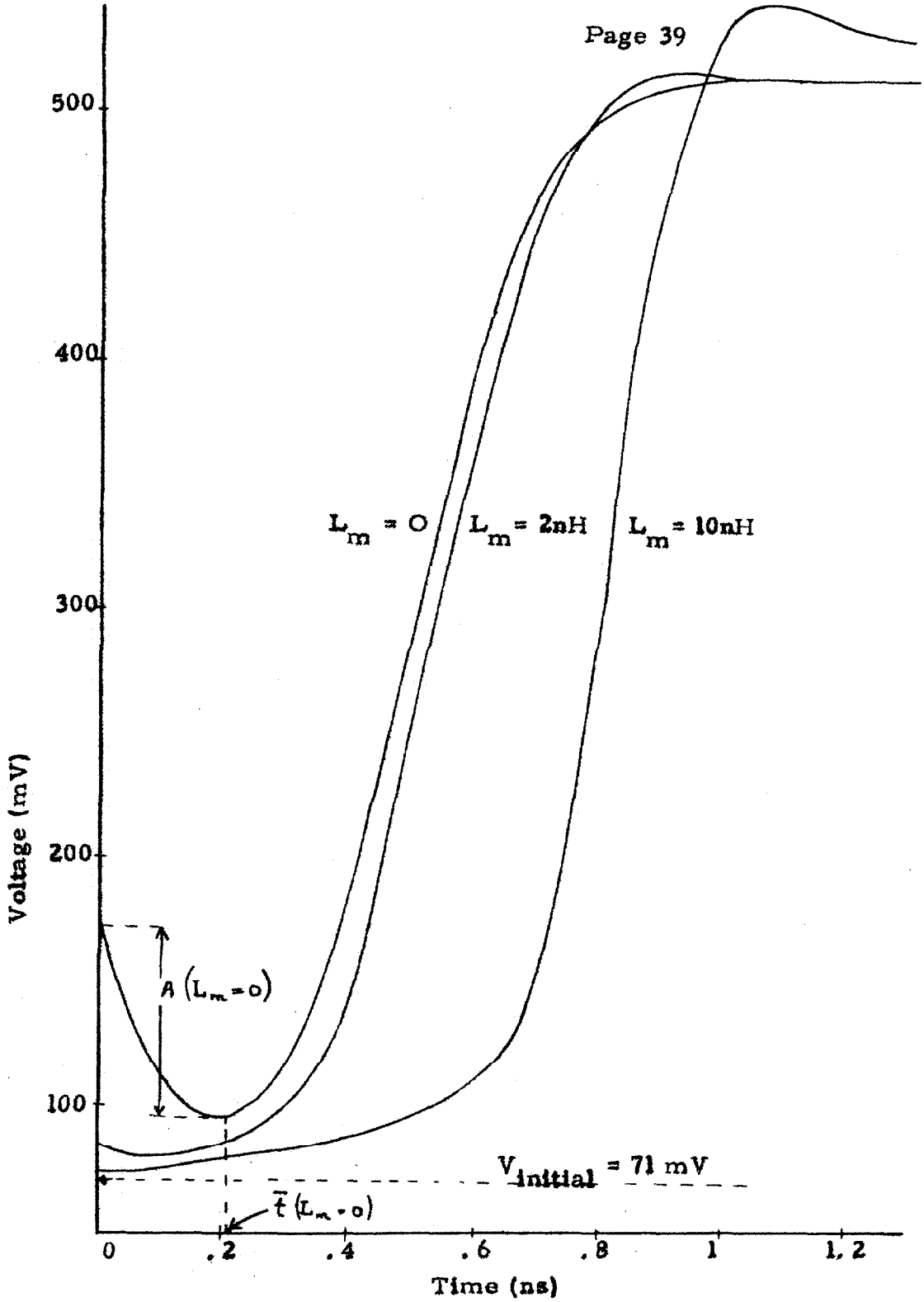


Figure 2.8:- Computed output waveforms

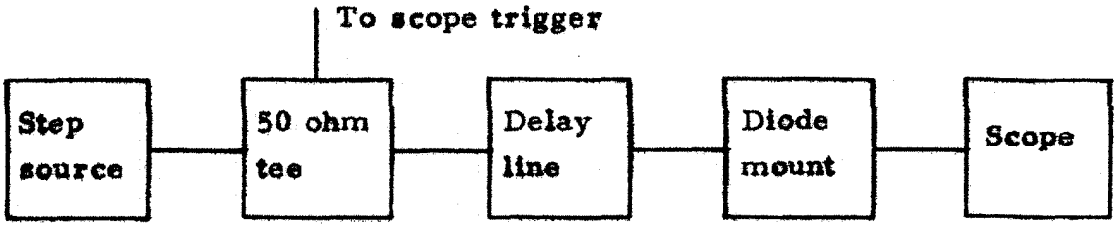


Figure 2.9:- Schematic layout

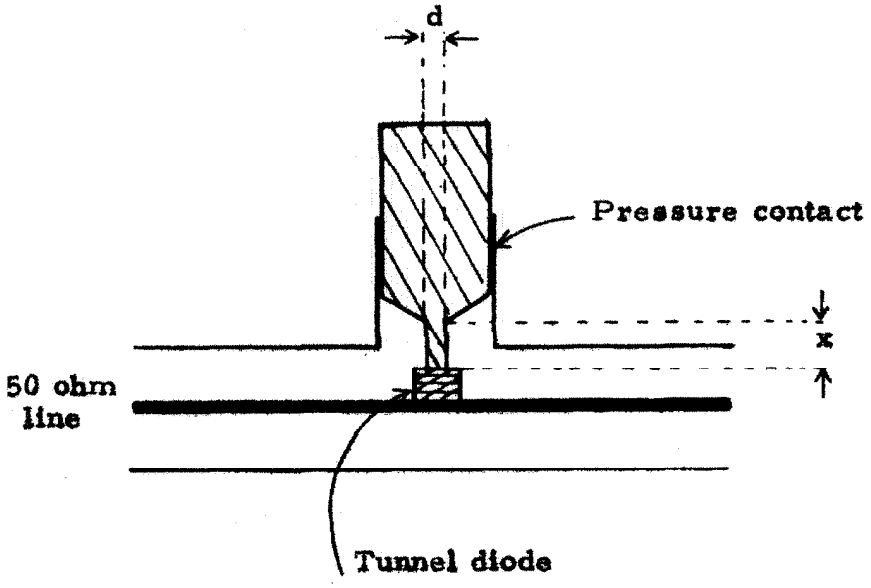
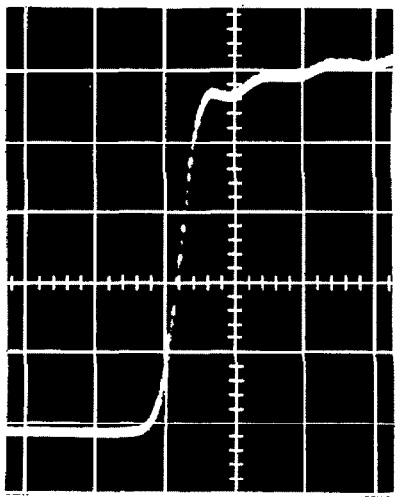
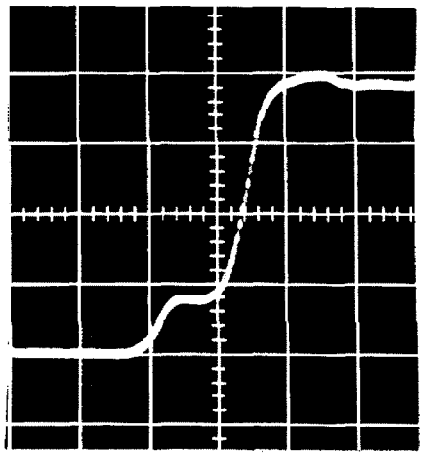


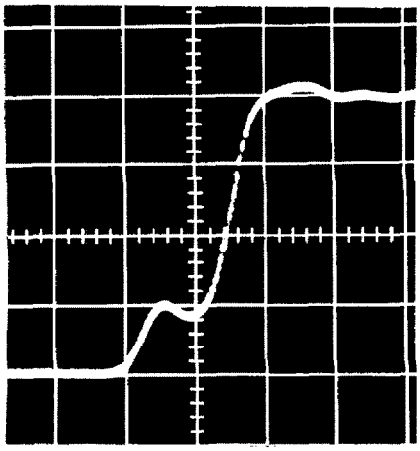
Figure 2.10:- Diode mount of figure 2.9



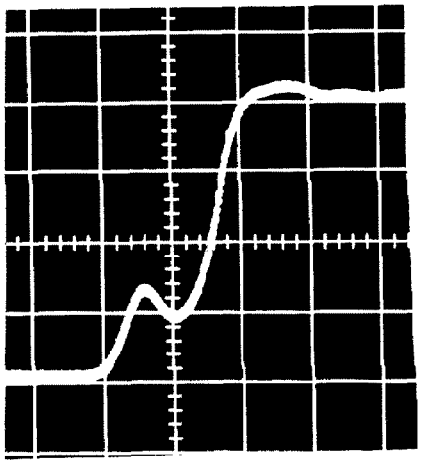
Input



Output $L_s = L_{s1}$



Output $L_s = L_{s2} > L_{s1}$



Output $L_s = L_{s3} > L_{s2} > L_{s1}$

Scales:- Hor. 1ns/cm. Ver. 100mV/cm.

Figure 2.11:- Experimental input and output waveforms of the circuit of Figure 2.9.

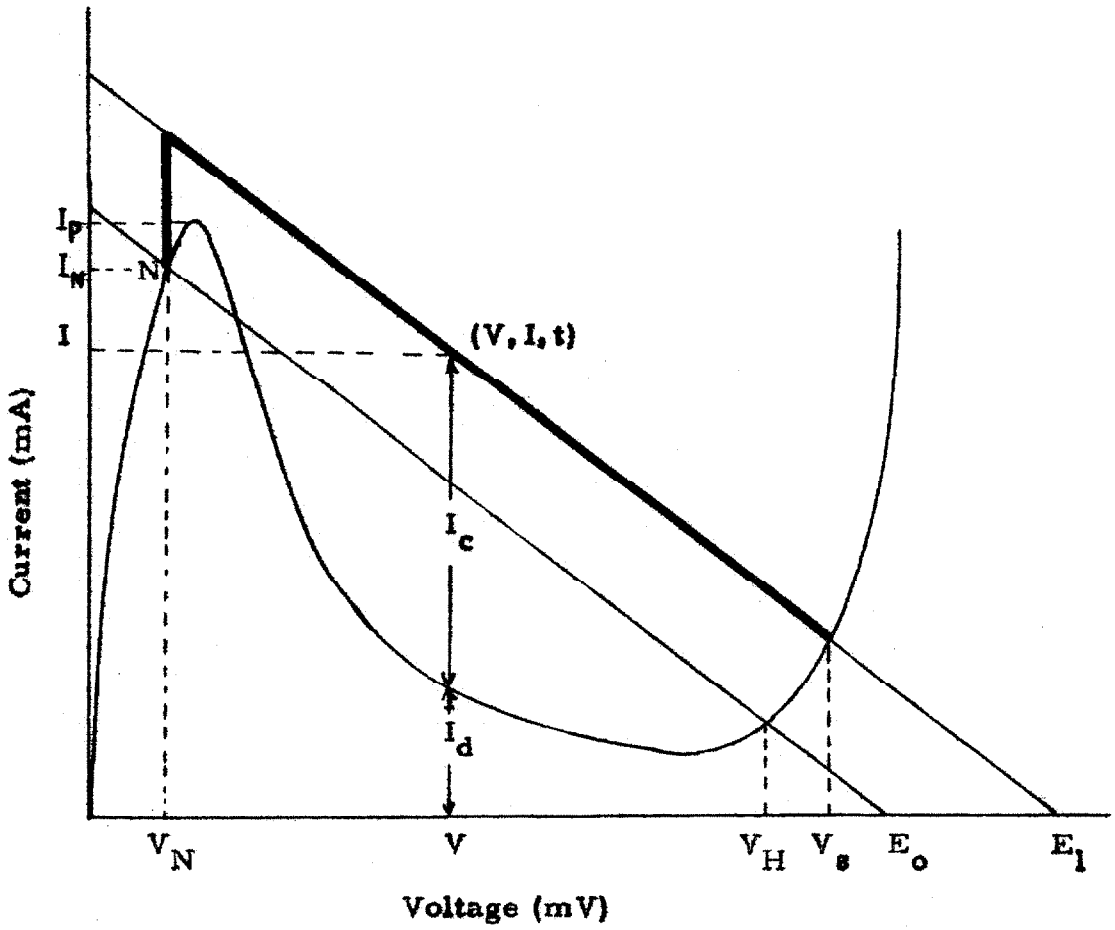
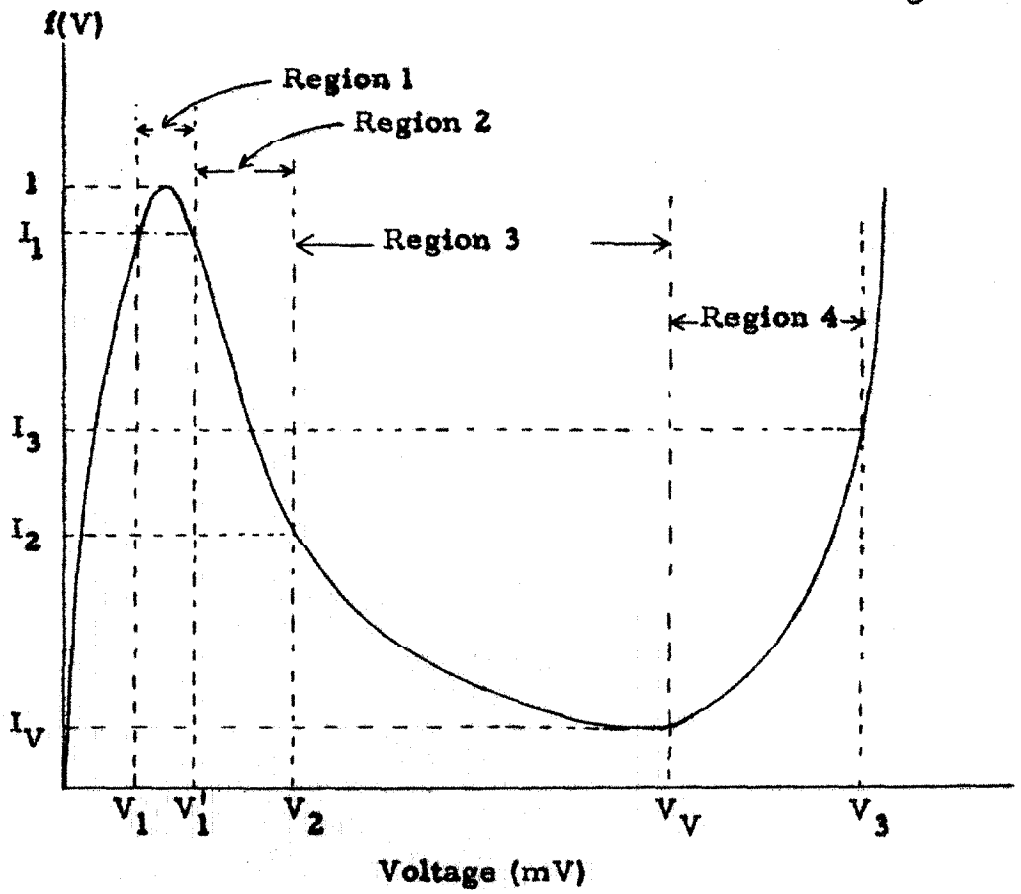


Figure 2.12:- The dynamic trajectory when parasitic inductance is negligible



Typical values for germanium diodes

$V_1 = 45$, $I_1 = 0.925$; $V_p = 65$; $V_1' = 85$;

$V_2 = 150$, $I_2 = 0.425$; $V_V = 400$, $I_V = 0.1$;

$V_3 = 525$, $I_3 = 0.6$.

Figure 2.13:- The approximation to f(V)

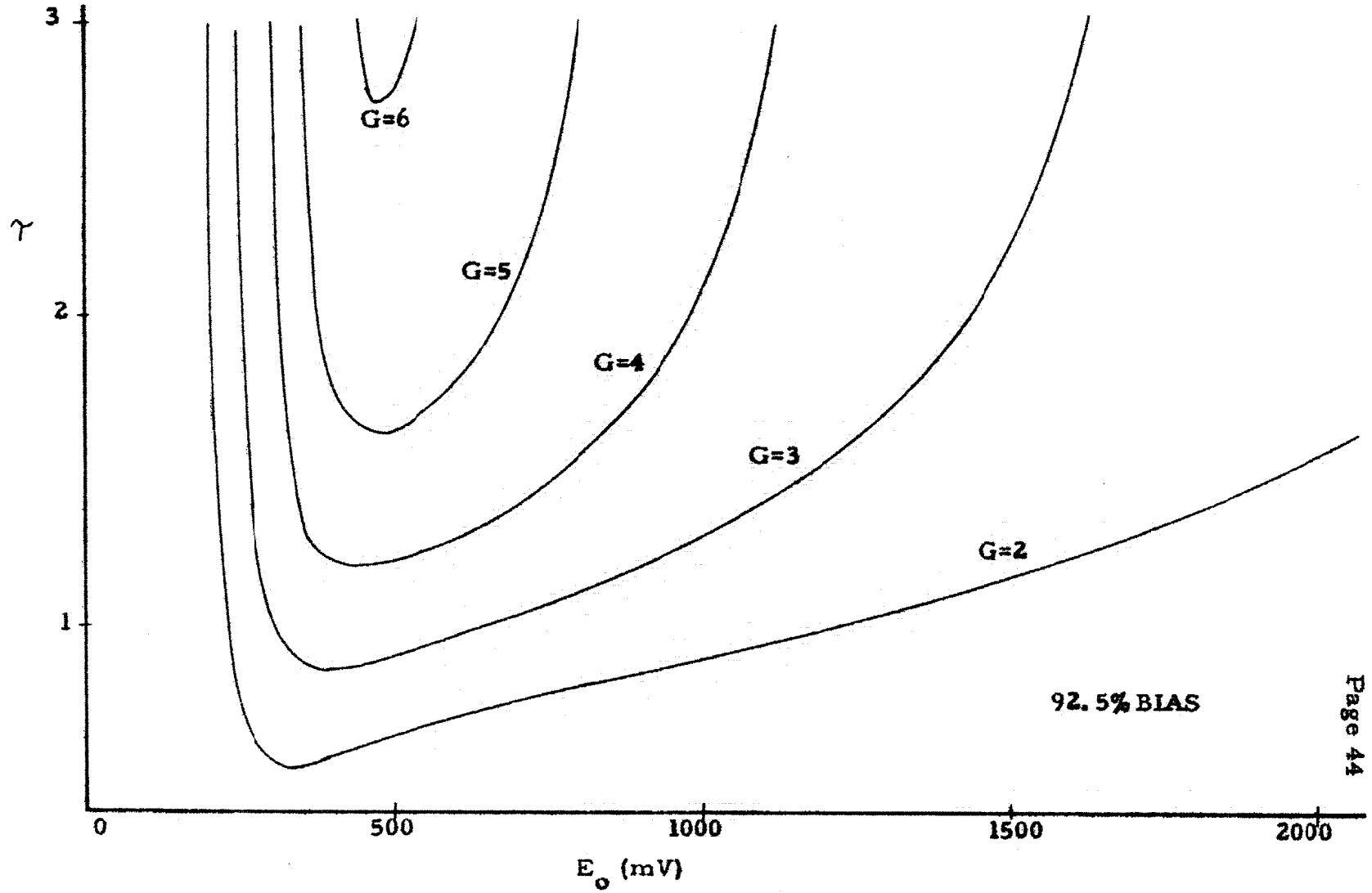


Figure 2.14a:- Dependence of γ on E_o and gain at 92.5% bias

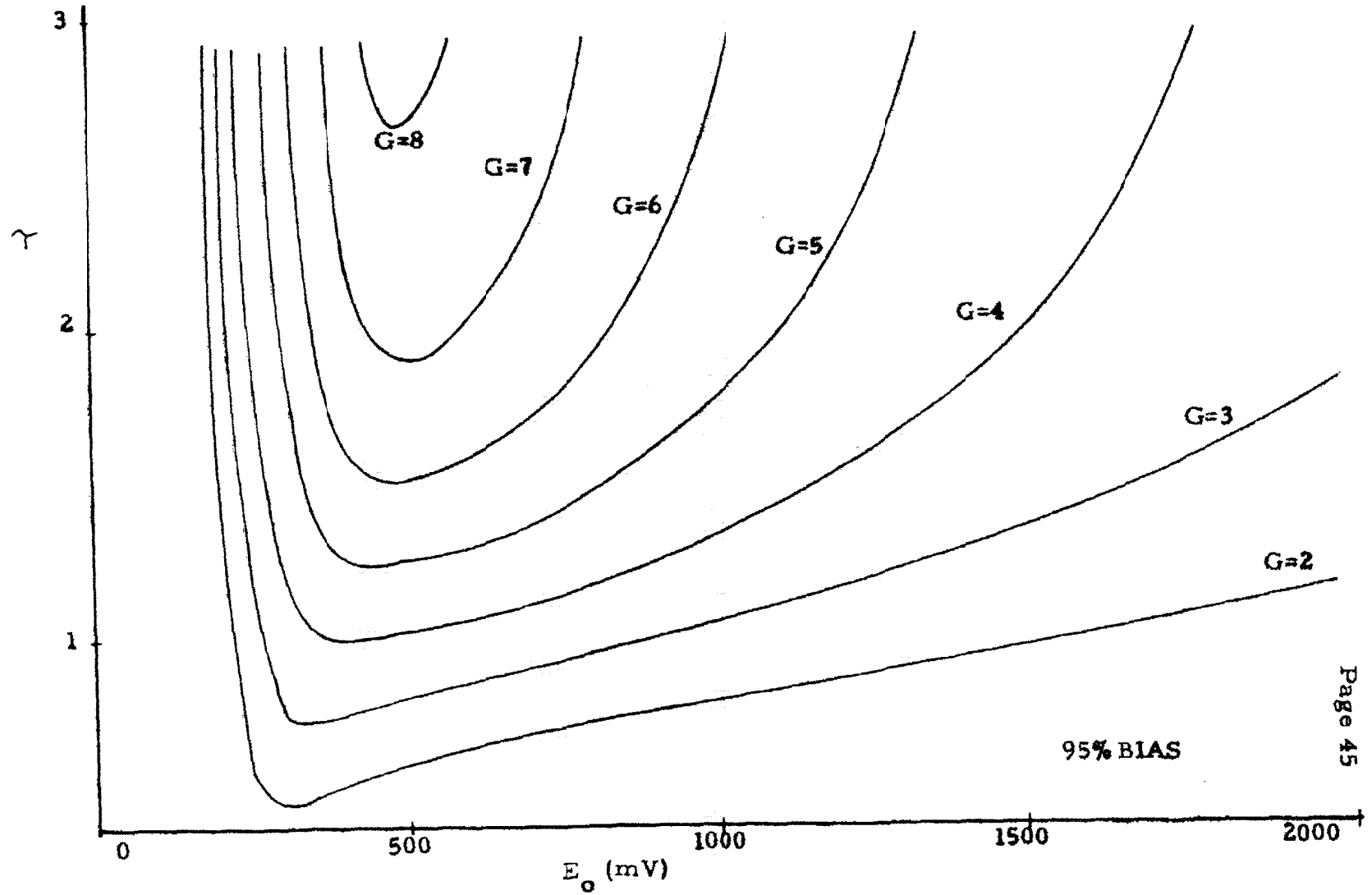


Figure 2.14b:- Dependence of τ on E_o and gain at 95% bias

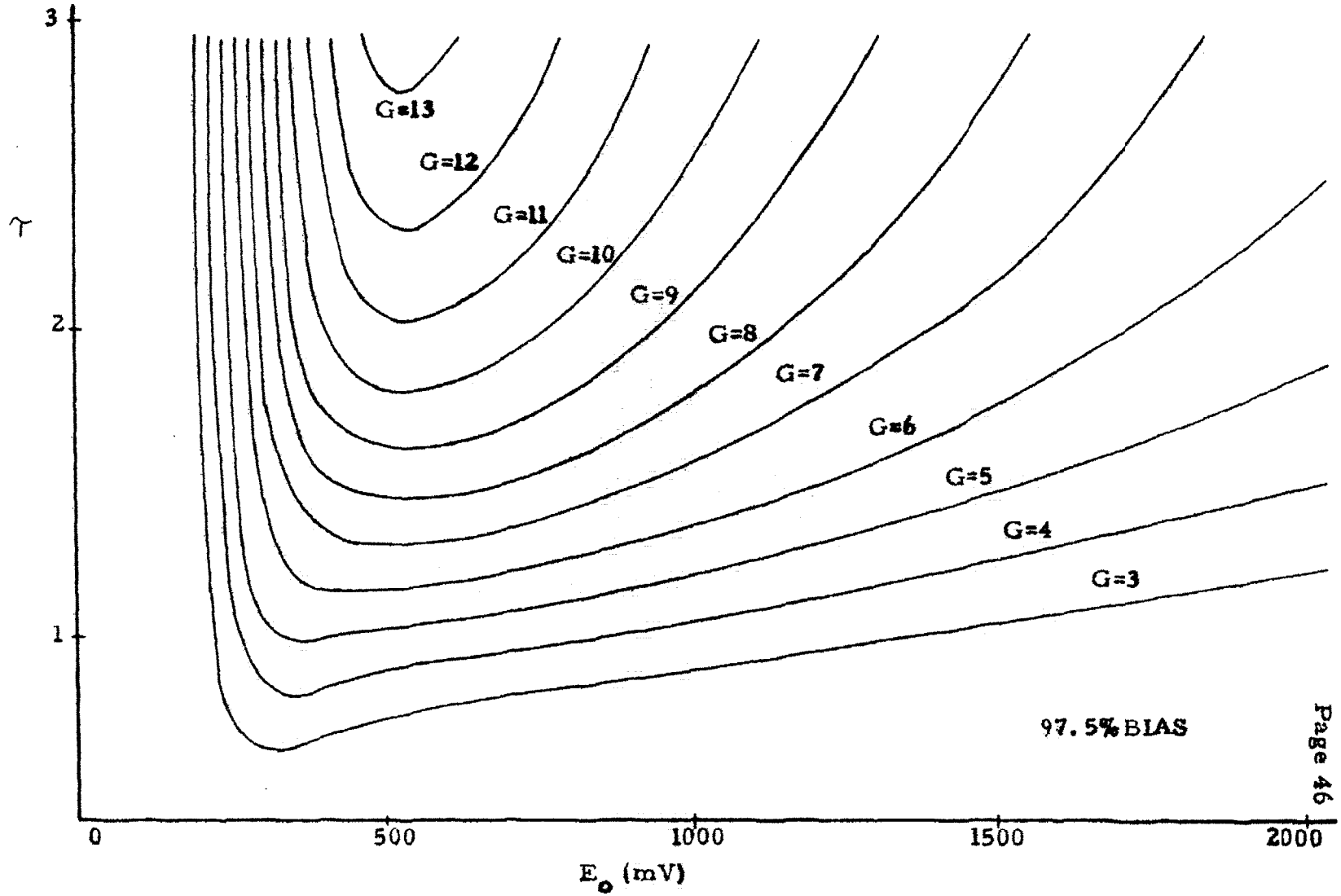
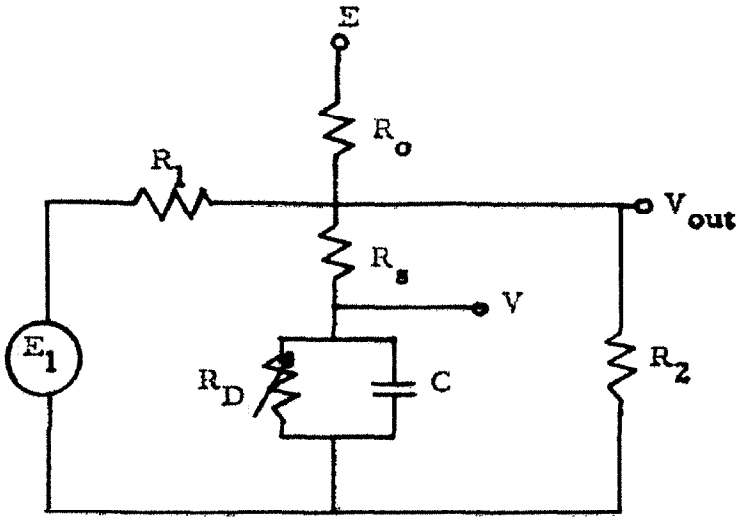
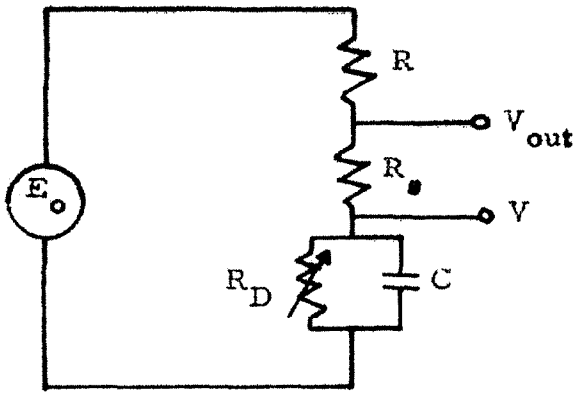


Figure 2.14c:- Dependence of τ on E_o and gain at 97.5% bias



(a)



(b)

Figure 2.15

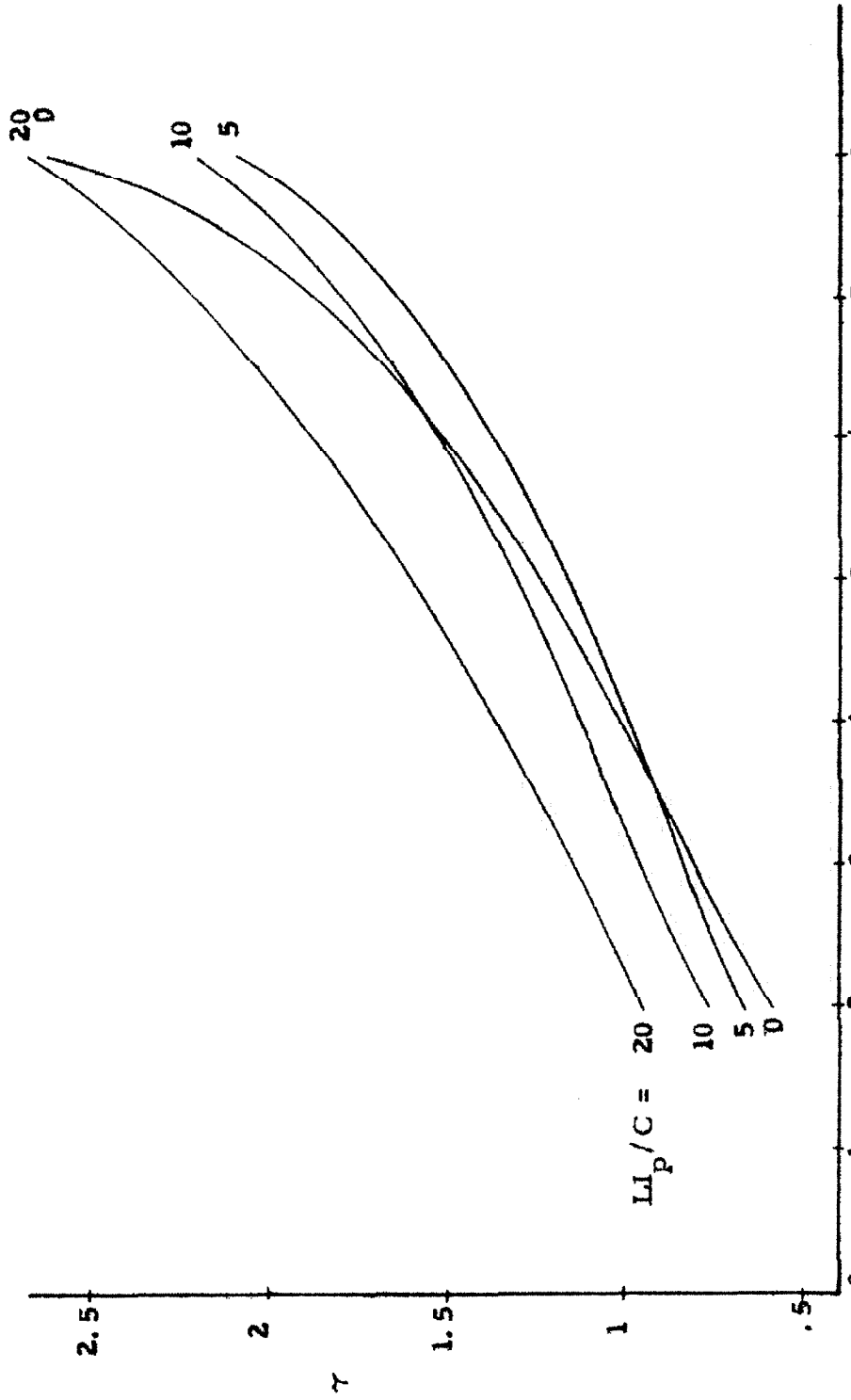


Figure 2.16:- Dependence of γ on LI_p/C for variable gain and fixed E_o (500 mV)

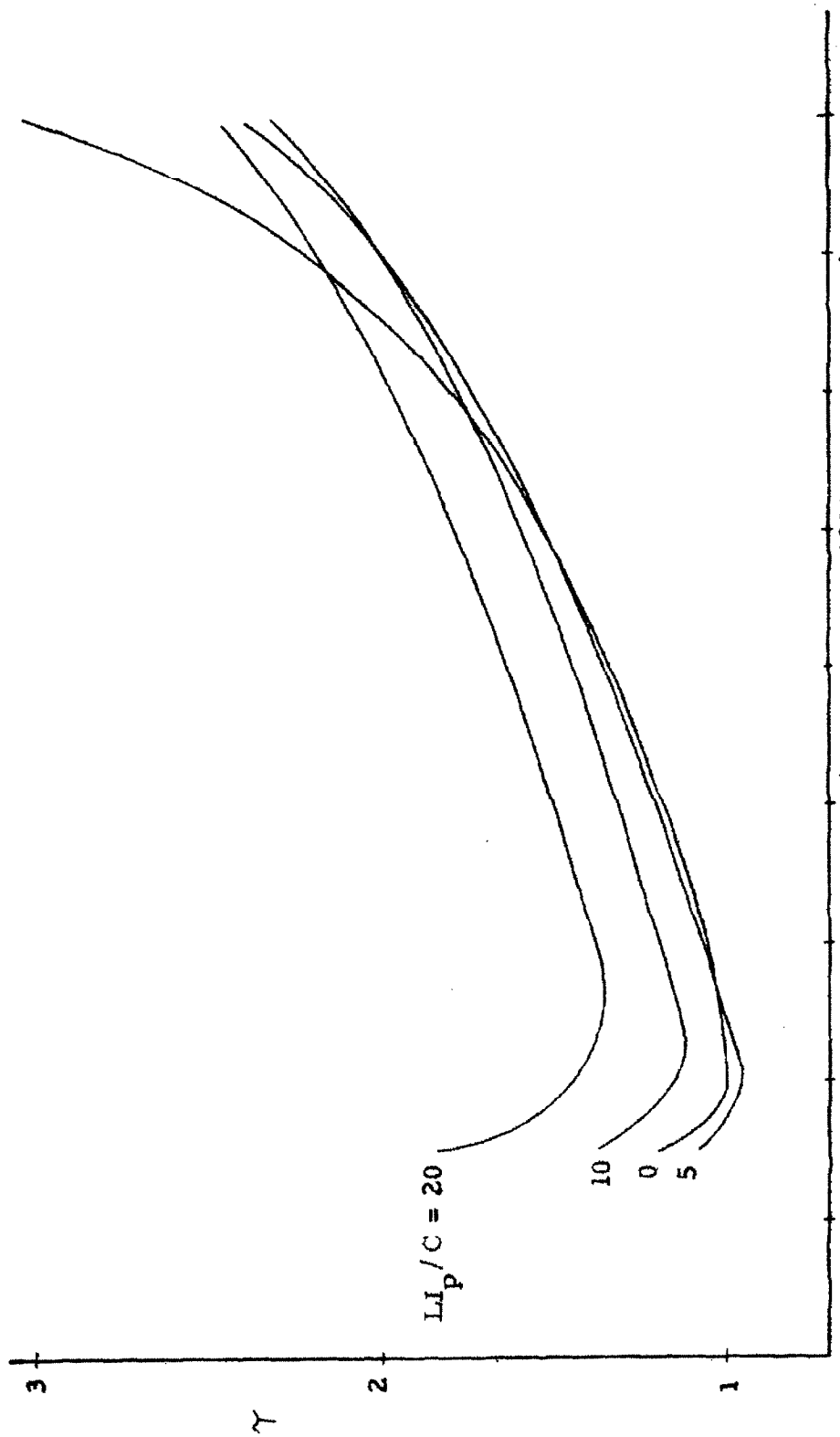


Figure 2.17:- Dependence of γ on LI_p/C for a fixed gain of 4 and variable E_o

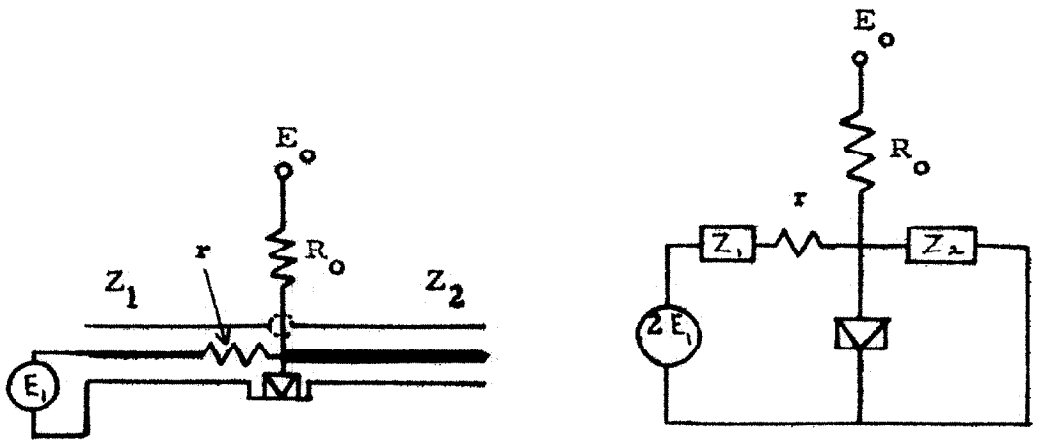


Figure 2.18:- Input and output transmission lines

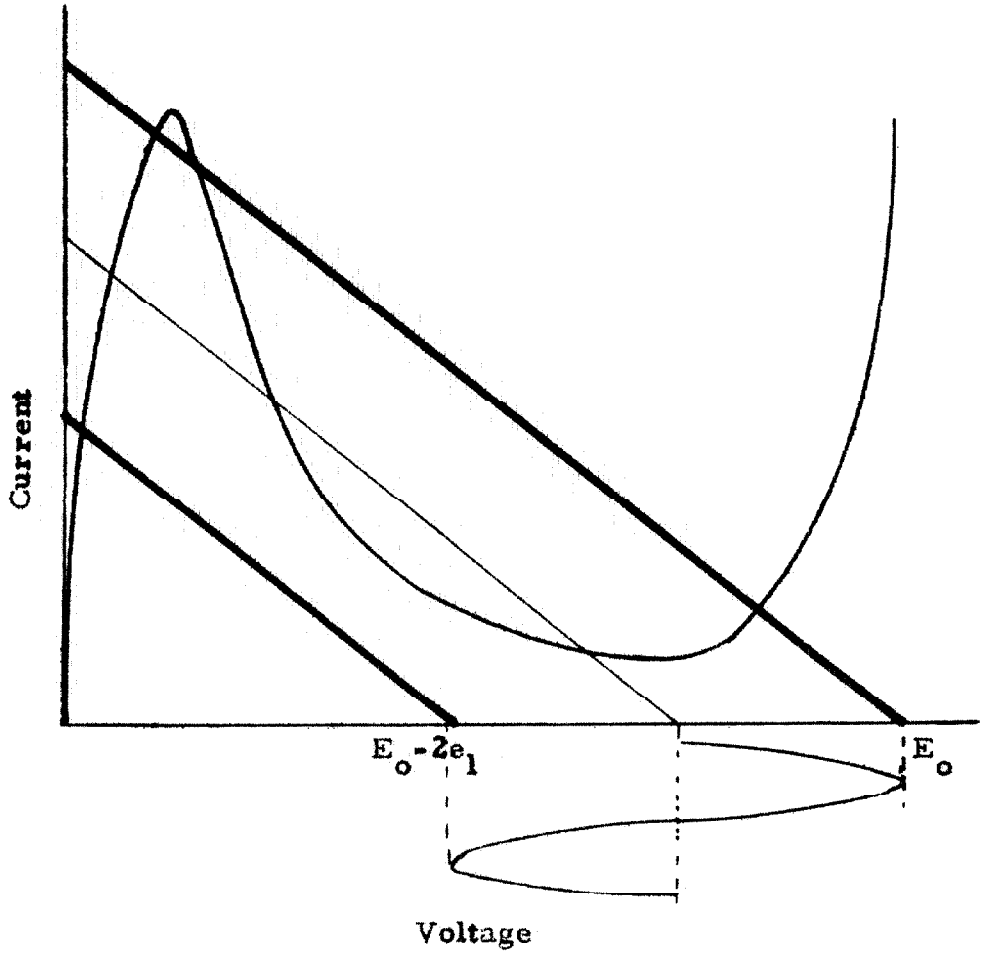


Figure 2.19:- Time dependence of the load line with an A. C. bias component

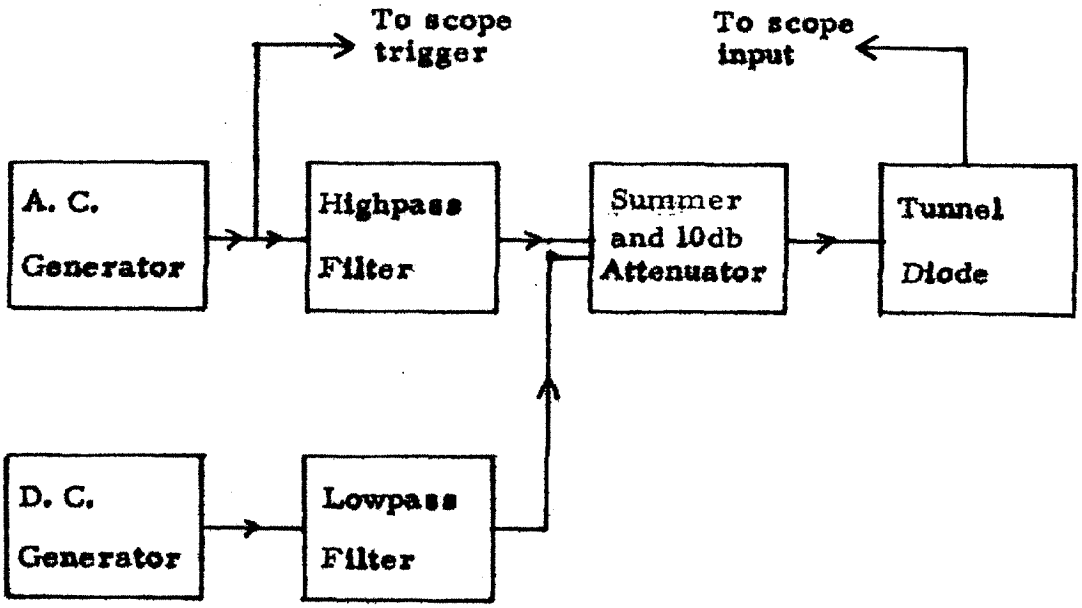
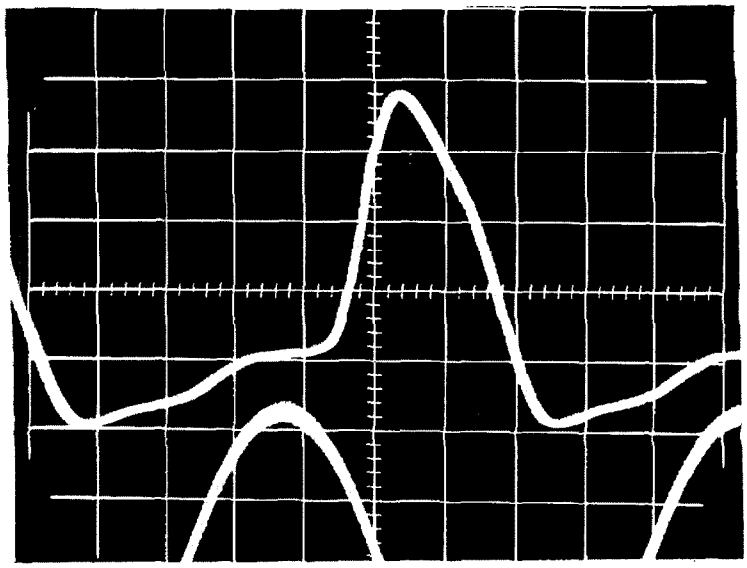
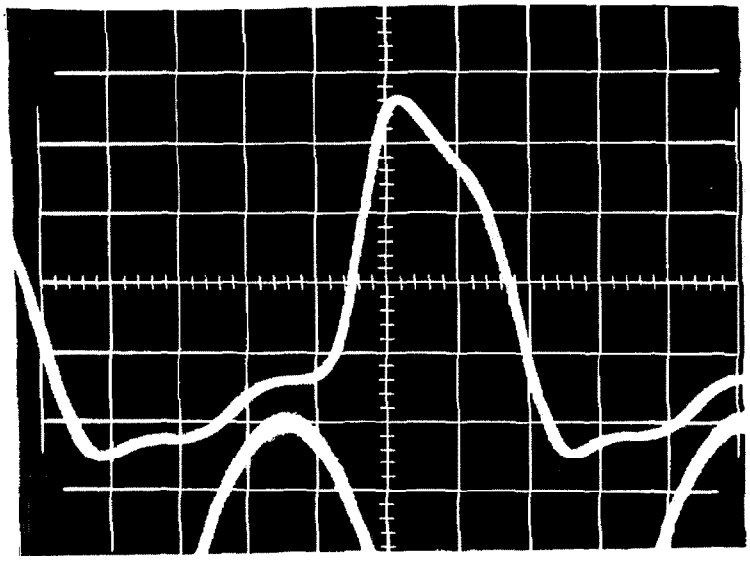

To scope
trigger
To scope
input
A. C.
Generator
Highpass
Filter
Summer
and 10db
Attenuator
Tunnel
Diode
D. C.
Generator
Lowpass
Filter

Figure 2. 20a

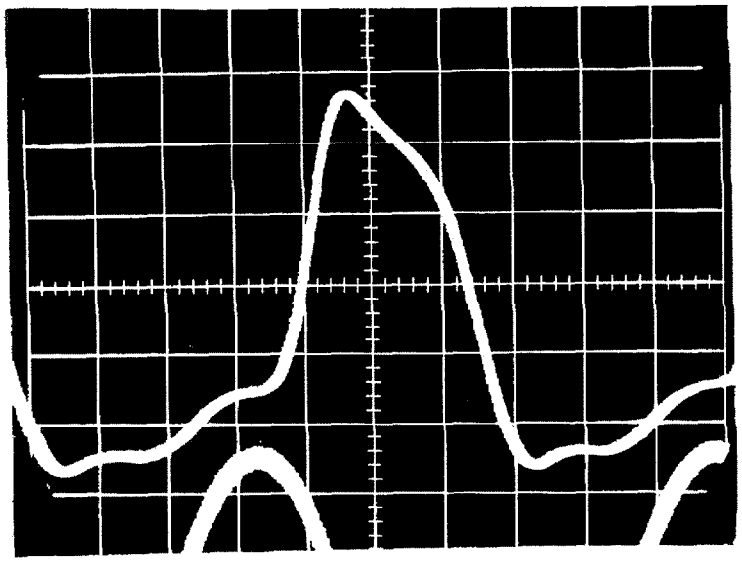


Gain = 7

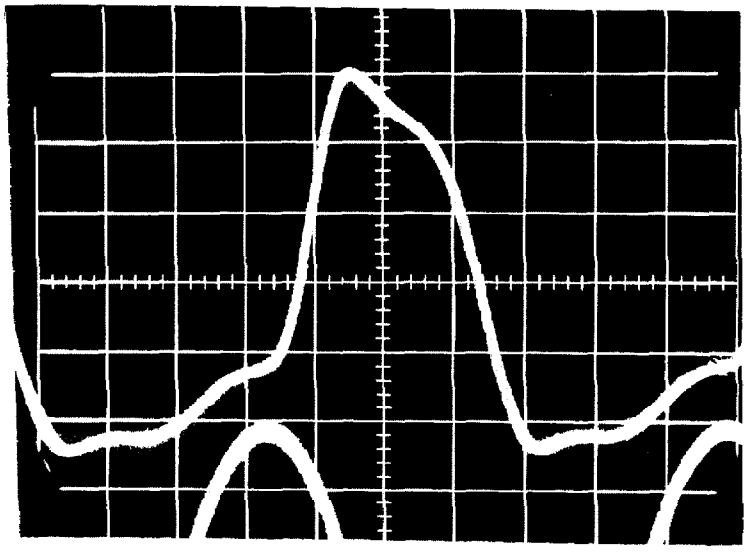


Gain = 5.25

Figure 2.20b (Part 1):- Output pulse when A. C. bias component is employed.



Gain = 4.2



Gain = 3.4

Scales:- Hor. 0.5ns/cm. Ver. 100mV/cm.

Figure 2.20b (Part 2):- Output pulse when A. C. bias component is employed.

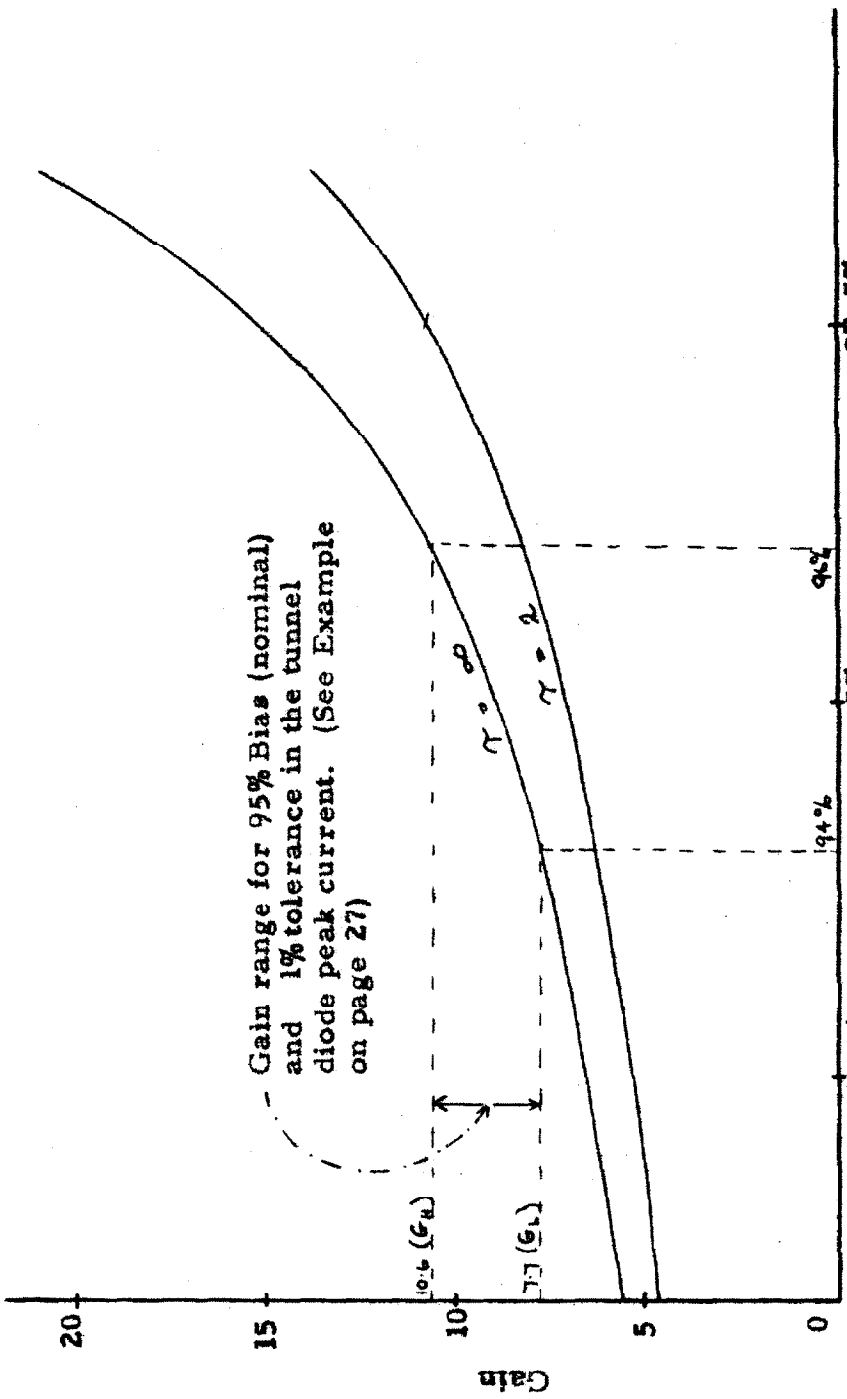
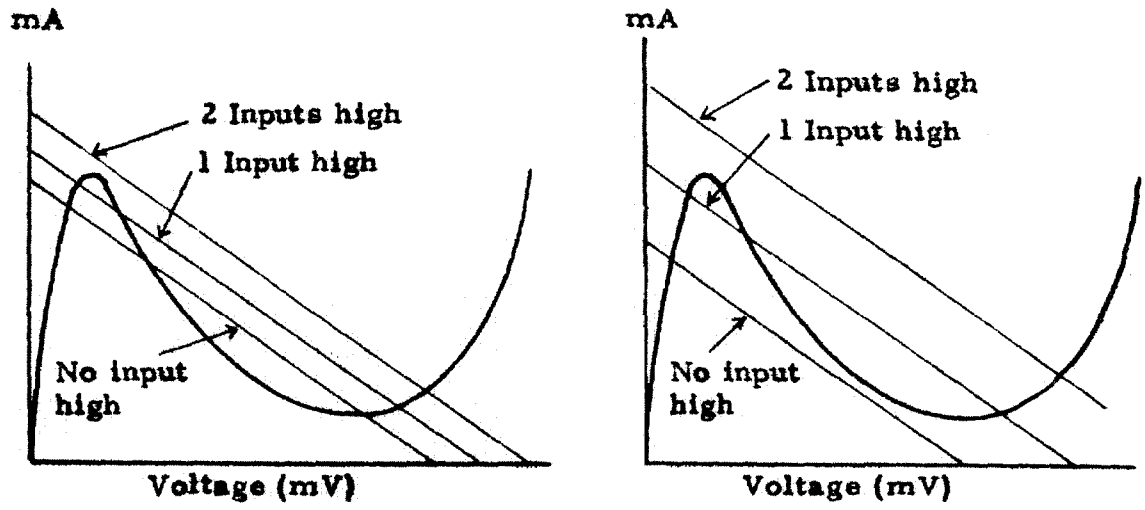


Figure 2.21:- Gain vs. % bias for fixed values of γ



High %Bias
High G^1
High τ
High % variation in τ

Lower % Bias
Lower G^1
Lower τ
Lower % variation in τ

Figure 2. 22:- The direct AND gate (2 inputs)

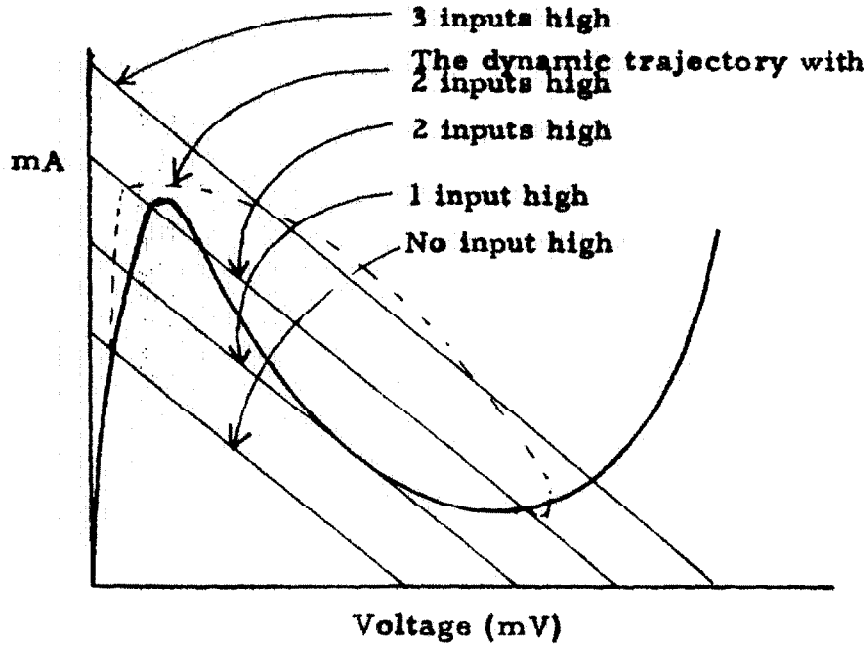


Figure 2. 23:- the direct AND gate (3 inputs)

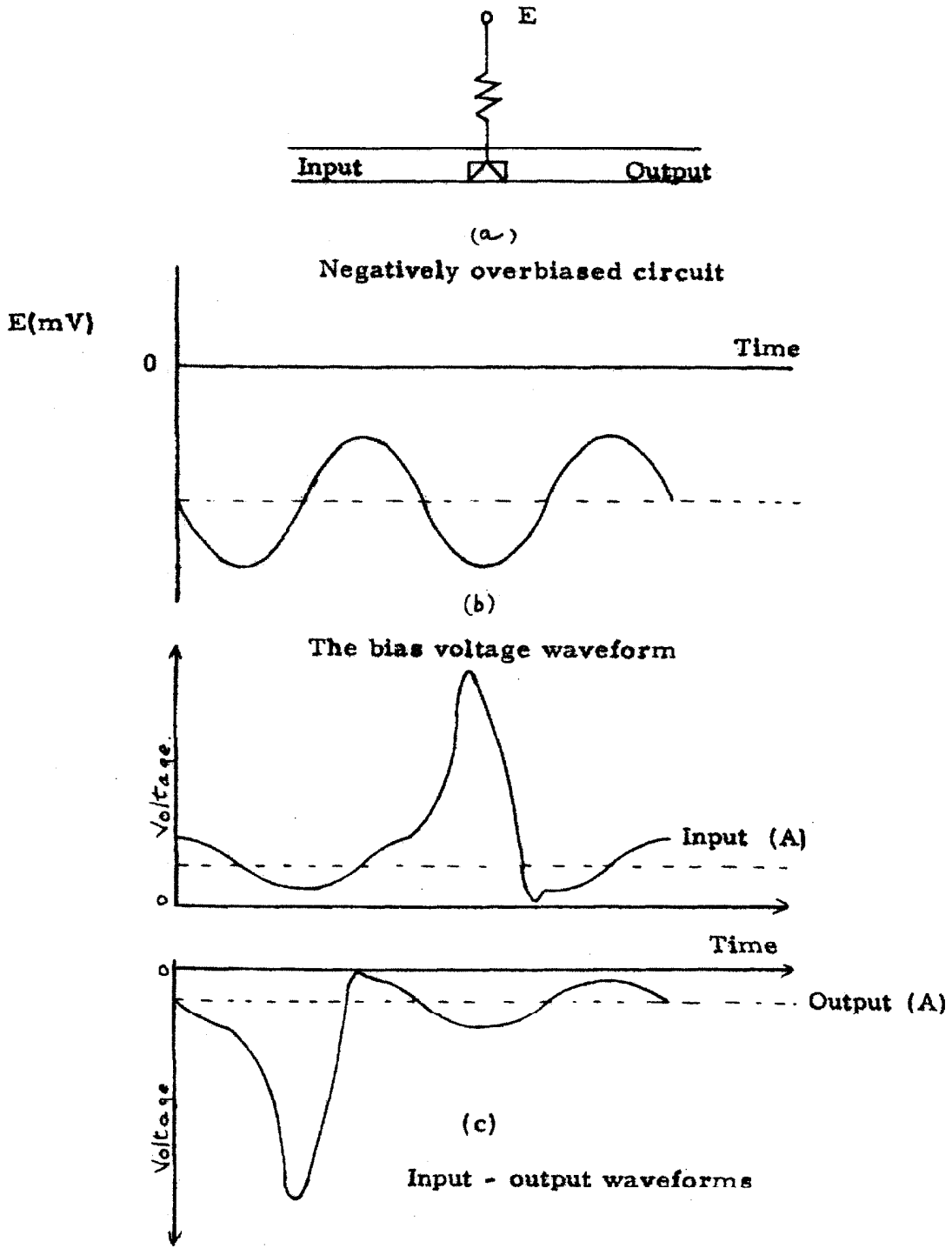


Figure 2. 24;- Signal modification prior to input to modified AND gate

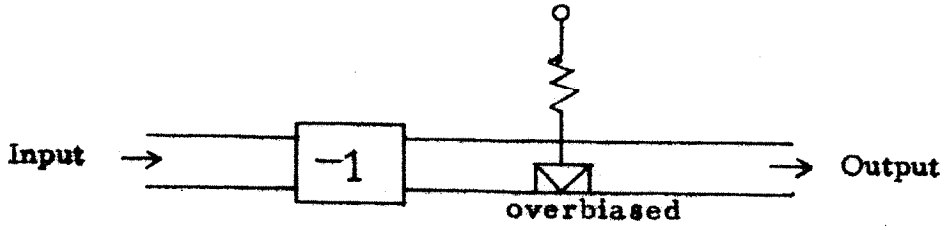


Figure 2.25: COMPLEMENT circuit

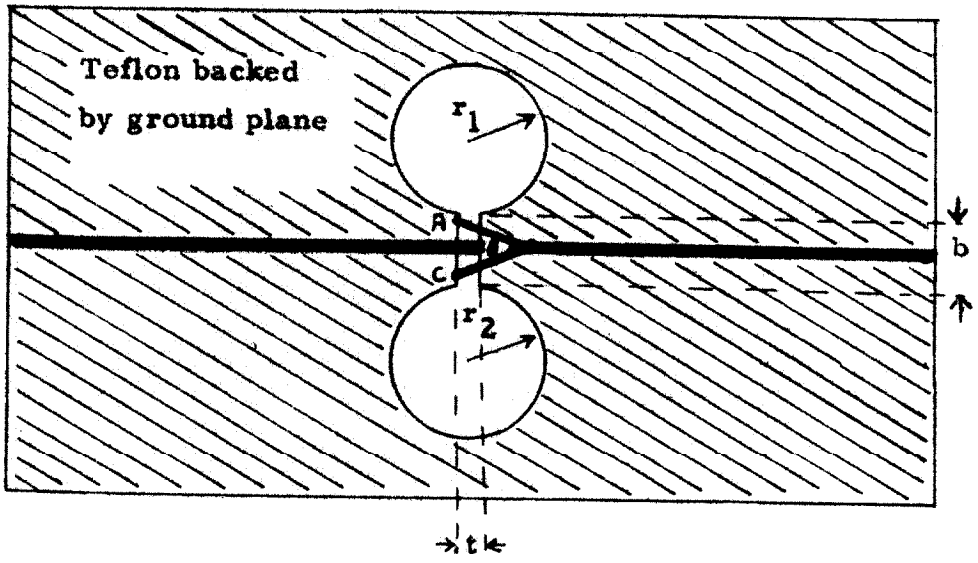


Figure 2.26: The inverting transformer

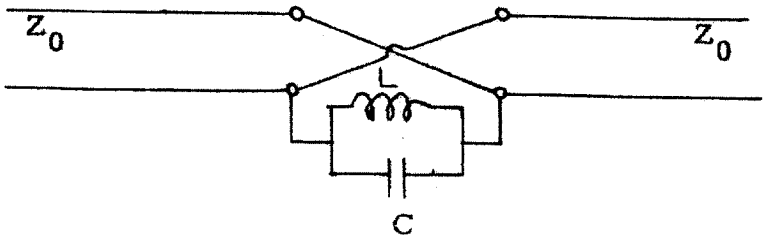


Figure 2.27: Approximate equivalent circuit of the inverting transformer

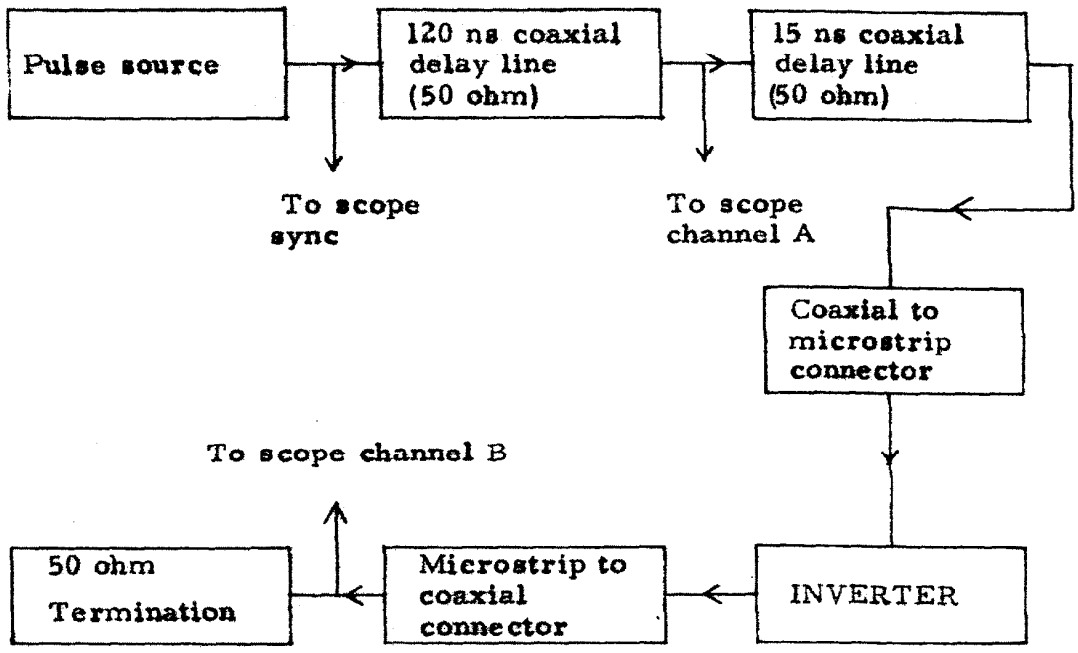


Figure 2.28; Test circuit to measure the response of the inverting transformer.

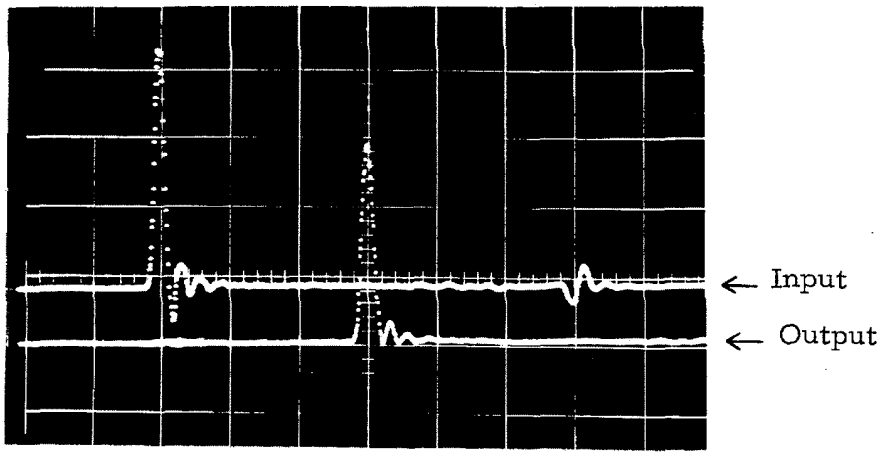


Figure 2.29a:- Direct Microstrip Line
Scale:- Hor. 5ns/cm.

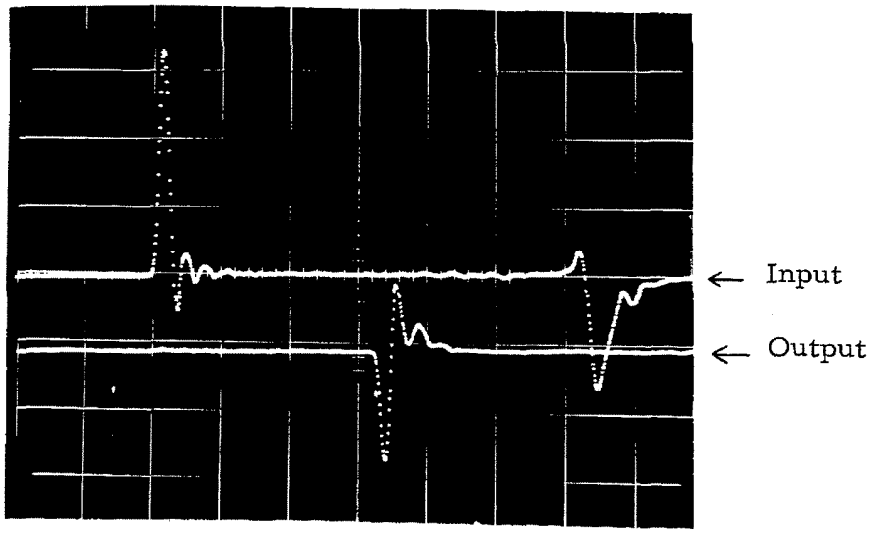


Figure 2.29b:- Inverted Microstrip Line
$r_1 = r_2 = 1$ inch.

Scale:- Hor. 5ns/cm.

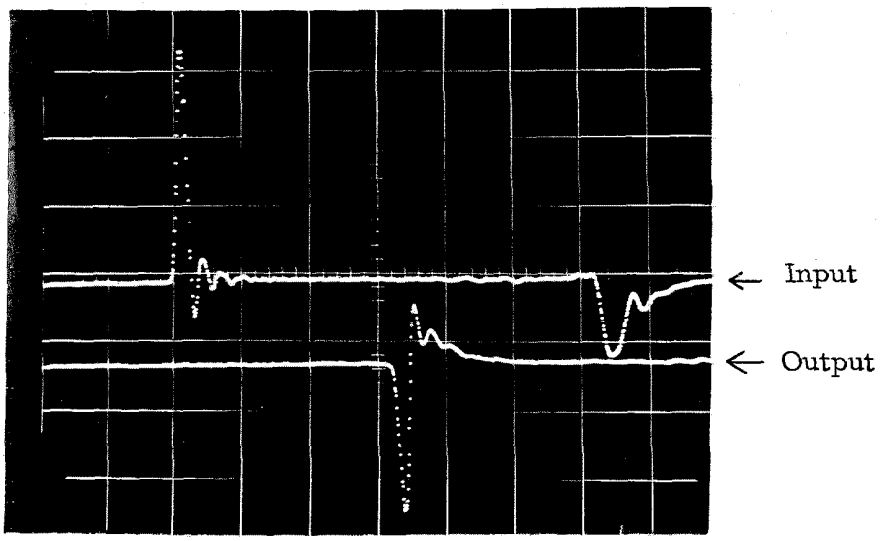


Figure 2.29c:- Inverted Microstrip Line
$r_1 = r_2 = 1.8$ inches.

Scale:- Hor. 5ns/cm.

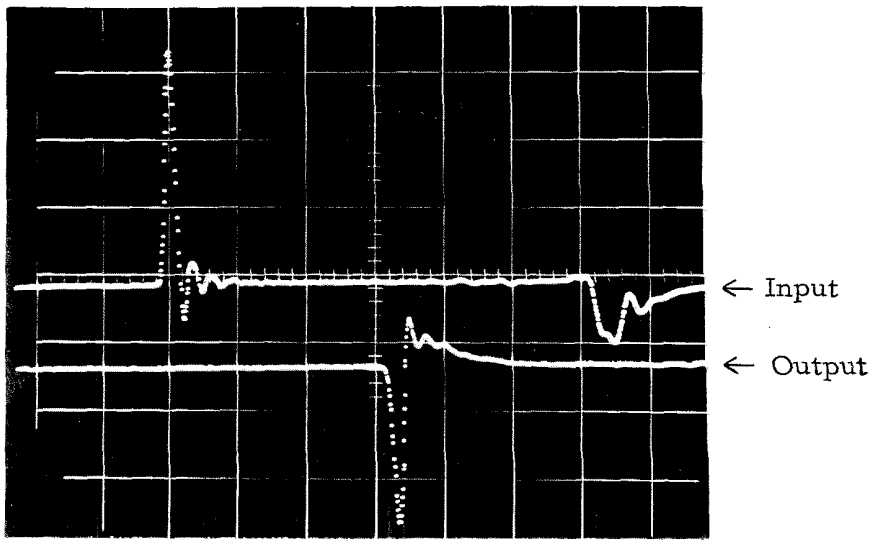


Figure 2.29d:- Inverted Microstrip Line
$r_1 = r_2 = 2.3$ inches.

Scale:- Hor. 5ns/cm.

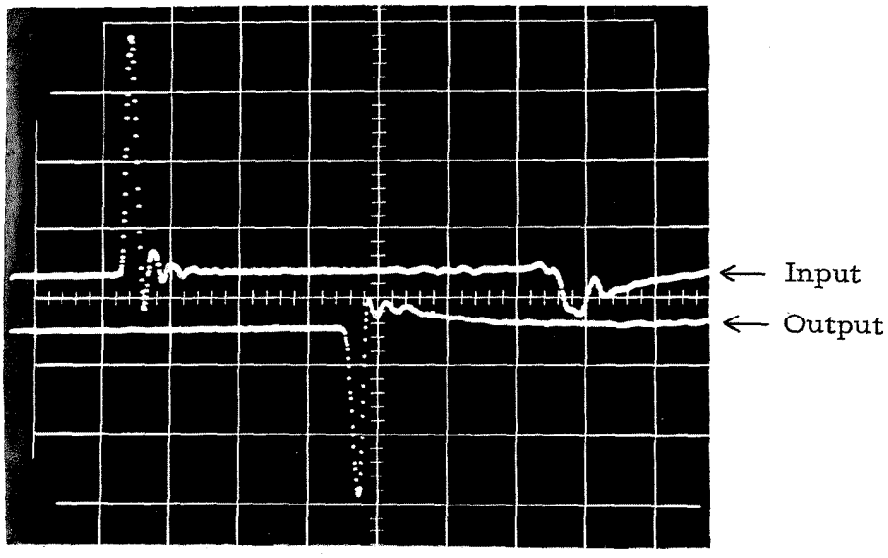


Figure 2.29e:- Inverted Microstrip Line
r_1 = 2.3 inches
r_2 = ∞

Scale:- Hor. 5ns/cm.

PART 3

THE CONNECTION OF LOGICAL ELEMENTS

In OR, AND and COMPLEMENT circuits the logically correct output depends only on the state of the inputs and accordingly these circuits must not respond to the pulses which return along their output lines. Since the tunnel diode is a two terminal device these return pulses must be attenuated, suppressed or cancelled. In this part some possible methods of connection of the logic elements of the previous part will be investigated the primary object being to make the diodes insensitive to pulses returning along the output lines but at the same time responsive to the pulses coming from the input lines.

1) Passive Network Coupling.

Consider the two diodes A and B connected by a transmission line of characteristic impedance Z_0 in series with a linear passive bilateral network (N) as shown in figure 3.1. The Reciprocity Theorem [3] can be employed with the result that if the output of A can trigger B then the output of B can trigger A and vice versa if the diodes are identical and have the same load line and % bias. Hence, if the coupling is to connect the output of A to the input of B it is immediately seen that the necessary property of insulating A from the output pulse at B is not obtained.

2) Directional Coupling Using Blocking Diodes.

When the network (N) of figure 3.1 is linear by the reciprocity theorem the current pulse I_B produced at diode B when A switches is equal to the current pulse I_A produced at diode A when B switches. If N is a directional network the amplitude of these current pulses will be no longer equal. Defining the directionality D by the equation

$$D = \frac{I_{Bmax}}{I_{Amax}}$$

we see that the type of directional coupling needed is that which gives a high value to D since this effectively insulates A from the output of B.

Suppose the network N at the input to B consists of a blocking diode in series with a transmission line whose characteristic impedance is real and equal to Z_0 as shown in figure 3.2. Neglecting the forward impedance of the diode the directionality factor D will simply be

$$D = \frac{V_{max}}{V_{2max}}$$

where V_{max} and V_{2max} are the maximum values of V_1 and V_2 when the diode switches from the low to the high state. An inspection of figure 2.8 shows that a good approximation to V_1, when the D. C. bias value is removed is

$$V_1(t) = \begin{cases} \frac{Vmax}{2} \left[1 - \text{Cos} \left(\frac{\pi t}{2t_1}\right)\right] & 0 < t < 2t_1 \\ Vmax & t > 2t_1 \end{cases}$$

as illustrated in figure 3.3a.

For low values of inductance and a tunnel diode of capacity C and peak current I_p

$$2t_1 = \tau \frac{C}{I_p} \text{ m}\mu\text{secs.}$$

Since "return to zero" A. C. bias circuits are of primary interest it will be further assumed that V_1 returns to zero giving mirror symmetry about $2t_1$ (see figure 3.3b) so that

$$V_1(t) = \begin{cases} \frac{Vmax}{2} \left[1 - \text{Cos } \pi t/(2t_1)\right] & 0 < t < 4t_1 \\ 0 & t > 4t_1 \end{cases}$$

Neglecting A. C. bias noise and assuming the blocking diode has the equivalent circuit of figure 3.4 where r is zero if the diode is forward biased and infinite when reversed biased V_2 is simply as illustrated

in figure 3.5 where I and the initial voltage across C_B are zero at t=0. The solution is

$$\frac{V_2(t)}{Vmax} = \frac{1}{2}\left[\frac{e^{-t/(C_B Z_0)}}{1 + 2t_1/(\pi C_B Z_0)^2} + \frac{\text{Sin}\{\pi t/(2t_1) - \theta\}}{\sqrt{1 + 2t_1/(\pi C_B Z_0)^2}}\right]$$

for $0 \leq t \leq 4t_1$

where $\theta = \tan^{-1}\left[\pi C_B Z_0/(2t_1)\right]$

The plot of $V_2(t/t_1)/V_{max}$ for various values of $t_1/(C_B Z_0)$ is shown on figure 3.6 and the directionality $D = V_{max}/V_{2max}$ is plotted against $t_1/C_B Z_0$ on figure 3.7.

EXPERIMENT:- The circuit schematically shown on figure 3.8a was set up with co-axial circuitory. A 20 ma germanium strip line tunnel diode (R.C.A. IN3129) and an axial packaged germanium back diode (G.E. BD-3) were mounted in a modified BNC connector. The voltages V_1 and V_2 were measured across 50 ohm scope terminations. The bias had the shape shown in figure 3.8b and was fed through a 50 ohm transmission line the positive step being supplied with a repition rate of about 100/sec. The amplitude of this positive step was set to give marginal triggering of the diode. The oscillographs of the voltages V_1 and V_2 are shown on figure 3.9. Clearly the experimental value of D = 3.5 and t_1 = 0.6 mμ secs. The value of the blocking diode capacity was 4pF thus making $t_1/(C_B Z_0) = 3$. From figure 3.7 the theoretical value of D is 4.1. Hence, the experimental value is slightly lower than the theoretical and this discrepancy is mainly due to reverse conduction in the blocking diode and inductance in series with the blocking diode. A careful examination of V_2 on figure 3.9 shows a slightly negative value of the voltage V_2 after the diode had switched and this negative overshoot is characteristic of series inductance.

Turning now to figure 3.10 which will be considered as an OR gate with two inputs and two outputs clearly the return pulse along the input line will depend on whether or not an input pulse appeared on that line. If an input pulse occurs only on line A then the input - output pulses will be as shown on figure 3.11 where the input pulse on line A is assumed to be some fraction of the output on line C or D. Initially the input pulse on line A is negatively reflected but is later positively reflected when the diode switches with the result that V_{Amax} will be slightly greater than V_{Bmax}. Because of this and the effects of the non infinite reverse resistance and the series inductance of the blocking diode the directionality as shown in figure 3.7 is slightly on the optimistic side.

Consider a logical circuit with n inputs and n outputs. The return pulses along the n output lines must be equivalent to less than one input. To obtain a rough approximation to the blocking diode requirements assume that these return pulses should be at most equivalent to half an input.

$$\frac{D}{n} > 2$$

The third column of Table 3.1 can be then be constructed using figure 3.7. If a 20 mA tunnel diode and a 25 ohm load line are used and the output impedance of an input line is assumed equal to DZ_0 then

$$\frac{DZ_0/n}{1 + D} = 25$$

or

$$Z_0 = 25n(1 + 1/D)$$

Assuming the minimum values of D the values of Z_o corresponding to the given values of n are then obtained. An inspection of figure 2.14 reveals that a value of $\tau < 1.5$ is reasonable and if the capacity of the 20mA tunnel diode is less than 10 pF (e.g. R.C.A. type

TD182) then from equation 2.9

$$t_1 < \frac{1.5}{2} \; 10/20 \quad < \quad 0.375 \; m\mu \text{ secs}$$

TABLE 3.1

n	D	$t_1/C_B Z_0$	Z_0 (20mA tunnel diode)	Maximum blocking diode capacity (C_B) t_1 = 0.375 mμ secs.
2	> 4	> 2.8	62.5	2.14 pF
3	> 6	> 4.5	87.5	0.95 pF
4	> 8	> 6	112.5	0.56 pF

The maximum permissible values of the blocking diode capacity (column 5 of Table 3.1) are now easily determined since Z_0 and the upper bound of $t_1/C_B Z_0$ are known for the given values of n.

These maximum values are extremely low especially for n > 2. Even with n = 2(i.e. two inputs and two outputs) a blocking diode whose capacity must be about 2pF through which a 20 mA tunnel diode can be triggered from the output of a similar stage must be found. It should be remembered that Z_0 is inversely proportional to the peak current (I_p) and the maximum permissible blocking diode capacities are accordingly proportional to I_p. Hence, by using a 100 mA tunnel diode with an I_p/C ratio of 2 mA/pF and blocking diodes of 4 pF * it is possible to achieve the necessary directionality for an OR gate with n = 3 (three inputs and three outputs). Some improvement can also be obtained using multistage current amplification. (4)

---

* Examples of 4pF blocking diodes are:-
1) R.C.A. type nos. TD-151 and TD-152
2) G.E. type no. 4JF2-BD3

Apart from the high power requirements this approach has two major disadvantages.

1) The non linearity of the blocking diodes gives severe harmonic distortion of a sinusoidal clock.
2) In the case of an OR gate driving a modified AND gate or a COMPLEMENT gate the blocking diodes will allow the negative return pulses to pass thus destroying the logic of the OR gate.

While the first of the above two objections could be overcome by using a suitably phased "spike" clock or a synchronous d. c. biased monostable circuitry (presumably using inductive switching) the second is a far more serious problem.

In the following sections of this part an alternative coupling method permitting direct connection of the simple logic elements of Part 2 will be studied.

3) Synchronized Coupling Techniques

In the previous section no effort was made to utilize the clock phase as a possible method of suppression of the reflected pulses (i. e. these pulses that are incident on the output terminal of a diode). Suppose in figure 3.12 the A. C. phases of diodes A and B can be arranged so that when A switches its output pulse reaches B when E_B is a maximum but when B switches it output reaches A when E_A is a minimum. Then, except for the effects of multiple reflections, the necessary directionality is obtained and logical information will propagate from A to B as indicated by the arrow on figure 3.12. Due to the fact that the output of A (if high) will lag the clock by about 1/4 of the clock period (figure 3.13) it is impossible to obtain the correct phase at B without a loss in the transmission line. Suppose in figure 3.12 that the delay time of the line is

$$\nu = \frac{j}{2} \quad T + \nu_1 \qquad (3.1)$$

where T is the clock period, j is an integer > 0 and $0 \leq \nu_1 < T/2$. Then for optimum suppression the pulse arriving at A from B should have its maximum when the clock at A is at its lowest point. Accordingly if the switching delay is ν_2 as illustrated in figure 3.13 then

$$2\nu_2 + 2\nu_1 = \delta T + T/2 \qquad (3.2)$$

where δ = 0 or 1 and the clock at B must lag that at A by the time interval

$$\Delta t = \nu_2 + \nu \qquad (3.3)$$

Since the maximum operating frequency will roughly correspond to a value of $\nu_2 = T/4$ this value of ν_2 will be assumed.

1) j odd

If n is odd equations 3.1, 3.2 and 3.3 become

$$\nu_1 = 0 \qquad (3.1a)$$

$$\nu = \frac{j}{2} T \qquad (3.2a)$$

$$\Delta t = 3T/4 \qquad (3.3a)$$

Essentially then the logical elements must be connected by delay lines whose lengths are odd multiples of the half wave length (at the clock frequency) and in the direction of propagation the phases of the A. C. voltage across successive diodes must lay by an angle of $3\pi/2$. The problem now is to design a system with these two properties.

Consider an infinite chain of identical diodes in the low voltage state with each one connected to its nearest neighbour by 1/2 wave length lines all of the same characteristic impedance Z_0 and fed through a bias resister R_0 with A. C. superimposed on D. C. and the applied A. C. phase at each station lagging the one on its left by $3\pi/2$ as illustrated in figure 3.14. From symmetry the combined effects

of the clocks applied at stations B and D will produce a standing wave of zero amplitude across the diode at station C. Thus the voltage across the diode at station C will not be altered by the presence of stations B and D and the traveling waves originating at B and D will not be attenuated at C and similary those originating from E and A will not be attenuated at D and B respectively.

It will be now assumed that the impedance of a diode in the low state is constant. This is equivalent to saying its series inductance, capacity and the slope of its V-I curve are all constant in the range of the A. C. oscillation (see figure 3.15). Then the voltage across each diode will be sinusoidal and of equal magnitude and if the phase across the diode at C is $\underline{/\alpha}$ then from symmetry that across B and D will be $\underline{/\pi/2 + \alpha}$ and $\underline{/-\pi/2 + \alpha}$ respectively and so on. Hence, if V is not equal to zero the primary requirement for directionality is achieved.

The magnitudes of V and α can be calculated in the following way. In figure 3.14 there is between station C and E a line of unit wavelength with opposite voltages at its ends. The transmission line equation then is

$$V\underline{/\alpha} = V\underline{/\alpha + \pi}\,\mathrm{Cosh}\Gamma L - I_s Z_0 \mathrm{Sinh}\Gamma L \qquad (3.4)$$

where I_s is the current supplied to the line at C and

$$\Gamma L = \alpha' L + j\beta L \qquad (3.5)$$

$$\beta L = 2\pi \qquad (3.6)$$

$$e^{\alpha' L} = \text{line attenuation (X)} \qquad (3.7)$$

From equation 3.4

$$\frac{V\underline{/\alpha}}{I_s Z_0} = \frac{\mathrm{Sinh}\,\Gamma L}{1 + \mathrm{Cosh}\,\Gamma L}$$

and using equations 3.5, 3.6 and 3.7

$$\frac{V\angle\alpha}{I_s Z_0} = Z_0 \frac{X-1}{X+1} \qquad (3.8)$$

Hence, the A. C. bias voltage $V\angle\alpha$ at station C is unchanged when the circuitry to the right and left of C is replaced by an infinitely long line of characteristic impedance

$$Z_0^1 = \frac{Z_0}{2} \frac{X-1}{X+1} \qquad (3.9)$$

The equivalent A. C. bias circuit is then that of figure 3.16 where the A. C. bias ($E\angle 0$) is equal to $E\sin\omega t$. Clearly V = 0 for lossless lines (X = 1).

It is of course possible to increase the length of the coupling lines by any multiple of the wavelength (at the clock frequency) and the attenuation X will be that along a length of line equal to twice the coupling length.

2) Finite chain of diodes (j odd).

Suppose that there are no diodes to the right of B in figure 3.14. It is possible to simulate the effects of the missing diodes by a stub transmission line suitably terminated. The infinite chain of figure 3.14 consists of two independent infinite chains as shown in figure 3.17 since the diodes of one chain are at the points of zero standing wave amplitude of the other chain. The voltage on the line between stations B and C is then the superposition of the voltages due to the two independent chains.

Using the notation of figure 3.17

$$E_1 = V\angle\alpha \left[\cosh \Gamma y - \frac{X+1}{X-1} \sinh \Gamma y \right]$$

$$= V\angle\alpha \left[-\frac{e^{\Gamma y}}{X-1} \right] + V\angle\alpha \left[\frac{X}{X-1} e^{-\Gamma y} \right]$$

$$\omega_1 \qquad\qquad \omega_2$$

and

$$E_2 = jV/\underline{\alpha} \left[- \frac{e^{\Gamma z}}{X - 1} \right] + jV/\underline{\alpha} \left[\frac{X}{X - 1} \right] e^{-\Gamma z}$$

ω_3 ω_4

where

$$\Gamma = \alpha^1 + j\beta \ , \ \beta L = 2\pi$$

and

$$e^{\alpha^1 L} = X$$

Clearly there are four traveling waves (ω_1, ω_2, ω_3, and ω_4) between stations B and C. The two waves ω_2 and ω_3 are moving from C to B and ω_1 and ω_4 are moving from B to C. also, ω_1 and ω_3 have the same phase at $\beta Z = \pi/4$ (i. e. $\beta y = 3\pi/4$) and the ratio of their amplitudes is

$$\left. \frac{/\omega_1/}{/\omega_3/} \right|_{\beta Z = \pi/4} = e^{\alpha^1 L/4} = X^{1/4}$$

at the same point ω_2 and ω_4 have the same phase (opposite to that of ω_1 and ω_3) and the ratio of their amplitudes is

$$\left. \frac{/\omega_4/}{/\omega_2/} \right|_{\beta Z = \pi/4} = e^{\alpha^1 L/4} = X^{1/4}$$

Accordingly the effects of the diodes to the right of B can be simulated by a 1/8 wavelength line identical to the coupling lines and terminated to give a positive reflection coefficient of $1/X^{1/4}$. Since $X^{1/4}$ is the two way attenuation factor of the 1/8 wavelength stub line a positive reflection coefficient of unity could also be employed if the attenuation factor of the line were squared. A short circuited 3/8 wavelength stub could also be used. Hence, with coupling lines that are odd multiples of the half wavelength a 1/8 wavelength open circuit

or a 3/8 wavelength short circuit stub line can be used to terminate at the receiving end * of an infinite chain of diodes. A similar analysis for the sending end ** results in a 3/8 wavelength open circuit line or a 1/8 wavelength short circuit line. The two way loss in the shorted or open circuited stub must be always equal to the one way loss in the coupling lines.

3) j even (wavelength coupling lines).

If the length of the coupling lines is some integral multiple of the wavelength then the direction of propagation will be the reverse of that for j even. The infinite chain can also be terminated and the correct termination at the sending end is the same as that at the receiving end with j odd and vice versa. Again the two way attenuation in the stubs has to be equal to the one way loss in the coupling lines.

4) Multiple Reflections.

Multiple reflections between diodes can be divided into two classes namely those due to negative reflections of trigger pulses (class a reflections) and those due to negative reflections of suppressed pulses (class b reflections).

Class a reflections

The output pulse from a diode (A) impinging on the next diode in the direction of propagation (diode B) will be initially negatively reflected at B and returning to A will be again negatively reflected so that it will reappear at the input to B an integral number of bit times later and may now lead to false triggering of B unless it has been sufficiently attenuated by the coupling line.*** Clearly class a multiple reflections have the worst possible effect when the line is distortionless and the reflection

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* i.e. the end towards which the logical information flows.

** i.e. the end from which the logical information flows.

*** "bit time" is used to denote one period of the phasing clock.

coefficients are -1. The effect is then equivalent to a directionality factor X where X is the two way attenuation of the coupling lines. In multiple input-output circuits class a reflections limit the fan in and if this is equal to n and these reflections can at most be equivalent to some fration α of an input then

$$n = < \alpha X$$

It should be noted that termination of the lines at the input or output will overcome this effect but a loss in gain will result.

Class b reflections

In figure 3.14 the pulses originating from C will be suppressed at B with a negative reflection coefficient close to unity. Returning to C these will be again negatively reflected so that they return to B with the same polarity and are again suppressed. If these pulses are attenuated without distortion (Heaviside line) the effect can be tolerated but in practice the attenuation will be low at D. C. and increase with frequency. Accordingly the pulses will spread and cause significant shifts in the D. C. bias except in the simple case of a closed chain of OR gates. In this latter case the D. C. shifts introduced at a diode by the diodes at both sides of it will have opposite sign. In all other cases it is necessary to terminate at input(s) or output(s) of each gate.

5) Except for the closed chain of OR gates which will be later considered as a register or memory device from multiple reflection considerations it is necessary to terminate the transmission lines connecting the logical elements at least at one end. Termination at both ends will further reduce reflections and the current which must be suppressed by the clock thus enabling the circuits to operate with

lower A. C. bias. With terminations at one or both ends the correct phasing can be obtained with lossless lines. Table 3. 2 shows the dependance of the required gain (the G parameter of figures 2. 14) on the terminations when the attenuation factor of the coupling lines (all having the same characteristic impedance Z_0) is equal to $\sqrt{X}$, the fan in and fan out ratios are n and m respectively and the load line is invariant with respect to the termination or the fan in and fan out ratios. In the non terminated case it has been shown from A. C. bias consideration that the

TABLE 3. 2

Termination Type	$G/\sqrt{X}$	Comments
Not terminated	$\frac{n}{2} + \frac{m}{2}$	Multiple reflection problems
Terminated at input	$\frac{n}{2} + m$	Class a reflection eliminated. One class b reflection
Terminated at output	$n + \frac{m}{2}$	One class a and one class b reflection
Terminated at both ends	$n \mid m$	Class a reflections eliminated. No class b reflections

characteristic impedance of the connecting lines was reduced by the factor $\frac{X - 1}{X + 1}$ so that only in cases where X must be high such as in a dynamic register or memory device where a large number of bits are stored in a delay line can the non terminated case be justified. In the logic matrix where the connecting lines will be no longer than a few wavelengths then X will be virtually equal to unity and since

it will be later seen that the gain demands are easily met termination at both ends is optimum in these cases for the following reasons:-

a) Reflections are kept to a minimum as are the currents which must be suppressed by the clock

b) The circuits are symmetrical, the circulating currents in mixed bias circuits are reduced and the D. C. short of the necessary transformer in the complement circuit is removed.

6) Fan in and fan out

With a fan in of n and a fan out of m and termination at both ends the value of the gain (G) must be

$$G = m + n \qquad (3.13)$$

If a value of τ is selected then figures 2.14 give the maximum value of m + n as a function of the percentage bias. For example a τ of 1.5 mμ secs/pF/mA leads to the following values of m + n for different % bias levels:-

% Bias	Maximum value of m + n for τ = 1.5
97.5	8
95	6
92.5	4

If a lower value of τ had been selected the maximum permissable values of the sum of the fan in and fan out integers would be also lower. This implies a compromise between maximum operating frequency and fan in fan out. Since all the coupling lines should preferably have the same characteristic impedance the peak

current of the tunnel diode must be proportional to m + n and the % bias must increase with m + n.

7) The A. C. Bias Amplitude

The A. C. bias amplitude must be large enough to guarantee reset. However, if its amplitude is extremely high the load line will drop below the diode characteristic before the diode can switch. Hence, the optimum A. C. bias is the minimum value which guarantees reset. Here the suppressed currents must be taken into consideration since in the connection of like biased circuits the action of the suppressed currents will be to increase the diode current thus tending to impede reset or cause switching during the negative part of the clock cycle.

Suppose the diode in figure 3.18 has a fan out of m. The maximum suppressed current (I_s) will occur when the diode is low and return pulses occur on all the output lines and at a time when the A. C. bias is low. Hence, the peak to peak A. C. current ($I_{A.\,C.\ p>p}$) must be greater than I_{smax} and so

$$I_{A.\,C.\ p>p} > m\,\frac{/Vout/}{2Z_0}$$

and in dimensionless form

$$\frac{I_{A.\,C.\ p>p}}{I_p} > \frac{m/Vout/}{2}\ \frac{1}{I_pZ_0}$$

In the above I_p and (Vout) are respectively the peak current of the tunnel diode and the output amplitude when the diode switches.

Since

$$\frac{2Z_0}{m+n} \doteq \frac{E_0}{I_p}$$

the above equation becomes

$$I_{A.\,C.\ p>p}/I_p > \frac{m/Vout/}{2Z_0}\ \frac{2Z_0}{(m+n)E_0}$$

$$> \frac{1}{(1+n/m)}\ \frac{/Vout/}{E_0}$$

Also, from figures 2.14 E_0 should be about 500 mv and /Vout/ would then be about 350 mv. The above inequality then becomes

$$\frac{I_{A.C.\ p>p}}{I_p} > \frac{0.7}{1+n/m}$$

Accordingly if the peak to peak A. C. current is 70% of I_p the diode when low will not be switched by the suppressed currents.

More generally the ratio of the A. C. peak to peak current to the diode peak current must satisfy the inequality

$$\frac{I_{A.C.\ p>p}}{I_p} > \frac{\frac{/Vout/}{E_o}\ m_H}{m+n}$$

where m_H is the net number of return pulses with the same polarity as the D. C. bias. Return pulses of opposite polarity count as a minus one in m_H. The maximum value of m_H is accordingly m. The above inequalities are applicable only when the diode is in the low state. If the diode had been high the return pulses will tend to inhibit resetting and this will invariably be a more stringent restriction.

Using the circuit analyser a dynamic analysis was performed to study the effects the suppressed currents, the operating frequency and the % A. C. bias have on the performance of an OR gate when the combined number of inputs and outputs is 8. The tunnel diode circuit is shown on figure 3.18 and the Thevenin equivalent is shown on figure 3.19. Since a gain of 8 [equation 3.13] is required 97.5% bias was selected. Essentially there are four variables:-

a) m_H which is the net number of return pulses (return pulses of opposite polarity to the D. C. bias count as minus 1).

b) The % A. C. bias (i.e. ($I_{A.C.p\ p}/I_p$)

c) The per unit operating frequency

$$\bar{f} = f\, C/I_p = \frac{\omega}{2\pi}\, C/I_p$$

d) The load line which determines the magnitudes of the A. C. and D. C. bias.

The above factors (a), (b), and (c) have at most a second order effect on the optimum value of the load line. Accordingly the bias was selected from figure 2.14C and is about 500 mv. The A. C. and D. C. bias then make

$$E_0(t) = A + B \sin\omega t$$

where

$$A + B = 500$$

and the ratio B/A determines the % A. C. bias.

Next an approximate form was selected for the input and return pulses. The form selected for input was

$$f(t) = \begin{cases} 0 & t < 0 \\ \frac{350}{2}\left[1 - \cos 2\omega t\right] & 0 \le t \le \pi/\omega \\ 0 & t > \pi/\omega \end{cases}$$

and the return pulses were assumed equal to $f(t-\pi/2\omega)$. Hence,

$$E_0 = A + B\sin\omega t + \frac{k\, f(t)}{m+n} + m_H \frac{f(t - \pi/2\omega)}{m+n}$$

where k is the number of high inputs [k was always taken equal to unity since this is the worst case].

Computed dynamic trajectories are shown on figures 3.20, 3.21, 3.22 and 3.23. Figure 3.20 illustrates the effect of the % A. C. bias. The amplitude of the ouput signal decreases as the % A. C. bias increases but the rise time is not seriously affected. On figure 3.21 the % A. C. bias is held constant at 80% and the frequency is varied. Figures 3.22 and 3.23 show the effect of m_H on the reset and with 60% A. C. bias the maximum permissible value of m_H is

3 but with 80% A. C. bias m_H can be as high as 6 (m_H = 7 also O. K. in this case but marginal).

Clearly there is a compromise between the value of m_H and the operating frequency. As m_H increases the % A. C. bias must increase to guarantee reset and to maintain the same output amplitude the frequency must decrease as the % A. C. bias increases. In the cases examined (m + n = 8) 80% A. C. bias gave the necessary output amplitude to give a gain of 8 at values of f up to 0.15 (Kilomegacycles /pF/mA) and the suppressed currents did not cause false switching for values of $m_H \leq 6$. Hence, the maximum operating frequency in this case is about

$$fmax = 0.15\ I_p/C \text{ Kilomegacycles}$$

If the number of inputs and outputs is less than 8 the reset problem will not be as serious. Accordingly with diodes whose I_p/C ratio is 2 mA/pF it is possible to operate at frequencies up to 300 megacycles with $m + n \leq 8$ and $m_H \leq 6$.

On the other hand figure 2.14c predicts a value of τ of about 1.45 mμ secs/mA/pF at a gain of 8 and 97.5% bias and when this value is inserted in equation 2.20 the value of fmax obtained is $0.175\ I_p/C$. Hence, a slight discrepancy is evident and the value of τ in figures 2.14 when inserted in equation 2.20 gives a slightly optimistic value of fmax. Other cases examined gave somewhat similar discrepencies and a more conservative and accurate approximation to fmax is

$$fmax = \frac{1}{5\tau\ C/I_p} \qquad (3.13a)$$

where, as before, τ is given in figures 2.14.

8) Phase Identification and the Connection Rules.

The four phases are numbered 1, 2, 3, and 4 and their schematic vectorial and voltage time relations are shown on figure 3.24. The phase numbers are mod. 4 i. e. phase 5 and phase 1 are the same etc.

a) Directional coupling.

The gate driven by phase i can be connected to that driven by phase i + 1 or i - 1 and the direction of propagation will be from i to i + 1 or i - 1 as indicated in Table 3.3 where n = 0, 1, 2, . . . and the total delay is the time interval (in bit times) between the arrival of the input to one gate and the occurance of the output at the second gate. The minimum delay per stage of 1/4 of the bit time is due to the clock phases rather than the rise time of the diodes.

It should be noted that phase i cannot be connected to itself or phase i + 2 if directionality is required.

TABLE 3.3

D. C. Bias	Direction of Propagation	Length of connecting transmission line in wavelengths	Total Delay in bit times
Phase i and i + 1 both positive or both negative	i to i + 1	n	n + 1/2
	i + 1 to i	n + 1/2	n + 1
Phase i positive and i + 1 negative	i to i + 1	n + 1/2	n + 1
	i + 1 to i	n	n + 1/2
Phase i negative and i + 1 positive	i to i + 1	n	n + 1/2
	i + 1 to i	n + 1/2	n + 1

b) Bi - directional Coupling.

If two diodes A and B are connected so that A can drive or inhibit (or contributed towards driving or inhibiting) B and vice versa then the coupling will be termed bidirectional. With the four phase clock the only bidirectional couplings are where a diode whose A. C. phase is i is connected to another where A. C. phase is i or i + 2.

Bidirectional coupling can sometimes be employed to reduce the number of gates and delay time of a logical network. An example of this type of coupling will occur in the addercircuit [figure 3. 28].

9) Diode Bias and Power Requirements.

Here it is assumed that the diodes are interconnected by terminated lossless delay lines of characteristic impedance Z_0. When the diodes are interconnected the A. C. voltage across each one must be one of four phases in quadrature. Assuming this is so the A. C. power required by each and the relative phase of its driving voltage will now be determined.

The A. C. current $\hat{I}_a$ through any diode A whose A. C. driving voltage is E_a is given by the equation

$$\hat{I}_a = \frac{\hat{E}_a - \hat{V}_a}{R_0} + \sum_x \frac{\hat{V}_x \hat{K}_x - \hat{V}_a}{2Z_0} \qquad (3.14)$$

where $\hat{V}_a$ is the voltage across the diode A, R_0 is its bias resistor, $\hat{V}_x$ is the voltage across the diode X to which A is connected and $\hat{K}_x$ is a rotational vector depending on the length of the interconnecting line. If $\sum_x \hat{V}_x \hat{K}_x = 0$ then the neighboring diodes have no effect on the bias of diode A and for simplicity we will say that diode A is A.C. balanced. In this case equation 3. 14 becomes

$$\hat{I}_a = \frac{\hat{E}_a - \hat{V}_a}{R_0} - (m + n) \frac{\hat{V}_a}{2Z_0} \qquad (3.15)$$

where m and n are the fan out and fan in integers respectively. The power $\hat{P}$ which is supplied is then given by the equation

$$\hat{P} = \hat{E}_a \frac{\hat{E}_a - \hat{V}_a}{R_0} \quad .$$

When $\hat{E}_a$ is eliminated by means of equation 3.15

$$\hat{P} = R_0 I_a^2 + \left[1 + \frac{(m+n)R_0}{2Z_0}\right]\frac{(m+n)}{2Z_0} V_a^2$$

$$+ \hat{V}_a\hat{I}_a \left[1 + \frac{(m+n)R_0}{Z_0}\right]$$

and if

$$R_0 = 2Z_0/K \qquad (3.17)$$

then

$$\hat{P} = \frac{2Z_0 I_a^2}{K} + \left[1 + \frac{m+n}{K}\right]\left[\frac{m+n}{2Z_0}\right] V_a^2$$

$$+ \hat{V}_a\hat{I}_a \left[1 + \frac{2(m+n)}{K}\right] \qquad (3.18)$$

Remembering that the gain equation 3.13 is valid only when $R_0 >> 2Z_0$ the bias resistor is equivalent to K outputs and equation 3.13 now becomes

$$G = m + n + K \qquad (3.19)$$

Hence, a further compromise exists between the A. C. power, gain and fan in fan out integers.

Example:-

Suppose a value of τ of 1.8 is selected. Then from figure 2.14c the maximum value of G is 9. Assuming E_0 = 500 mV and a 20 mA tunnel diode is used then the A. C. power dissipation is that shown on Table 3.4 for varying K on the assumption that m + n+K = 9,

$\hat{V}_a$ and $\hat{I}_a$ are in phase and 80% A. C. bias is employed.

Clearly from Table 3.4 the A. C. power is almost directly proportional to R_0 which is reasonable since the diode is a low impedance device. Also the power even for K = 1 is not excessive.

TABLE 3.4

K	m + n	R_0	P (milli-watts)
1	8	225	9.0
2	7	112.5	4.5
3	6	75	2.9

While the results in Table 3.1 were computed for A. C. balanced diodes when a diode is not balanced the A. C. power dissipation will not change to any great extent.

R_0 could consist of a physical resistor R_0^1 connected to a low impedance (Z) power supply line where

$$R_0 = R_0' + Z$$

and in this way a number of diodes could be fed from one power line.*

The coupling through the power line between any two diodes will be suppressed by the A. C. phase but neglecting this it is at most equivalent to gain G_c where

$$G_c = \frac{m + n + K}{K} Z_0/Z \qquad (3.20)$$

Hence, in the previous example if $Z_0/Z = 10$ (i. e. Z = 11.25 ohms) then G_c is equal to 90, 40, 30 for values of K = 1, 2, 3 respectively.

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*A delay line of characteristic impedance R_0 matched at the power end to a low impedance (Z) power line is also feasible.

Since the lower of these values is considerably greater than Gmax at 97.5% bias and there will also be extensive suppression of the coupling due to the phasing the coupling through the power lines will not be severe.

In a tunnel diode which is not A. C. balanced the only serious consequence will be a phase shift in its anode voltage. This can be corrected by a slight phase shift of its driving voltage computed by means of equation 3.14.

10) The Generation of Boolean Functions.

The logic elements of Part 2 consist of diode circuits which are positively or negatively biased. The diodes can also be under or over biased. The input-output signals are positive (weight +1), negative (weight -1) or virtually at ground potential (weight 0).* The output of a positively (negatively) biased circuit then has weight +1 (-1) or 0 and is a function of the algebraic sum S of the inputs.** There are four classes of diode circuits and these are shown on figure 3.25. On this figure the equations giving the output weights for each class are also shown together with the representation of the inverting transformer which essentially changes the sign of a signal weight.

The inputs and outputs can be indicated by arrows on the connecting transmission lines but for directional coupling the connection rules of Table 3.3 must be satisfied. In cases of bi-directional coupling arrows will be shown pointing in both directions on the transmission line.

Figures 3.26 and 3.27 schematically illustrate the generation of a minterm and a maxterm respectively and a full serial adder is

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* i.e. weight +1 (-1) is associated with the output pulse of a positively (negatively) biased tunnel diode when this diode switches into the high voltage state. The weight 0 is associated with the output voltage of a tunnel diode in the low state.

** More correctly S is the algebraic sum of the input weights (e.g. if there are four input lines and the input pulses on these lines have weights +1, -1, +1 and 0 then S = +1). This algebraic sum if the governing parameter because current summation occurs at the input.

shown on figure 3.28. While some minterms and maxterms can be generated in less than 1 bit time if one bit time is allowed the maximum number of terms possible in a maxterm is n^2 (2n for a minterm) where n is the fan in ratio. The adder has a two bit time delay.

Clearly if the outputs are functions of the inputs only any Boolean expression can be generated and the delay in bit times will depend on the complexity of the outputs. In this case information can be supplied to the inputs at the clock frequency. However, where the outputs or internal states have to be fed back as inputs then it may be necessary to introduce certain dead periods and information must then be supplied to the inputs at a sub multiple of the clock frequency. Redundant elements can be employed to reduce or eliminate the number of dead periods and bi-directional coupling and internal feed back loops can also be employed to this end. In the adder circuit the dead period was eliminated by these latter methods.

No general method of evaluation of the extent to which dead periods must be introduced could be found and no existing theory seemed applicable.* On the other hand, a brief investigation into the logic equations of the LGP 30 computer indicates that inputs could only be supplied on every 5th cycle because of feed back restrictions. This, however, cannot be considered as a truly indicative result since the logic equations of the LGP 30 were minimized to suit the circuitory.

The great advantages of simplicity of the basic logic circuits coupled with their high operating frequency and the simplicity of the connection rules are of sufficient merit to stimulate further investigation on the part of logic designers at least for some special purpose applications.

In Part 4 a possible application to high speed memory devices is outlined.

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*The possible application of Markov processes was suggested.

Summary:- Passive network coupling or directional coupling using blocking diodes cannot be employed to couple the logic elements of Part 2. Apart from the low capacity restrictions on the blocking diodes they are completely ineffective when directionality is required between positive and negative biased circuits. On the other hand, phase techniques incorporating clock suppression of extraneous pulses proved to be a feasible method of connection of the logic elements and multiple reflection are eliminated by termination of the delay lines.

The use of a bias voltage consisting of A. C. superimposed on D. C. where the A. C. amplitude was sufficient to guarantee reset did not seriously alter the value of the available gain and the zero to 90% rise time was in good agreement with the value deducible from parameter τ of Part 2.

The power requirements are low and cross coupling through the power lines will be partially suppressed by the clock phase.

The connection rules are reasonably flexible and more than one configuration is possible for the generation of most Boolean functions. The only essential limitation is that the connection rules remove complete generality as to the types of Boolean functions that can be generated in a bit time. This restriction can always be removed by introducing p dead periods after each live period. In most cases p can be reduced or eliminated by redundant circuitry and bidirectional coupling and will rarely be greater than 2 or 3.

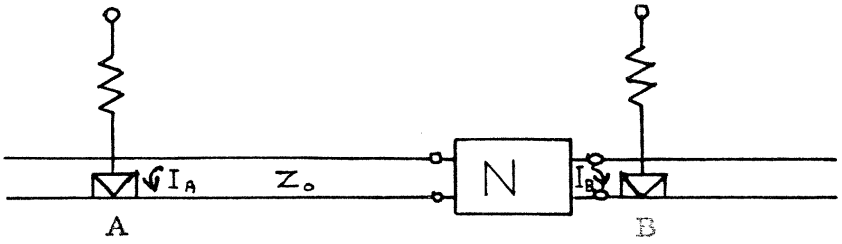


Figure 3.1:- Passive network coupling.

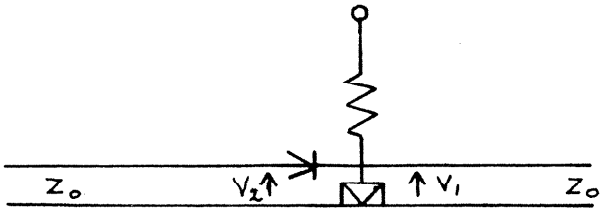


Figure 3.2:- Directional coupling using blocking diodes.

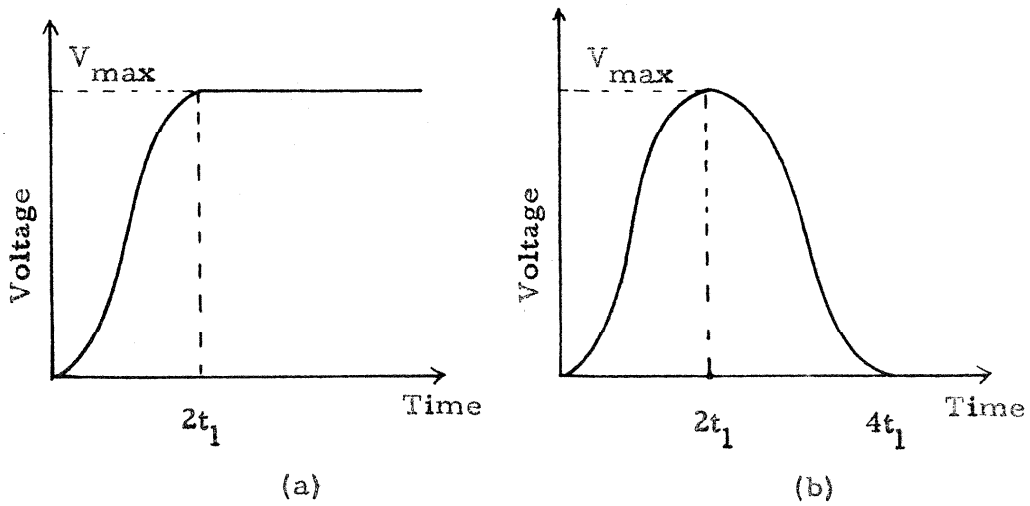


Figure 3.3:- Output voltage waveforms.

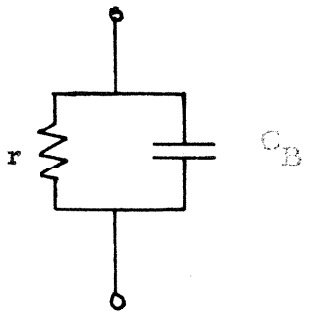


Figure 3.4:- Equivalent circuit of the blocking diode.

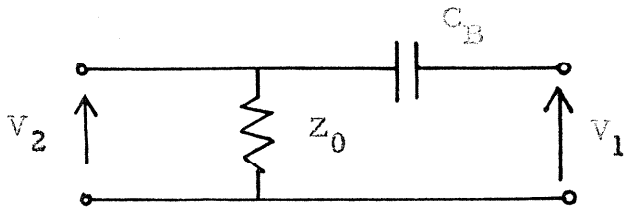


Figure 3.5

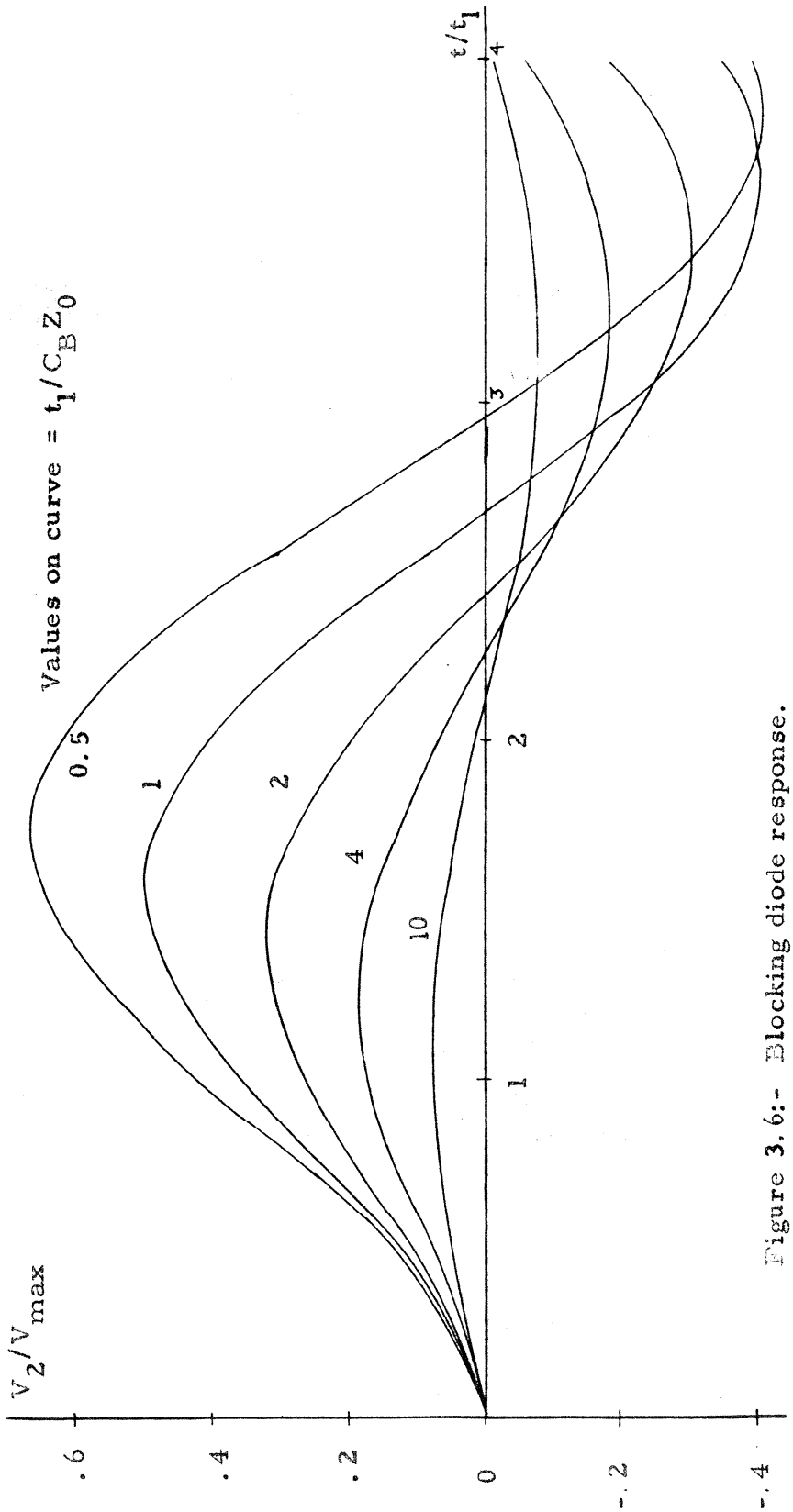


Figure 3.6:- Blocking diode response.

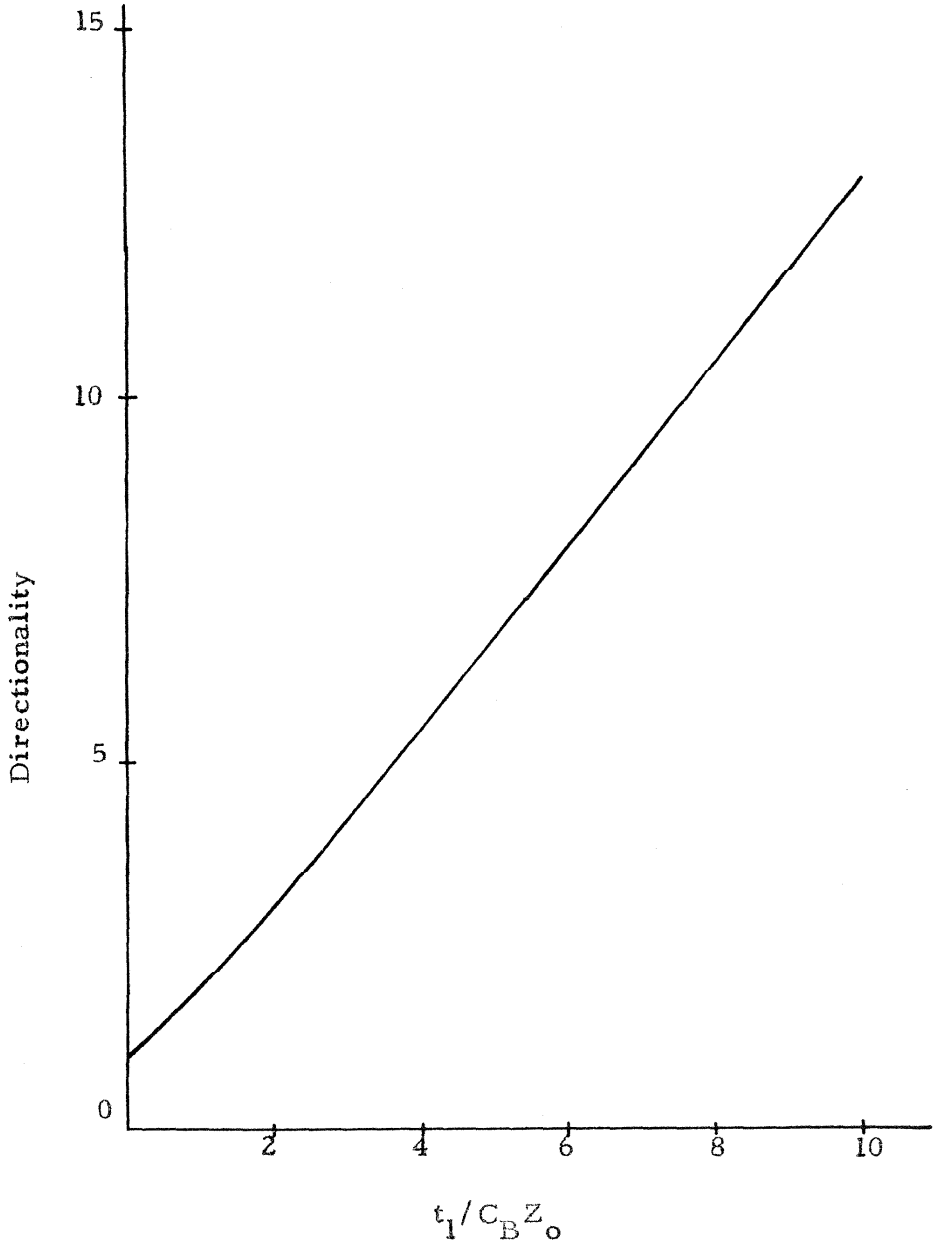


Figure 3.7:- Directionality vs. $t_1/C_B Z_o$

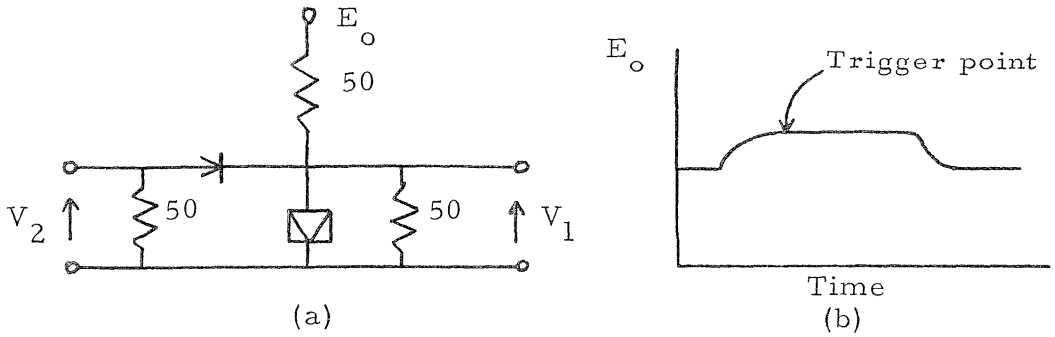
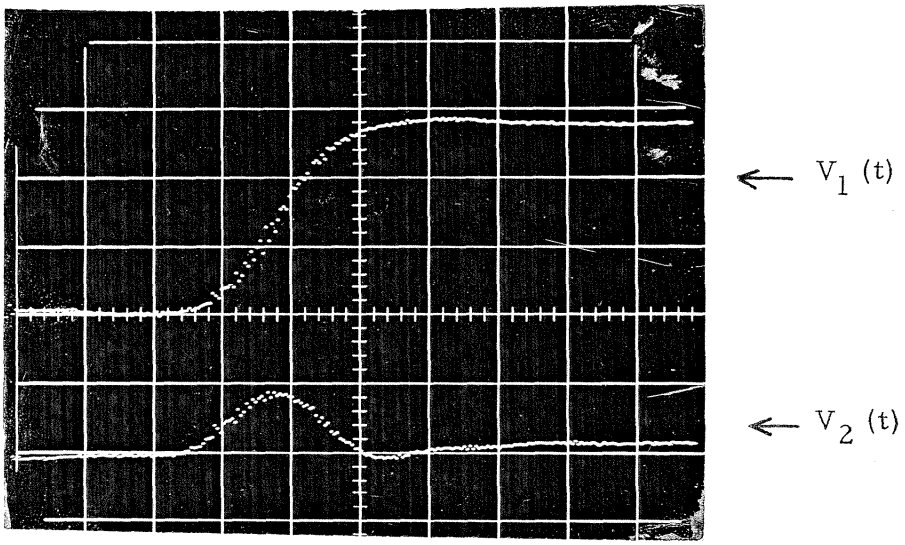


Figure 3.8



Scales:- Hor. 0.4ns/cm. Ver. 100mV/cm.

Figure 3.9:- Response of the test circuit of Figure 3.8.

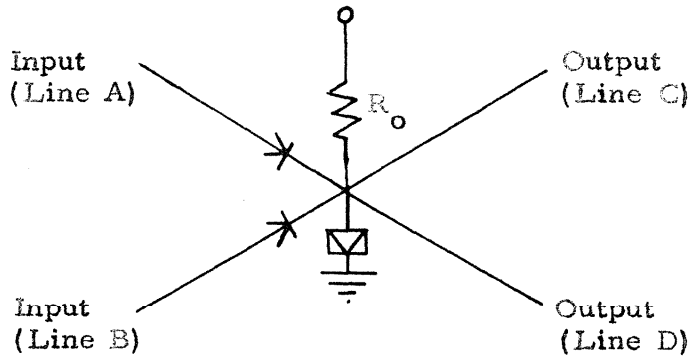


Figure 3.10:- Input-output configuration

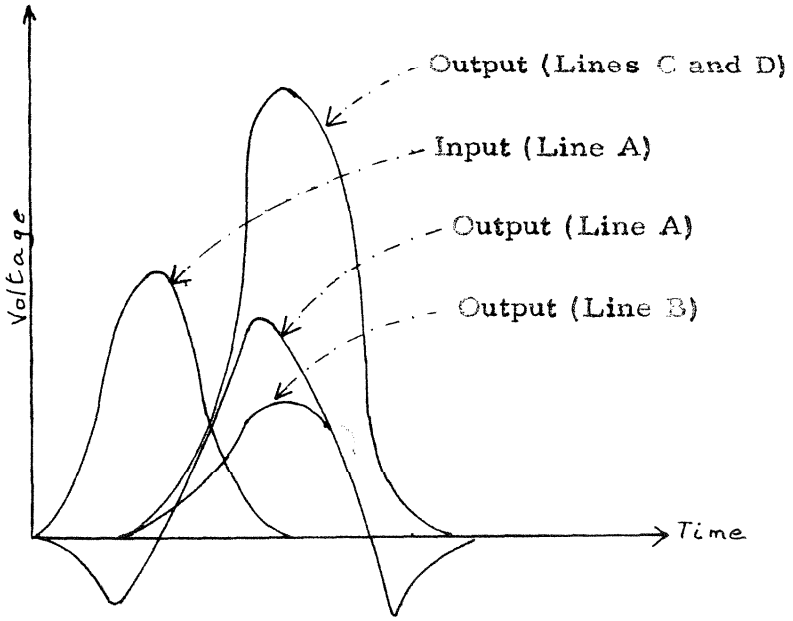


Figure 3.11:- Input-output waveforms of the circuit of figure 3.10 when an input pulse occurs only on line A.

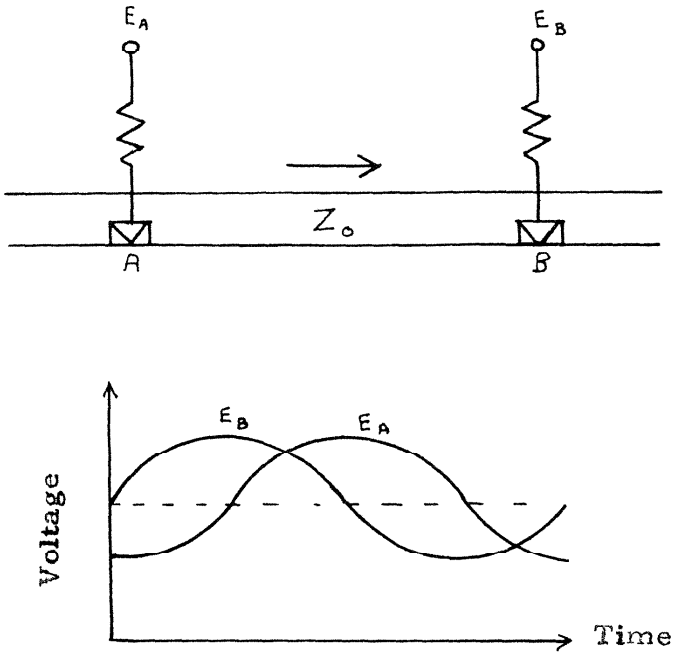


Figure 3.12:- Directionality by phase techniques

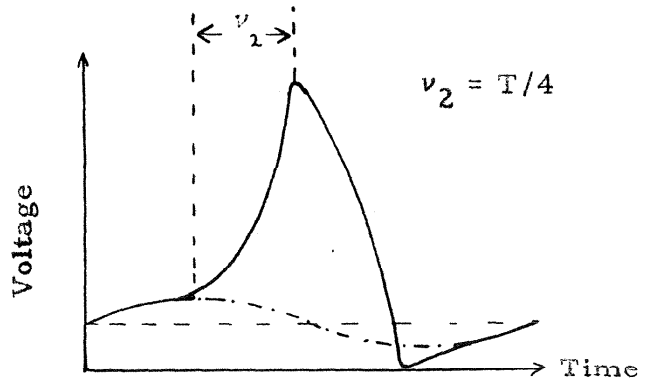


Figure 3.13:- Delay time of a tunnel diode circuit

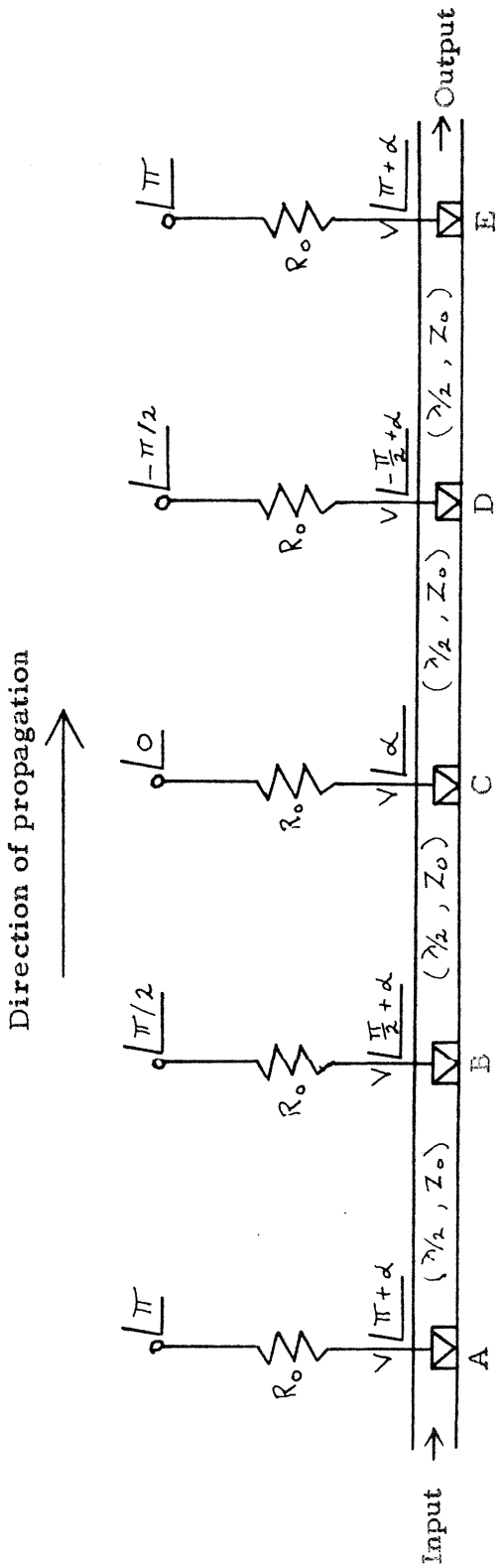


Figure 3.14:- Phase requirements for directionality

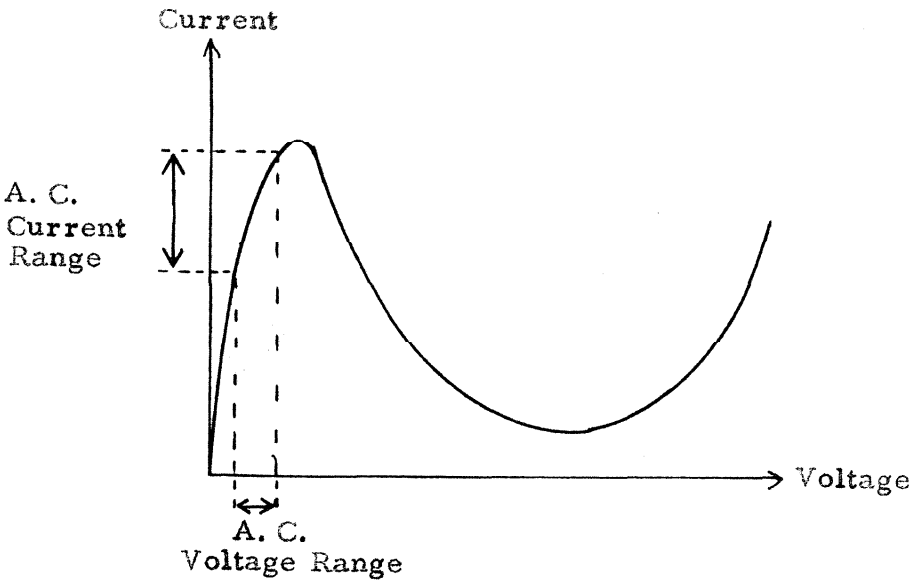


Figure 3.15

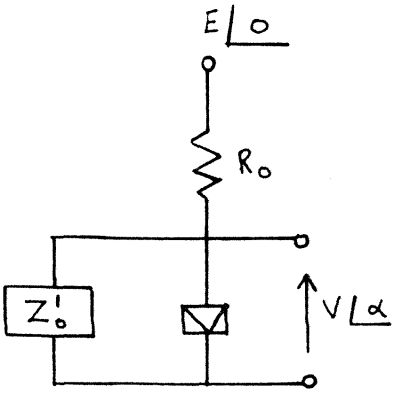


Figure 3.16

The equivalent steady state A. C. load of figure 3.14

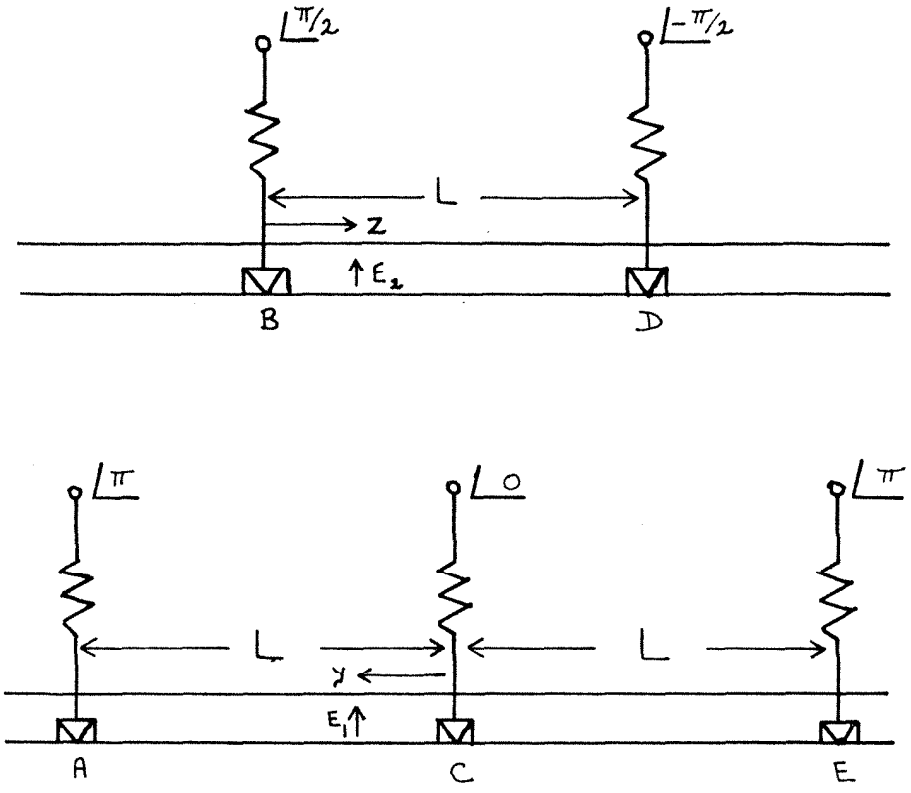


Figure 3.17

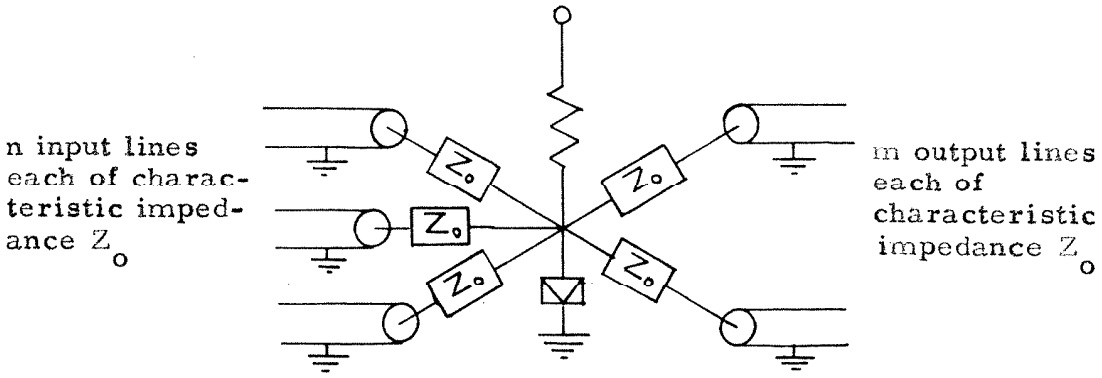


Figure 3.18:- Terminated input-output lines

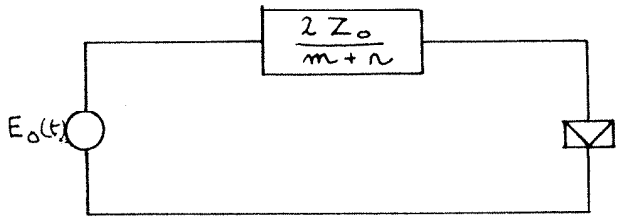


Figure 3.19:- The Thevenin equivalent of figure 3.18

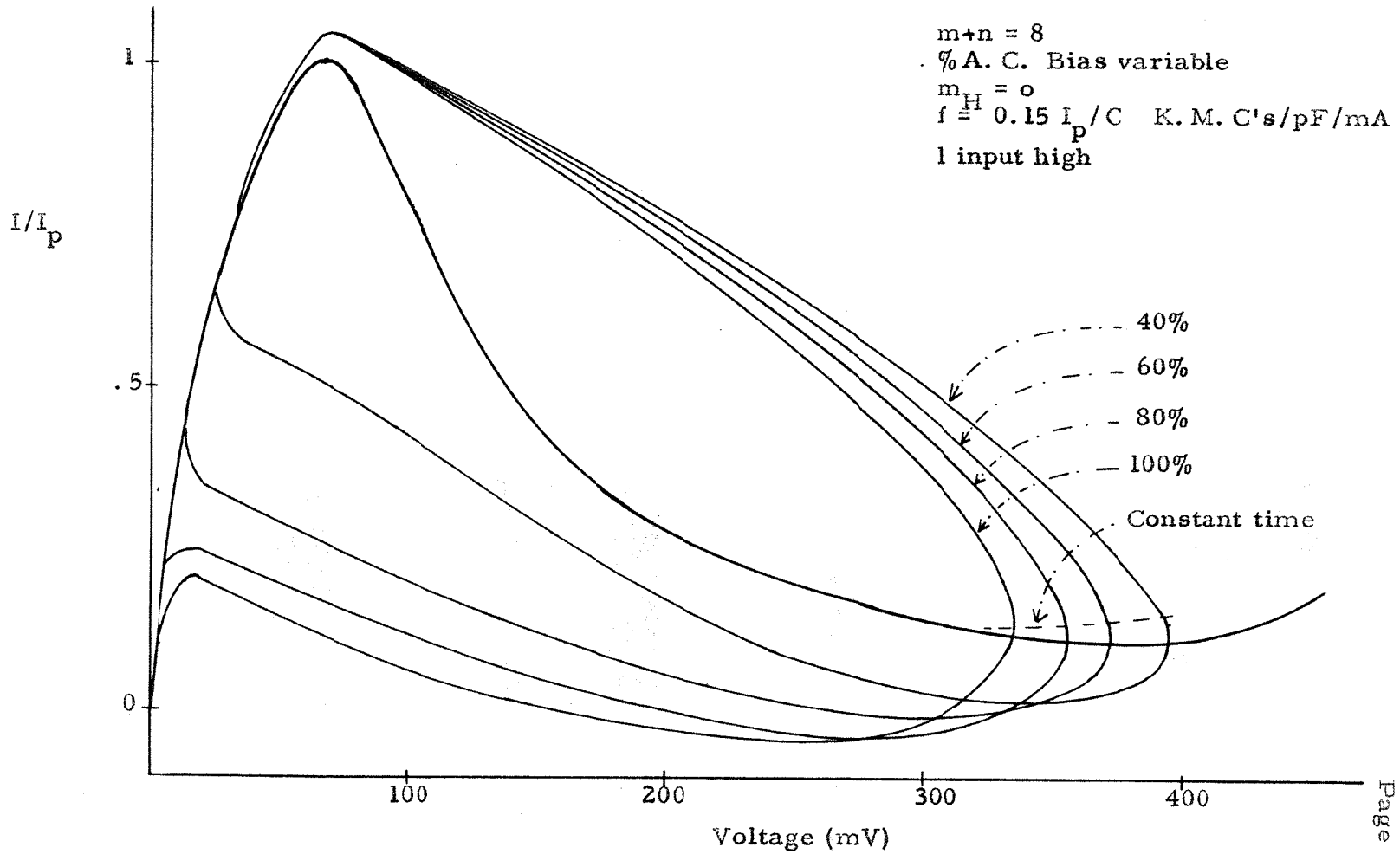


Figure 3.20:- The effect of the % A. C. bias on the dynamic trajectory

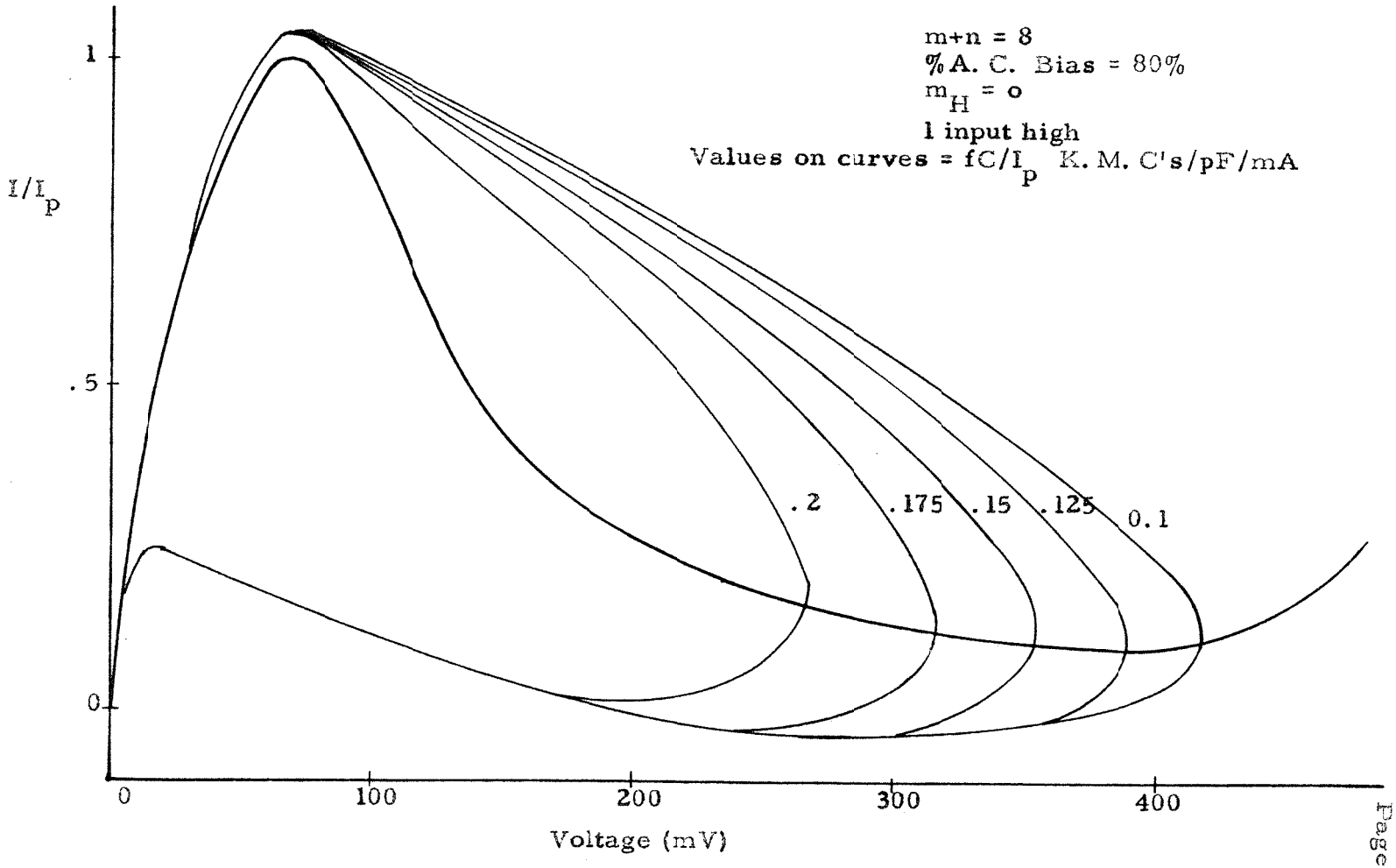


Figure 3.21:- The frequency dependence of the dynamic trajectory

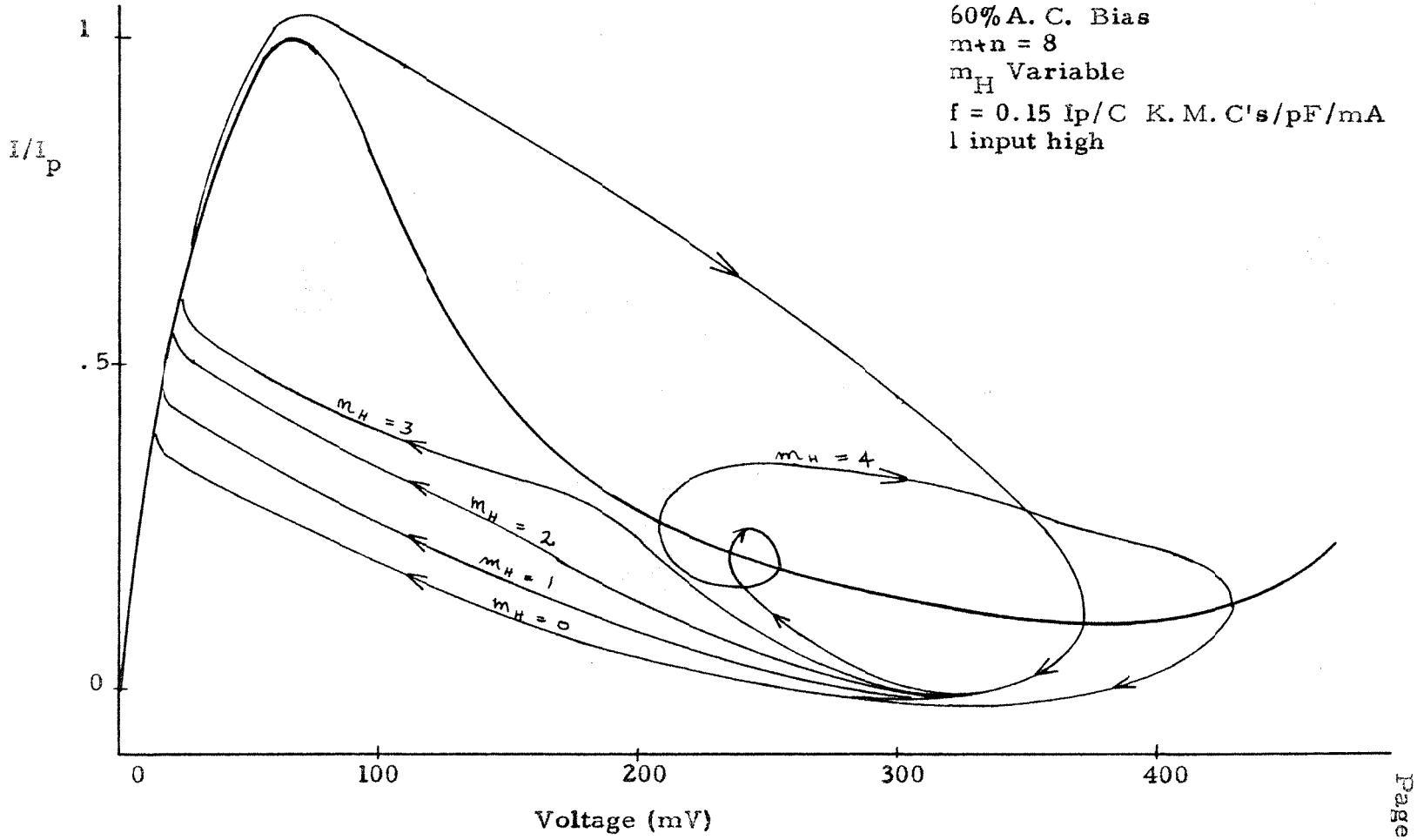


Figure 3.22:- The dependence of the dynamic trajectory on m_H at 60% A. C. bias

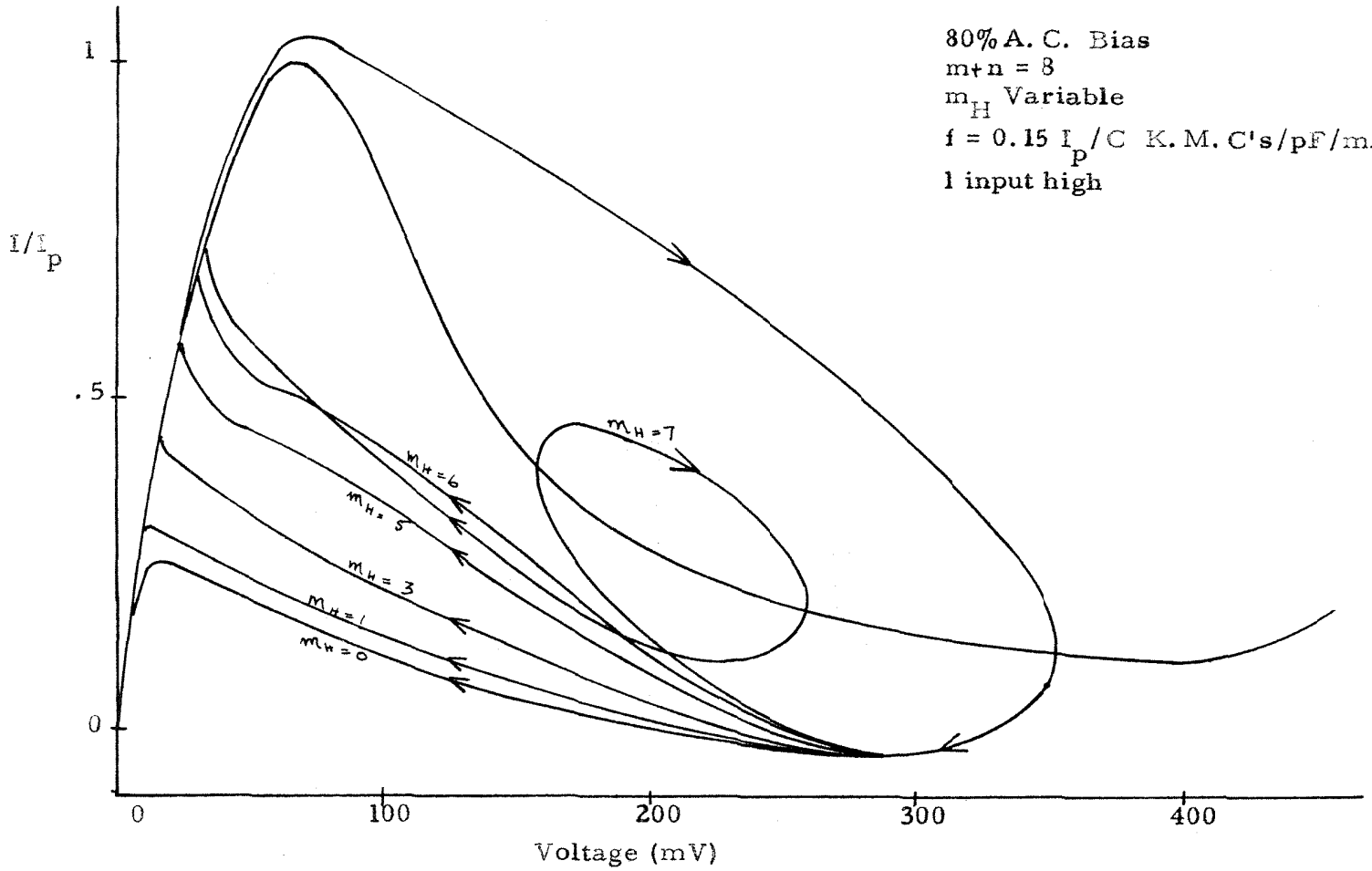


Figure 3.23:- The dependence of the dynamic trajectory on m_H at 80% A. C. bias

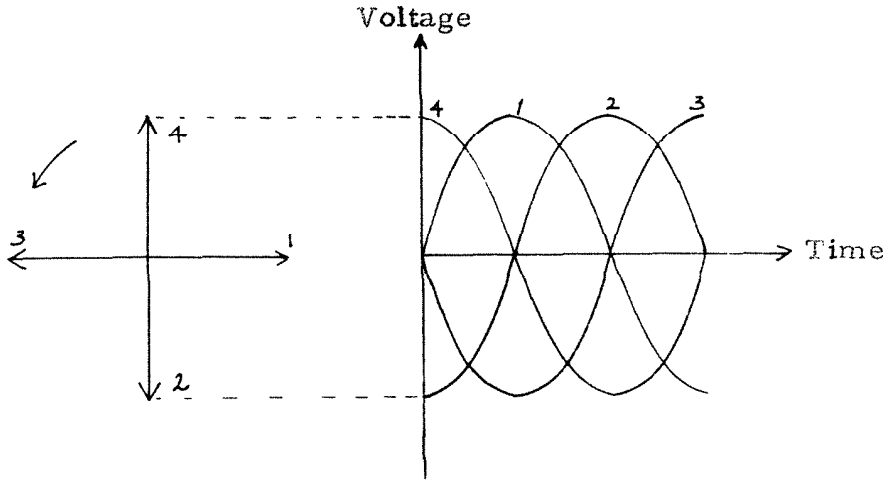


Figure 3.24:- Phase identification

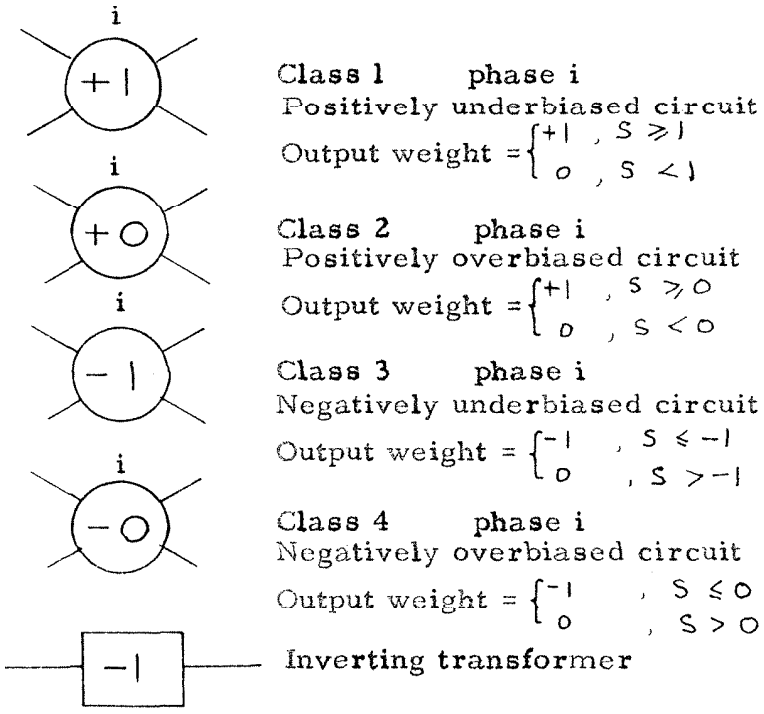


Figure 3.25:- Schematic representation of the basic logic elements and of the inverting transformer

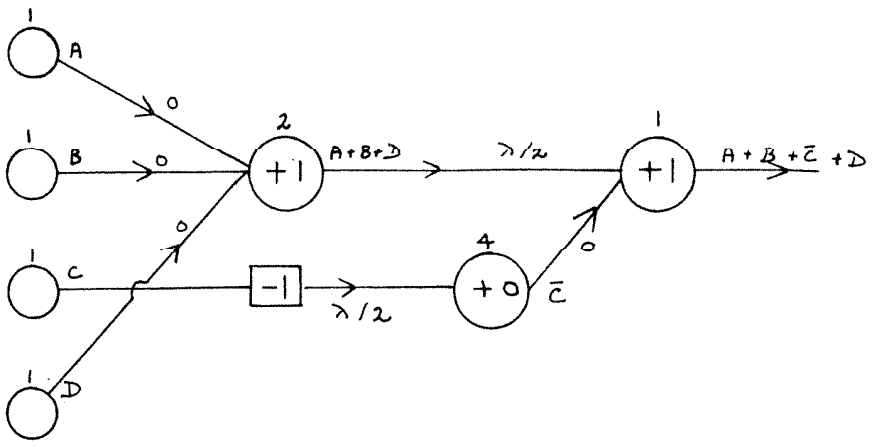


Figure 3.26:- Generation of the Maxterm $A+B+\bar{C}+D$

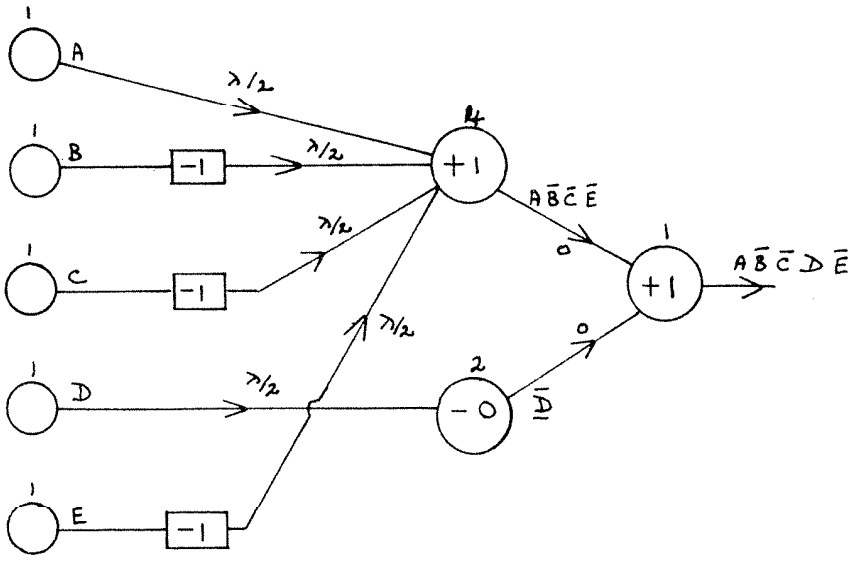
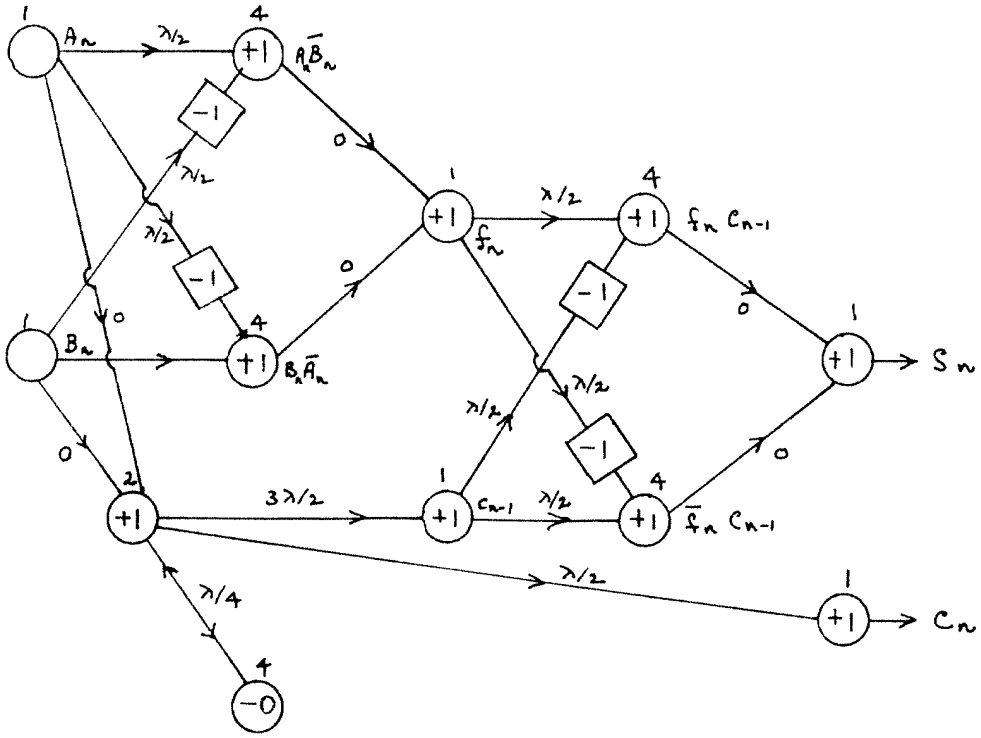


Figure 3.27:- Generation of the Minterm $A\bar{B}\bar{C}D\bar{E}$



Inputs A and B

$f_n = A_n\bar{B}_n + \bar{A}_n B_n$

$C_n = A_n B_n + A_n C_{n-1} + B_n C_{n-1}$

$S_n = f_n \bar{C}_{n-1} + \bar{f}_n C_{n-1}$

Figure 3.28:- The full adder circuit

PART 4
MINIATURE ELECTRICAL DELAY LINES

In present day digital computers electrical delay lines are predominantly employed as a connecting device between various elements and essentially no effort is made to make the delay time of these lines an important factor in controlling the logical operations of the computer, since to do so the lines would be extremely long and expensive. Tunnel diode circuits, on the other hand, have the single predominant advantage of extremely fast switching speeds, thus bringing the length of the delay lines well into the range of practical application.

In Part 3 it was shown that a delay time was sometimes necessary in the device connecting the logic elements of Part 2. Apart from satisfying this necessity electrical transmission lines have the following advantages when used with tunnel diode circuitory:-

(a) Delay lines and especially strip delay lines can be easily integrated into tunnel diode logic circuits.

(b) They can be employed as dynamic storage elements* capable of holding a large number of bits.

(c) Since a delay line can be looped to return to its starting point or near it or can connect distant points the individual tunnel diode circuits can be close together or far apart as is required by the particular application.

(d) When logic elements are connected by electrical delay lines parasitic effects will be very low.

(e) Since it is feasible to use delay lines of small cross sectional area (hence, the name "miniature delay lines") there is a strong probability that extremely low volume circuitory will be obtained.

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* The word dynamic is employed here to indicate that the bits of information move in the storage element as distinct from core or drum storage where the bits remain in a fixed position.

Some miniature delay lines were constructed and tested. The configuration selected consisted of a centre strip copper conductor sandwiched between dilectric sheets with copper ground planes as shown in figure 4.1. This configuration was selected for the following reasons:-

(a) Standard photo etching techniques were available to give the required centre conductor configuration.

(b) It gave a solid construction and the ground planes would provide the necessary isolation.

(c) Compactness could be readily achieved by stacking the layers one on top of another.

In the experimental tests the response of the lines was measured for an input pulse which, except for amplitude, would closely correspond to the output pulse of a tunnel diode when it switches in a return to zero system operating at about 400 megacycles. The attenuation of the pulse amplitude and the pulse spread were of primary concern.

Delay Line No. 1

Using the results of reference (5) this first line was designed to have a characteristic impedance of 50 ohms. This value was selected because the test equipment (oscilloscope, pulse generator, attenuators and connectors) was designed to operate with 50 ohm coaxial transmission lines. Since the velocity of propagation in the miniature delay line is inversely proportional to the square root of the relative permeability of the dilectric and a pulse has components of all frequencies an insulating material whose relative permeability is independent of frequency was required. In addition, the insulating material should also have a low loss tangent and so teflon* (relative permeability 2.1) was selected.

The dimensions and spiral are shown on figures 4.2 and 4.3

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* Trade name for Polytetrafluoroethylene manufactured by DuPont. For details see Reference 6 .

For the photo etching process a ten fold magnified drawing of the spiral was made which was then photographed to give the correct negative size. Standard photo etching techniques were then employed.

In this first delay line the inner end of the spiral was left open circuited and since the dimensions were small the outer end of the spiral and insulation thickness were expanded for connection to a 50 ohm coaxial line. The details are shown on Figs. 4.4 (a), (b), (c) and (d) and photographs of the constructed model are shown in Fig. 4.5. The test circuit and input-output pulses are shown in Fig. 4.6.

A fourier analysis was performed to check the results against those predicted by the existing theory.[5] The comparison was made between the fourier transform of the output and its expected fourier transform. The results are shown on Fig. 4.7 and the agreement is good except in the D. C. region. The reason for the low frequency discrepancy is that the theoretical attenuation (α) in db/unit length is

$$\alpha = \frac{A}{b}\sqrt{f_{KMC}{}^{k}} + \frac{27.3\sqrt{k}\tan\delta}{\lambda} \qquad (4.1)$$

where A depends on $\sqrt{k}$ Z_o, $\tan\delta$ is the loss tangent of the material and f_{KMC} and λ are the frequency in kilogmegacycles and the free space wavelength respectively, implies zero loss at D. C. and so assumes zero D. C. resistance which is not so in this case.

As might be anticipated, the discrepancy becomes pronounced when the skin depth is no longer small in comparison to t/2. An inspection of Figure 4.7 indicates that the error is appreciable for frequencies less than 100 megacycles at which frequency the skin depth is approximately equal to t/4 (i.e. 1/4 mill.). Since equal and opposite D. C. currents can be considered as flowing up and down the line which is terminated in its characteristic impedance the D. C. voltage drop = RI = RV/Z_o where V = input D. C. voltage and R = D. C. resistance of the line (both ways).

In this case R = 10 ohms and Z_o = 50 ohms, giving a 20% drop at D. C. which agrees with the experimental value.

Since pulse attenuation and spread are of primary concern, a

design criterion simpler than the fourier analysis approach was desired. Superposition is permissible and since the input pulses would approximately have the simple form

$$f(t) = \begin{cases} 0 & t < 0 \\ A \sin 2\pi ft & 0 \leq t < \frac{1}{2f} \\ 0 & t \geq \frac{1}{2f} \end{cases}$$

where f is obtained from the idealized input shape the output amplitude can to a high degree of accuracy be obtained from the sinusoidal attenuation at the frequency f provided the pulse spread is not too great. This is illustrated diagrammatically in Fig. 4.8.

In the case of delay line No. 1 Fig. 4.6 shows that this method of prediction of the output amplitude could have been employed. For the dimensions of the delay line equation 4.1 becomes

$$\alpha = 1.66 \sqrt{f_{KMC}} + 132 (\tan \delta) f_{KMC} \text{ db/meter} \qquad (4.1c)$$

From Fig. 4.6 $f_{KMC} \doteq 0.4$ and so $\alpha \doteq 1.05$ db/meter. The length of the line was 2.88 meters (5.76 meters both ways) giving a theoretical attenuation of 6 db or an attenuation factor of 2 which is in exact agreement with the experimental value (Fig. 4.6).

A discrepancy was detected in the delay time. The theoretical value* of 27.8 mμ secs. was about 7% in excess of the measured value of 26 mμ secs. This effect, which occurred in other delay lines, was due to the air gap between the teflon sheets.

The cross coupling between successive turns in the spiral produced no measurable effects so that the dimension a of Fig. 4.2 could apparently have been reduced.

Delay Line No. 2

In Delay Line No. 2 the parameter a of Figure 4.2 was

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* This was computed on the assumption that the transmission velocity was equal to $c/\sqrt{k}$ where c = velocity of light in vacuo and k is the relative permeability of the dielectric.

reduced to 50 mills thus giving greater length per unit area of transmission line. The spiral is shown in Fig. 4.9 and the construction, assembly and test circuit was identical to that for No. 1. Input-output pulses are shown on Fig. 4.10. The pulse spread is more significant than that for delay line No. 1 and the attenuation factor is about 3. The length of the spiral is 4.7 metres (9.4 metres both ways) so that the expected attenuation from eq. 4.1c is 1.05 x 9.4 = 10 db or 3.16. The attenuation obtained is slightly less than that theoretically expected and this discrepancy is clearly the result of overlap between pulses B and C in Fig. 4.8.

The expected delay was 45 mμ secs. and the experimental value was 42 mμsecs. again indicating an error of about 7%.

Delay Line No. 2a

This is identical to No. 2 except that the three outside turns of No. 2 are removed. It was first tested as in No. 2 and then immersed in oil* whose relative permeability was 2.2 and accordingly almost identical to that of teflon. The theoretical delay was 37.5 mμsecs. With the air gap the experimental delay was 35 mμsecs. and when immersed in oil the experimental delay was 37.5 mμsecs. The oscillographs obtained are shown on Fig. 4.11.

Due to the agreement between the theoretical and experimental delays when the delay line was immersed in oil clearly the air gaps must have caused the increase in the velocity of propagation.

Delay Line No. 2b

The 15 inner turns of No. 2a were removed thus making its delay time identical with that of No. 1 so that the effect (if any) of halving the separation distance a between the centre lines of successive spiral turns could be detected. No observable difference was obtained between the output and that of No. 1 indicating that the effect of halving the dimension a gave no measurable change in the cross

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* Wemco - c - Insulating oil

coupling.

The noise in the lines (see figure 4.11) could have been due to cross coupling or line imperfections. Another delay line (No. 3) with both ends accessible was tested so that a distinction could be made between cross coupling noise and other noise.

Delay Line No. 3

The dimensions of this delay line and the plan view of the centre conductor are shown on figure 4.12. The theoretical characteristic impedance of the line was about 30 ohms and was in good agreement with the experimental value. The a/b and a/w ratios were 2.9 and 2 respectively. The schematic circuit layout is shown on figure 4.13 where the end B of the miniature delay line was an open circuit except for the scope probe (2pFarads). The input, reflected and return pulses were detected on channel A and the transmitted pulse (doubled due to the open circuit) was measured on channel B. The return pulse on channel A was virtually unchanged when the scope probe at B was removed thus indicating that the effect of the scope probe at B was negligible. Some of the oscillographs obtained are shown on figures 4.14.

Since the measured output on channel B on figures 4.14a and 4.14b is zero until the pulse arrives cross coupling cannot have occurred because if it did it would have produced a precursor to the pulse. Hence, the noise must be due to line imperfections and the terminations.

As discussed in Part 5 this delay line was later used as a memory device with tunnel diodes connected at both ends.

The Selection of the Dilectric Constant

Since the previous experiments show good agreement with theory it was decided to investigate the variation of the losses per $m\mu$ secs. with the relative permeability of the insulating material. For simplicity the insulating material was assumed lossless (i.e. $\tan \delta = 0$ in eq. 4.1) so that the only losses are copper losses.

The second and third columns of table 4.1 show the value of A as defined in equation 4.1 for two different values of the ratio t/b

(see Fig. 4.2). With tan δ = O equation 4.1 can be rewritten

$$\alpha = \bar{A} \frac{\sqrt{f_{KMC}}}{b} \quad db/m\mu \text{ sec.}$$

where $\bar{A} = \frac{A}{C}$ and C = velocity of light per $m\mu$ sec.

If the dimension b is in metres then $\bar{A} = A/0.3$.

TABLE 4.1

$Z_o\sqrt{k}$	A	
	t/b = 0.01	t/b = 0.1
0	.00039	.00042
20	.00045	.00046
40	.00053	.00051
60	.00060	.00055
80	.00068	.00060
100	.00076	.00066
120	.00087	.00074
140	.00100	.00086
160	.00115	.00103
180	.00140	.00135

Hence, for any value of the characteristic impedance (Z_o) the value of A and accordingly the attenuation per $m\mu$ sec. increases as the dilectric constant increases when b and f_{KMC} are fixed. However, the volume per $m\mu$ sec. is approximately proportional to $1/\sqrt{k}$ and decreases with increasing k. Clearly then there must be a compromise between the losses per $m\mu$ sec. and the volume per $m\mu$ sec. and since tunnel diode circuits have low gain the value of the dilectric constant should be low except in cases where low volume is of primary importance.

If, however, the selection criterion called for minimization of the product of the volume per $m\mu$ sec. and the losses in db/$m\mu$ sec. then the minimum value of $\bar{A}/\sqrt{k}$ is required. For any value of Z_o

and for the two values of t/b in Table 4.1 the values of $A/\sqrt{k}$ are shown in Table 4.2 and with this criterion the optimum value of $\sqrt{k}\ Z_o$ is approximately equal to 140.

TABLE 4.2

b and t in meters

$\sqrt{k}Z_o$	$\frac{10^5}{Z_o}$ $A/\sqrt{k}$	
	t/b = 0.01	t/b = 0.1
0	---	---
20	7.58	7.66
40	4.40	4.25
60	3.33	3.05
80	2.82	2.52
100	2.55	2.22
120	2.42	2.05
140	2.38	2.04
160	2.47	2.14
180	2.56	2.50

It must be also remembered that materials with higher values of the dilectric are more liable to suffer from one or more of the following defects:

(a) High loss tangent

(b) The dilectric constant has a higher % variation with frequency.

(c) Are more expensive and are not available in sheet form.

While the above at least partially justifies the selection of teflon (k = 2.1) as the insulating medium it was decided to build one delay line (No. 4) whose dilectric had a relative permeability of 12.

Delay Line No. 4

The centre conductor employed in this case was the spiral of delay line No. 1 but Stycast (k = 12) was employed as a dilectric. Two

30 mill planar slabs of Stycast were cut from a block of the material and the spiral was etched from a 2 mill copper sheet. The enlarged "tail" of the spiral was removed and a miniature connector* was used to make the connection to the 50 ohm test circuitory. The expected values of the characteristic impedance and delay times were 37.5 ohms and 65 mμ secs. respectively but the experimental values were 54 ohms and 50 mμ secs. The discrepancy was undoubtedly due to air gaps which reduced the effective value of the relative permeability of the dilectric to about 7.1. With this reduced value the losses per mμ sec. were not very different to those for the teflon line (0.2 db/mμ sec. as against 0.23 db/mμ sec. for teflon) and the volume per mμ sec. was about 30% greater. Hence, from volume and loss considerations teflon is superior to K 12 Stycast as an insulating material.

Some test results are shown on Fig. 4.15. The output pulse had a precursor which must have been due to variation of the dilectric constant with frequency since the a/b ratio of 1.6 is only 20% less than that for delay line No. 3 where no cross coupling was detected.

Many constructional difficulties were encountered. The material was not available in laminated form and due to its extreme hardness the cutting task was difficult. Also an unanticipated reaction occurred between one of the photo etching chemicals** and the Stycast.

Summary:-

With an insulating material whose relative permeability (k) is independent of frequency (e.g. teflon) and an input that has the approximate shape of a positive half cycle of a sine wave of frequency f kilomegacycles and is otherwise zero,*** the output amplitude can be accurately predicted using equation 4.1 provided the attenuation is ≤10 db. For greater losses the pulse attenuation will be less than that for the corresponding sine wave and the pulse spread becomes

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* Manufactured by Microdot

** Kodak photo resist developer

*** This input pulse will closely correspond to a tunnel diode output when operating in a "return to zero" system at a frequency of f kilomegacycles.

significant. When this occurs synchronization by means of phase techniques will be no longer possible so that 10 db is about the upper limit of permissible attenuation. Since this value of the attenuation corresponds to a gain of approximately six in a tunnel diode circuit having one terminated input line and one terminated output line, the permissible losses in miniature transmission lines used as storage elements are compatible with the available gain in the tunnel diode circuits.

If the ratios of the characteristic dimensions of the transmission line (i.e. b/w, t/b and a/b of Figure 4.1) always have the same value then except at low frequency the db losses are inversely proportional to b and the volume is proportional to b^2. The net result is accordingly a compromise between volume and the maximum permissible length of the line. For a 10 db loss a delay time of about 42 mμ secs. was obtained with the spiral of Figure 4.9 using teflon as the dilectric. The total volume was about 0.02 cubic inches (volume of enlarged section for connection to coaxial line excluded).

For the delay lines constructed with teflon dilectric the experimental delay was 93% of the theoretical value except in the case where the delay line was immersed in oil with virtually the same relative permeability as teflon. In the latter case very good agreement was obtained between the experimental and theoretical delays. While the discrepancy could be allowed for in the design it should be remembered that this air gap effect will increase with the dilectric constant of the insulator. As an example the measured delay was only 77% of the theoretical value in delay line No. 4 where the relative permeability of the dilectric was 12.

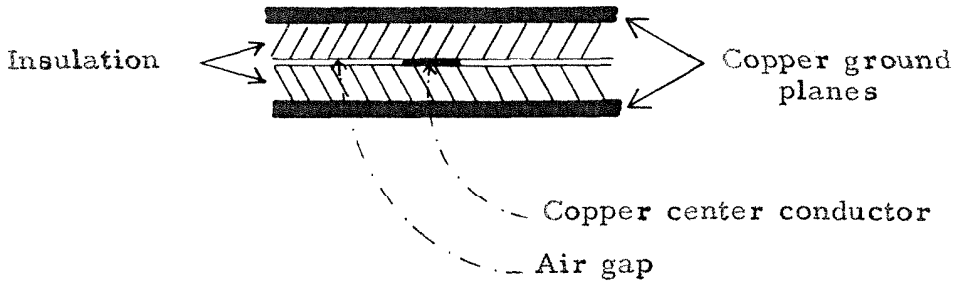
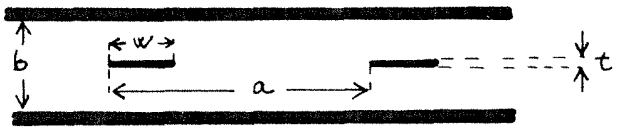


Figure 4. 1:- Delay line configuration



t = 1 mill

w = 16 mills

b = 21 mills

a = 100 mills

Figure 4. 2:- Dimensions of delay line No. 1

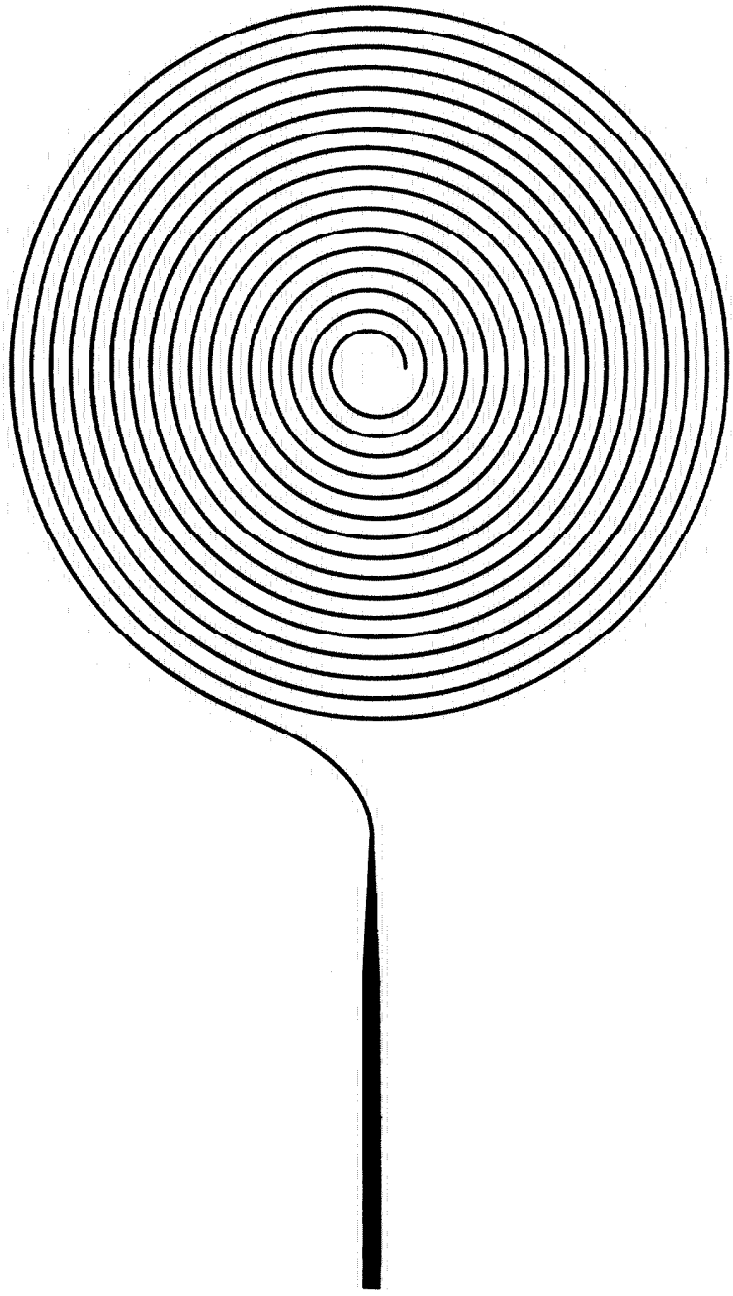


Figure 4.3:- Centre conductor of delay line No. 1

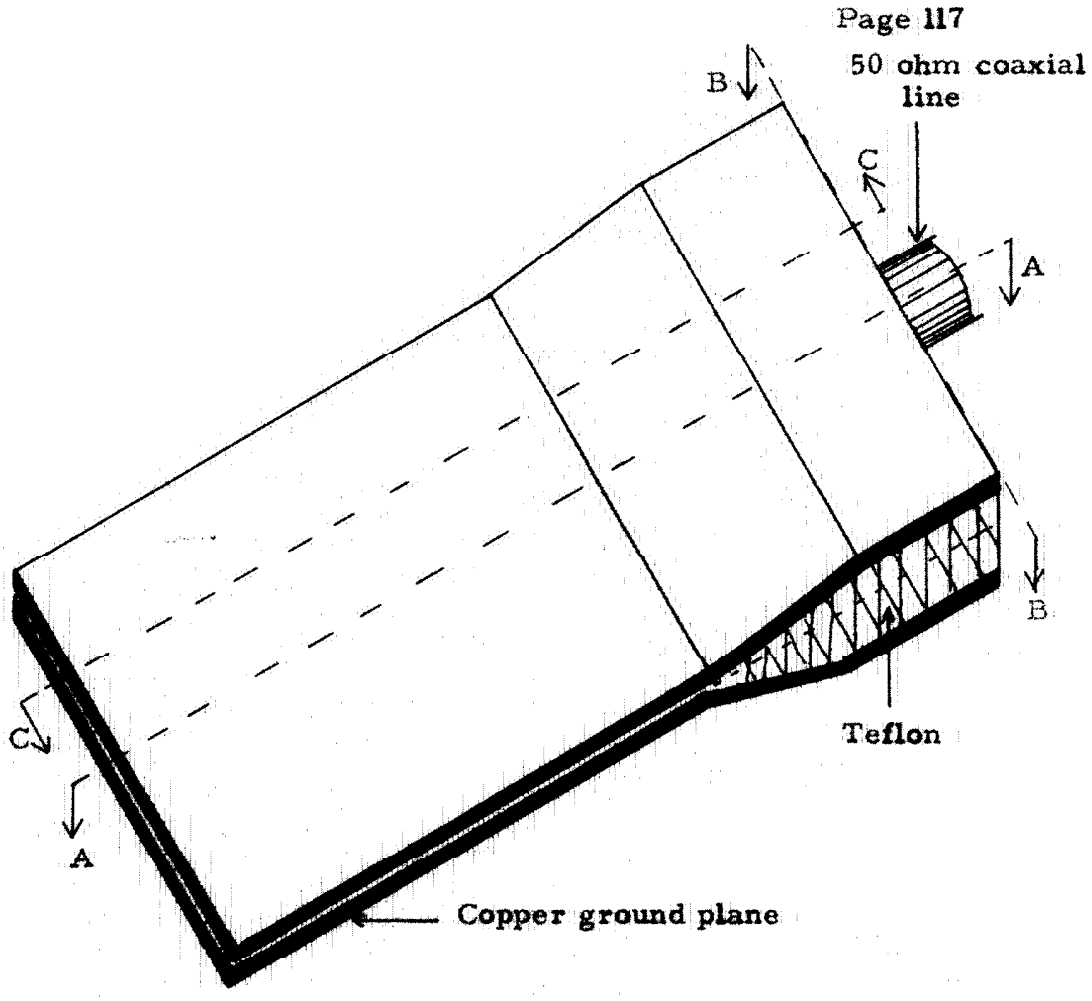


Figure 4. 4a:- Constructional details of spiral delay line

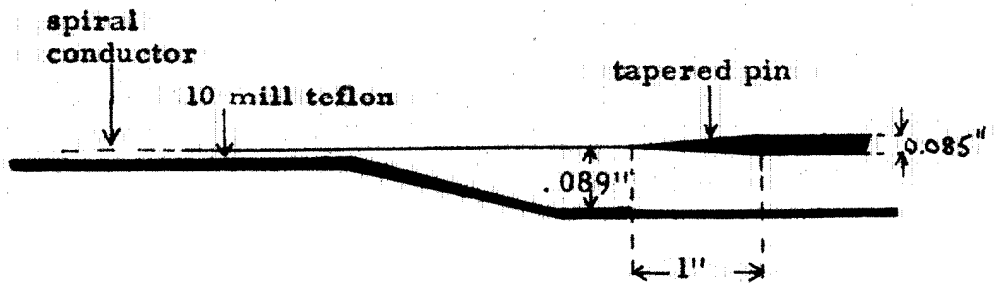


Figure 4. 4b:- Section A-A of figure 4. 4a

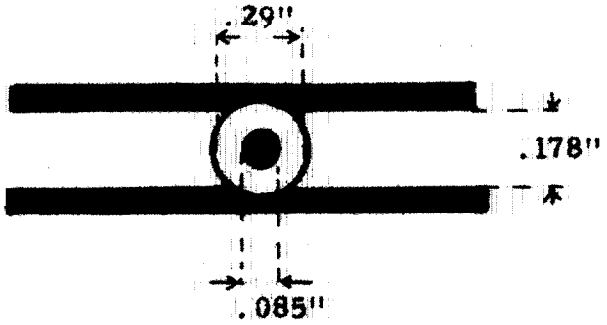


Figure 4.4c:- Section B-B of figure 4.4a

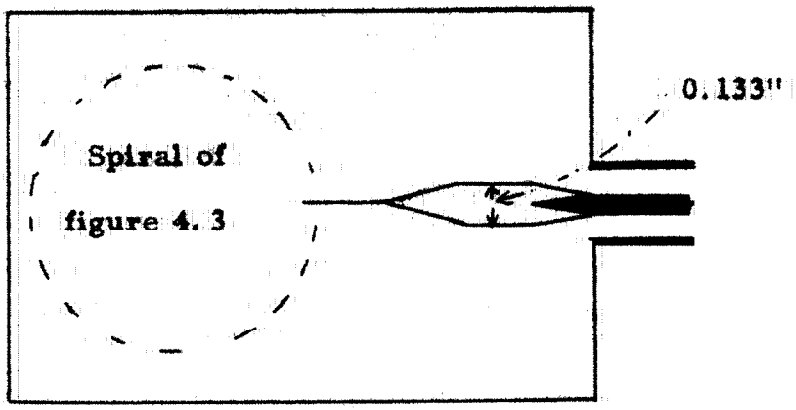


Figure 4.4d:- Section C-C of figure 4.4a

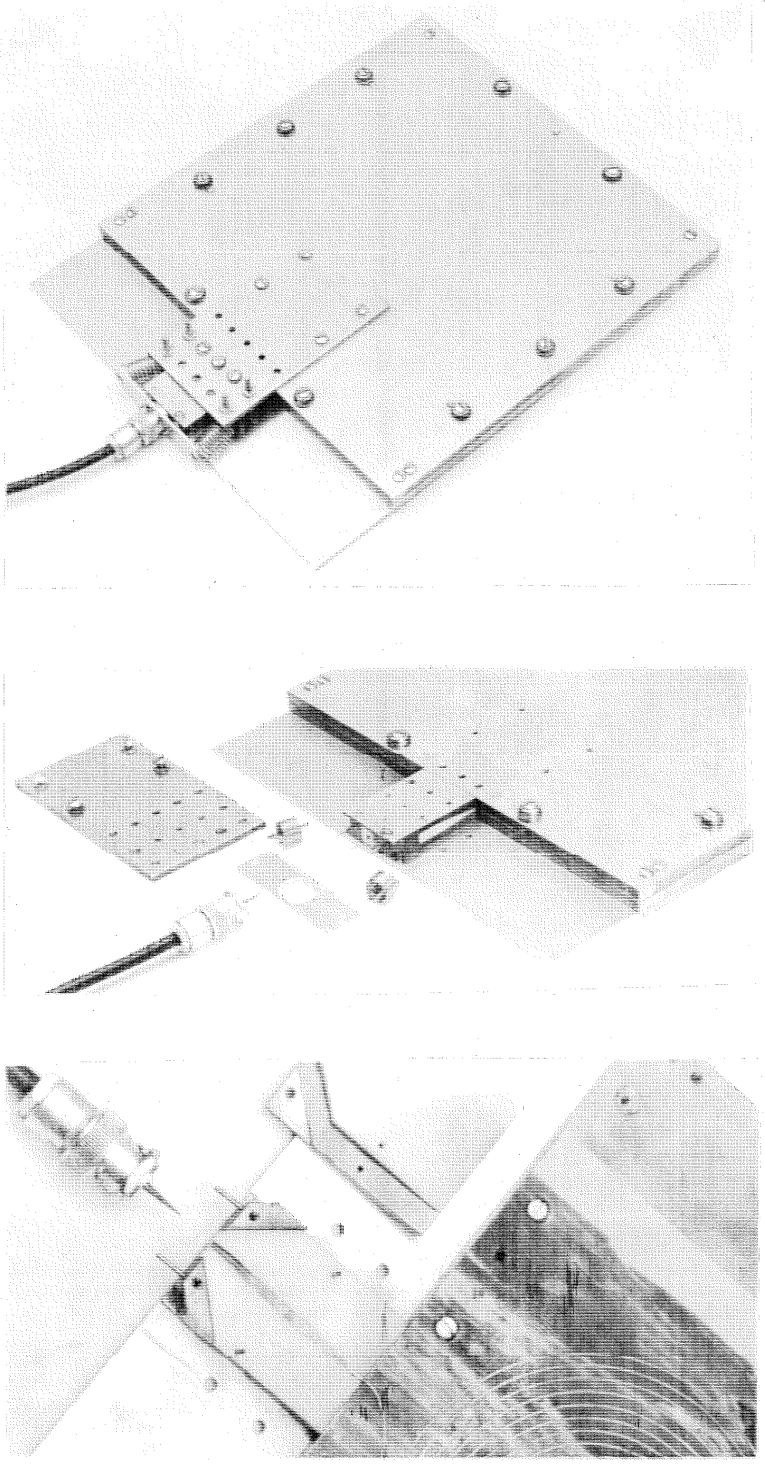
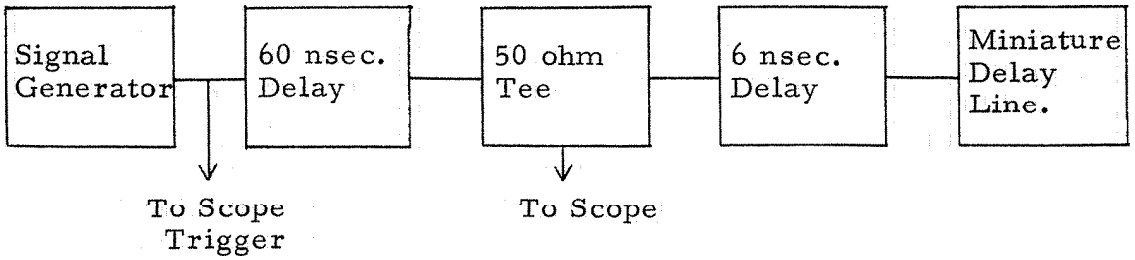
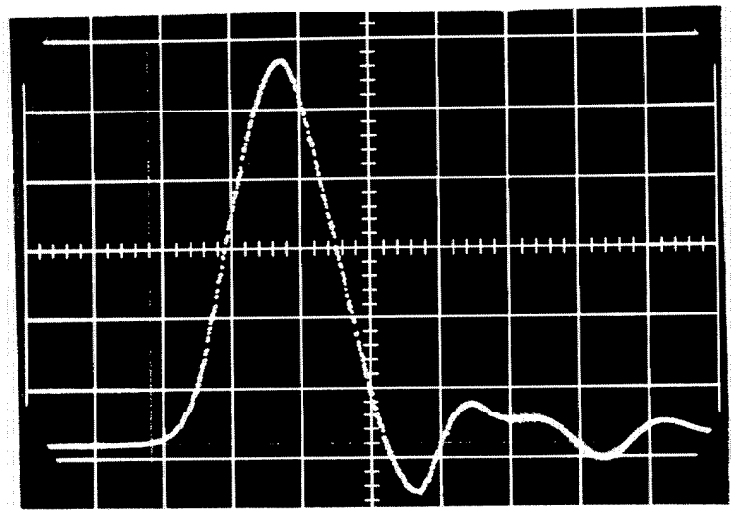


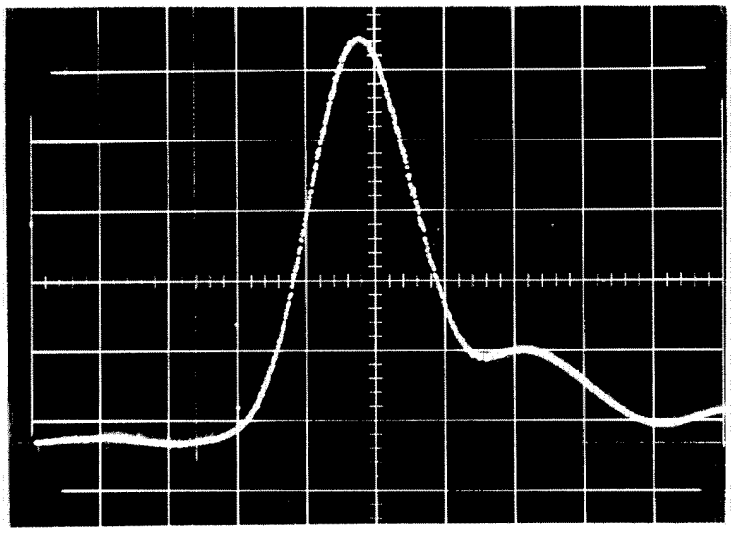
Figure 4.5:- Photographs of delay line No. 1





Input.

Scales:-
Hor. 0.5ns/cm.
Ver. 200mV/cm.



Output.

Scales:-
Hor. 0.5ns/cm.
Ver. 100mV/cm.

Figure 4.6:- Test circuit and input-output pulses of delay line No. 1

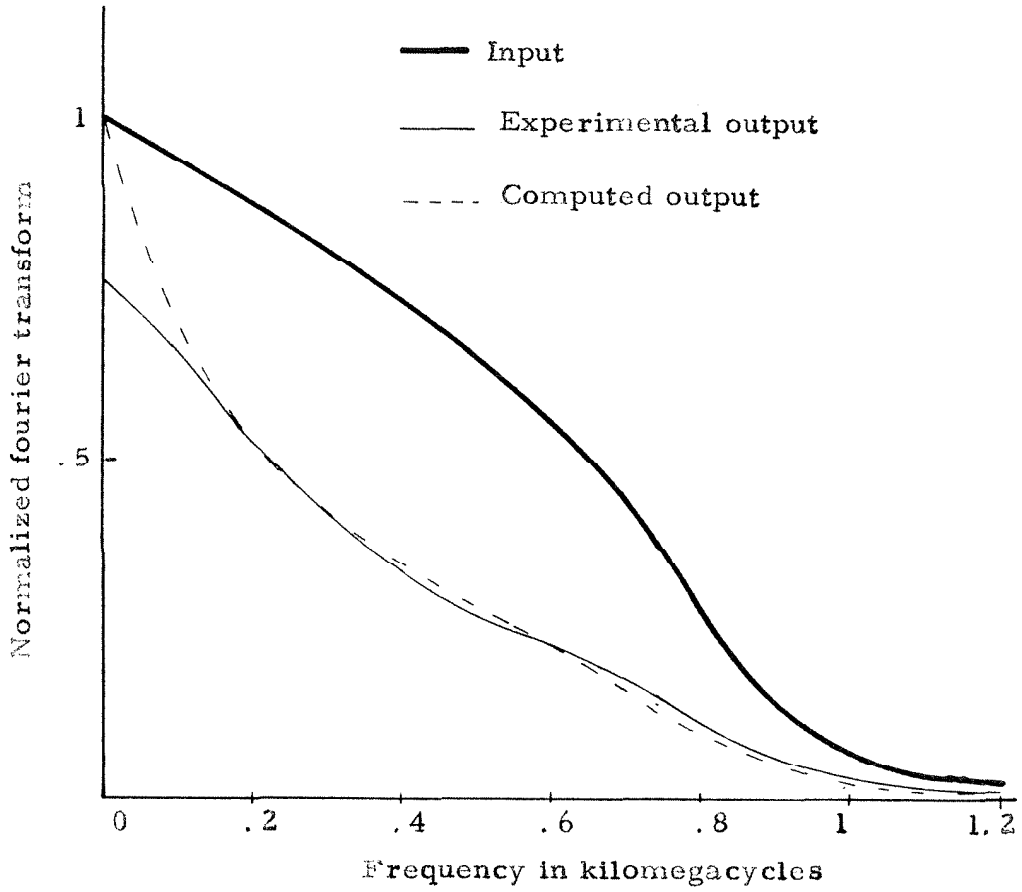


Figure 4.7:- Fourier transforms of input and output pulses for delay line No. 1 and computed fourier transform of the output

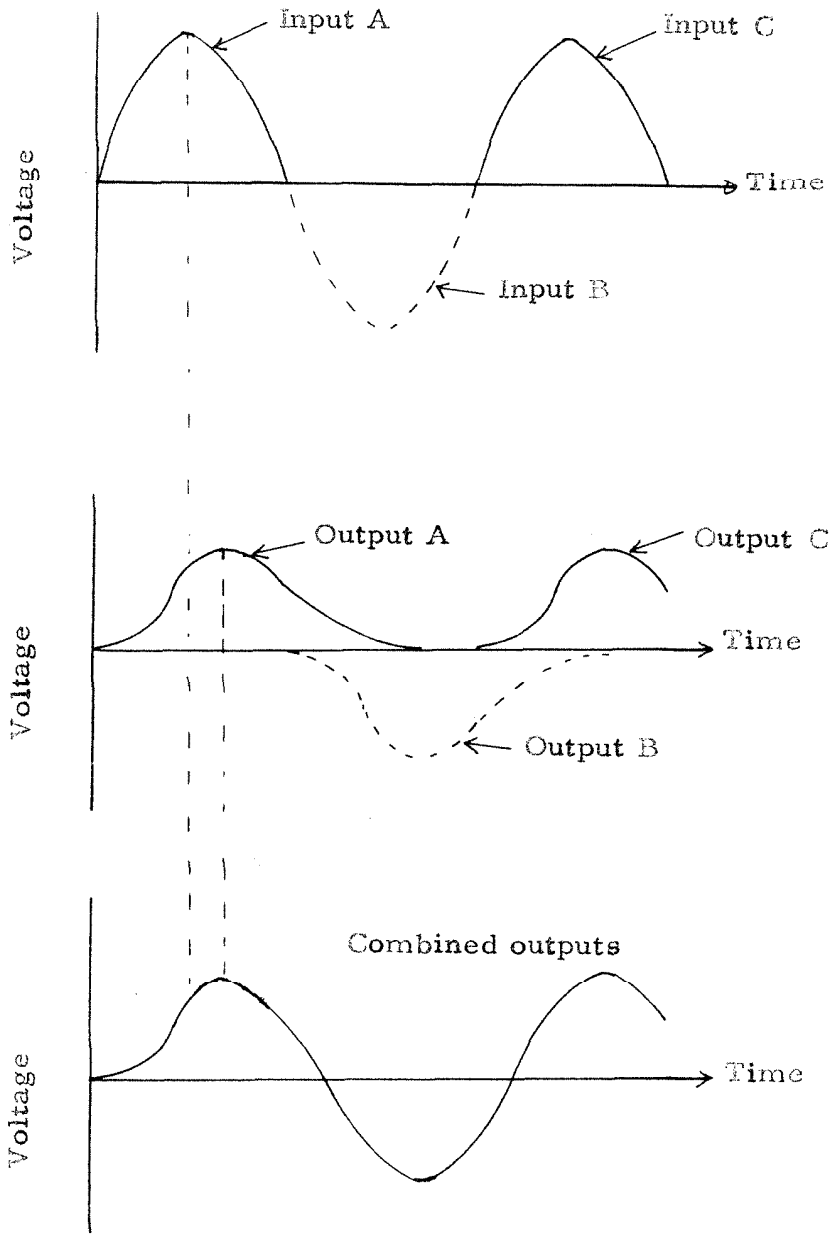


Figure 4.8:- Superposition of pulse responses

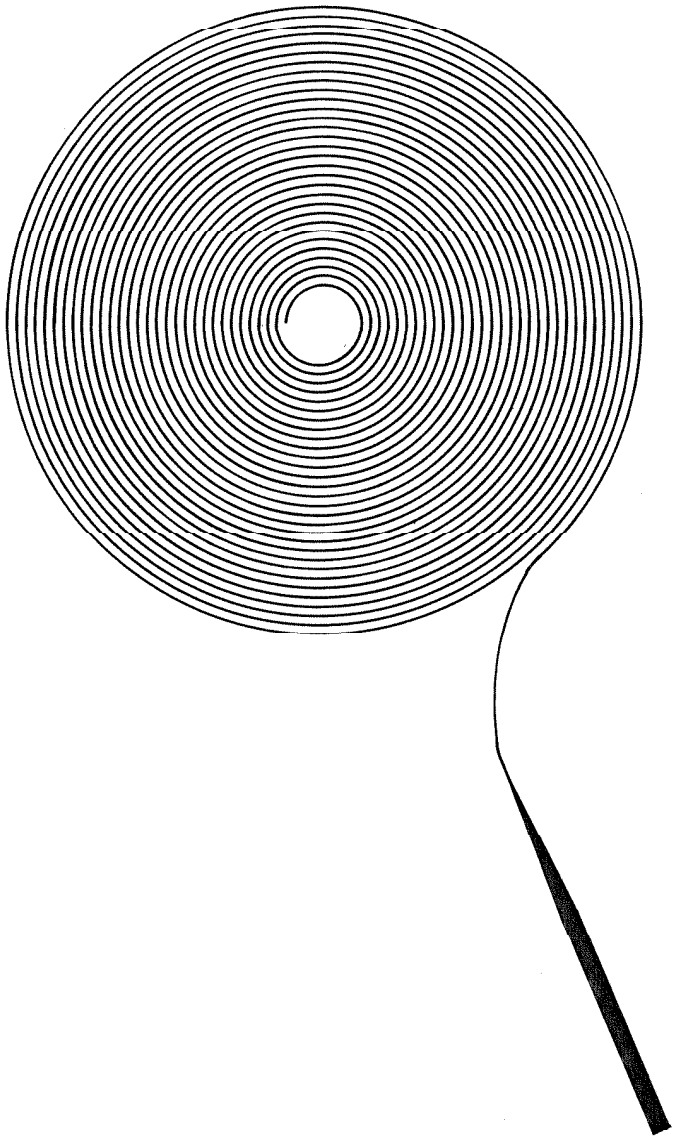
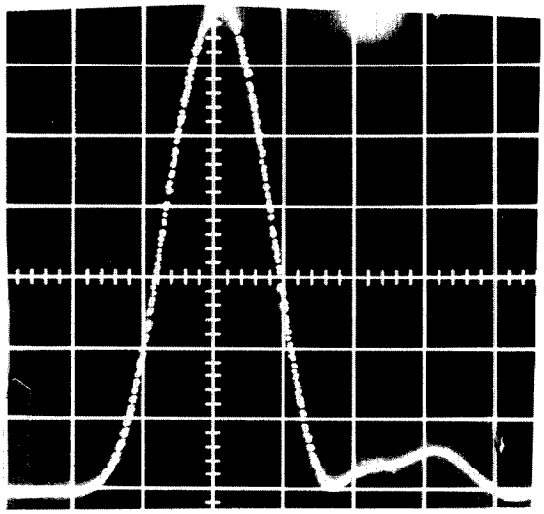
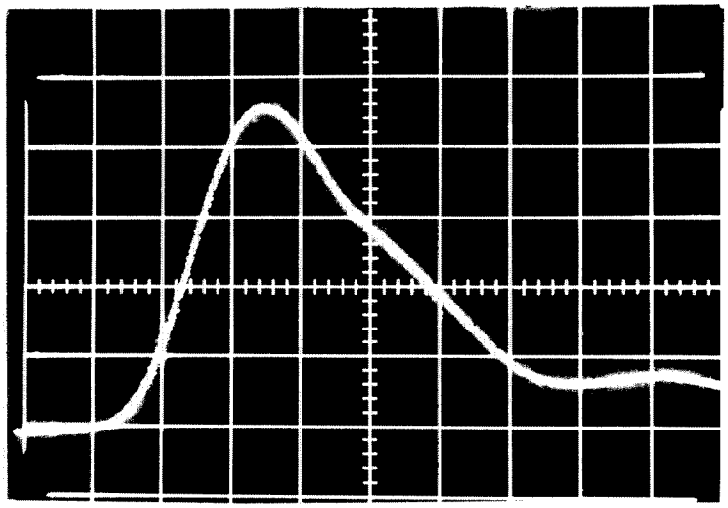


Figure 4.9:- Centre conductor of delay line No. 2

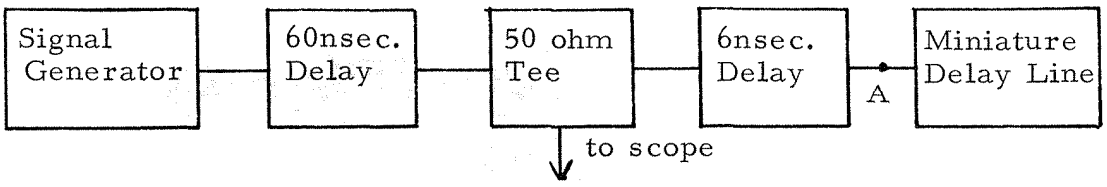


Input.
Scales:- Hor. 0.5ns/cm.
Ver. 100mV/cm.

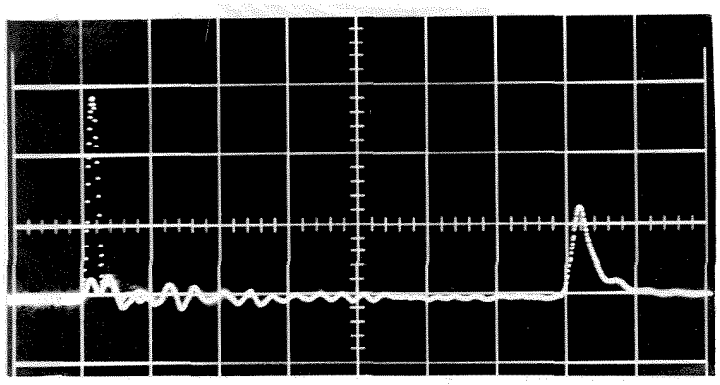


Output.
Scales:- Hor. 0.5ns/cm.
Ver. 50mV/cm.

Figure 4.10:- Input-Output pulses for delay line No. 2

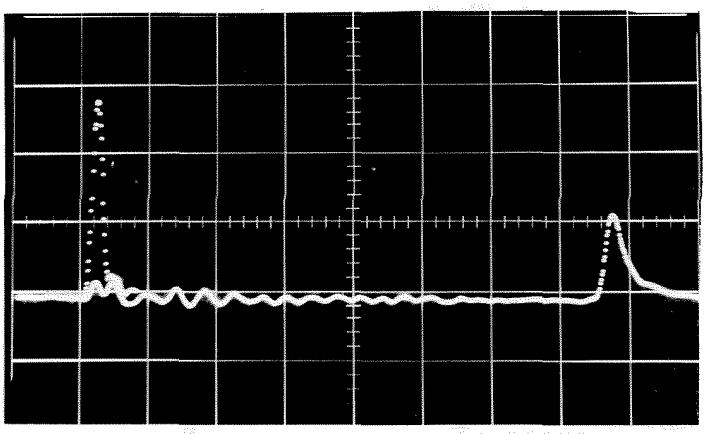


Schematic layout of test circuit



With air gaps.

Input on left obtained by second exposure with open circuit at A



Under oil.

Scales:- Hor. 5ns/cm. Ver. 200mV/cm.

Figure 4.11:- Effect of air gaps on velocity of propagation.

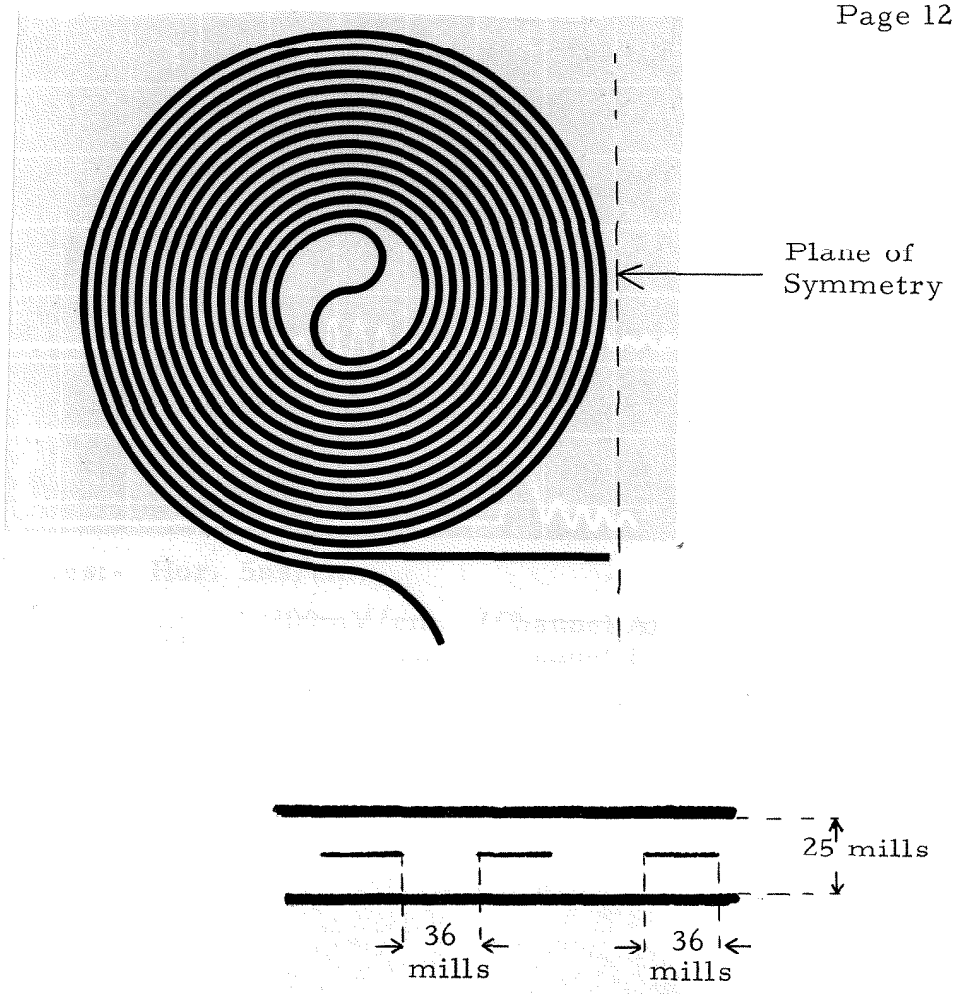


Figure 4.12:- Dimensions of delay line No. 3

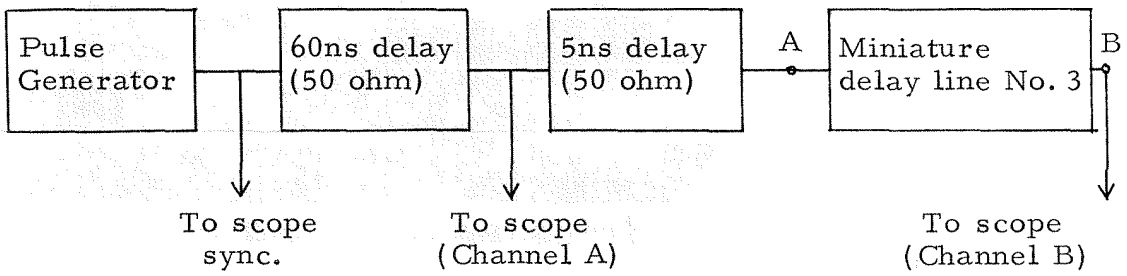
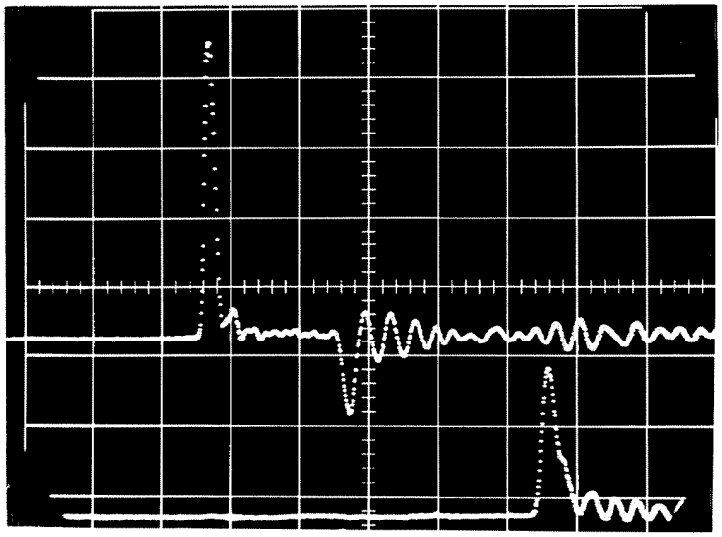


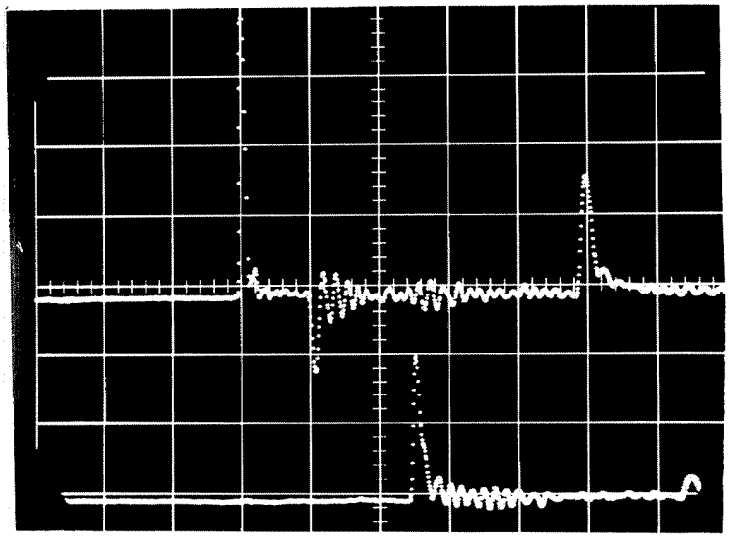
Figure 4.13:- Test circuit for delay line No. 3



Scales:- Hor. 5ns/cm.

Ver. 100mV/cm. (Channel A)
200mV/cm. (Channel B)

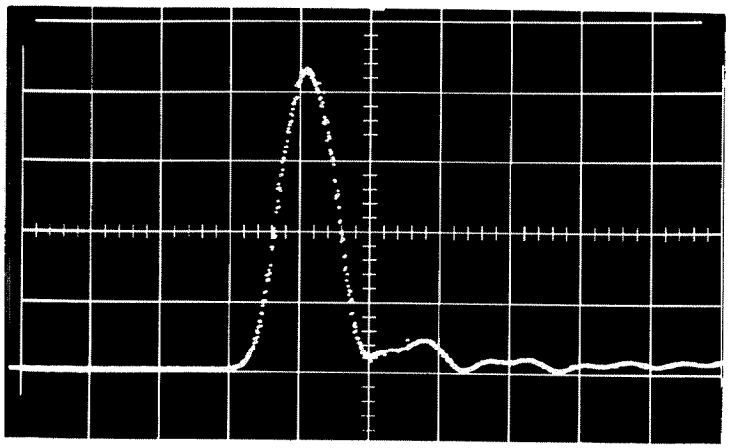
Figure 4.14a:- Pulse response of delay line No. 3



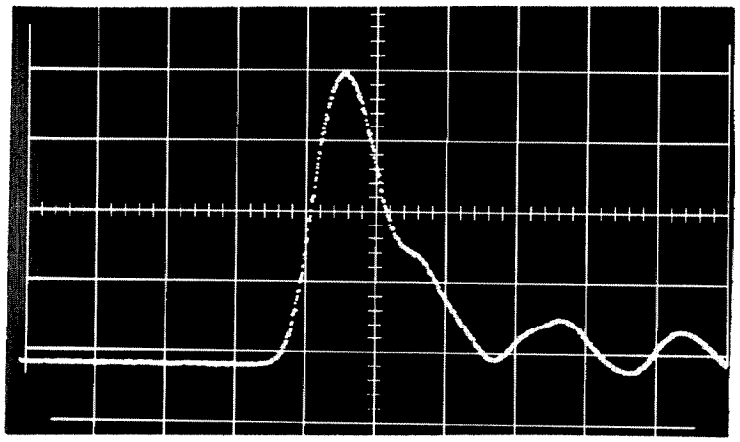
Scales:- Hor. 10ns/cm.

Ver. 100mV/cm. (Channel A)
200mV/cm. (Channel B)

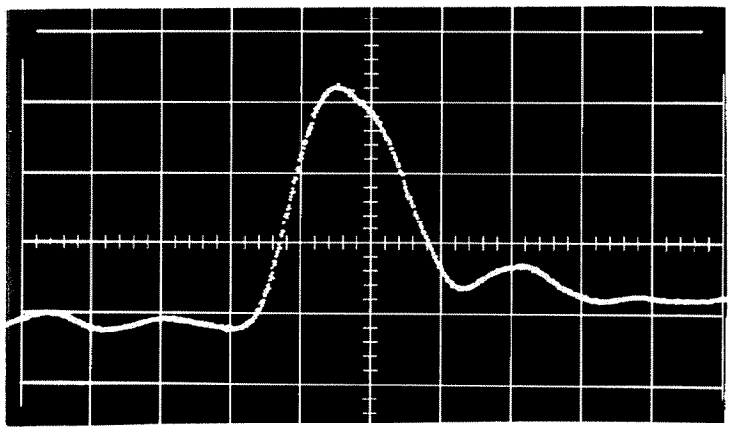
Figure 4.14b:- Pulse response of delay line No. 3



Input pulse (Channel A)



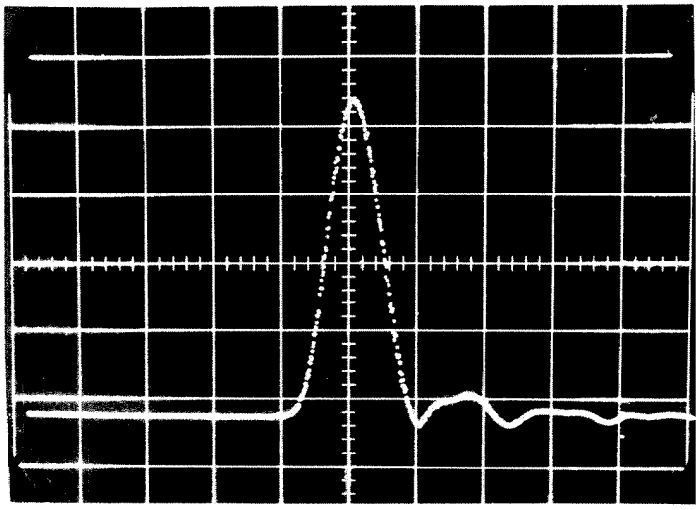
Output pulse (Channel B)



Return pulse from open circuit at B on Figure 4.13 (Channel A)

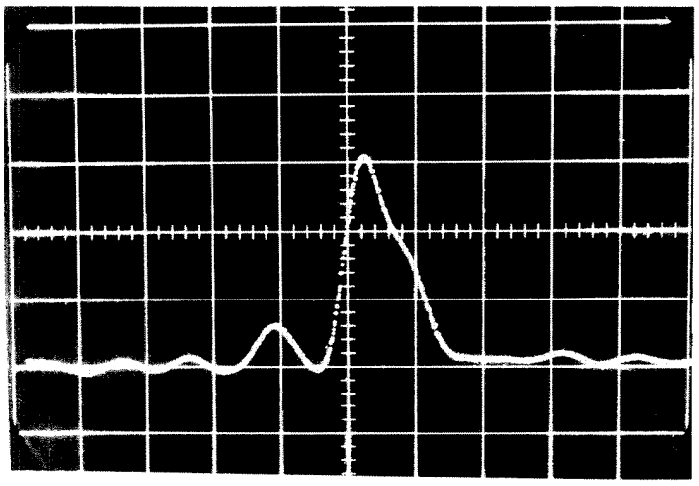
Scales:- Hor. lns/cm. Ver. 100mV/cm. for input and output pulses
50mV/cm. for return pulse

Figure 4.14c:- Pulse response of delay line No. 3



Input

Scales:-
Hor. 1ns/cm.
Ver. 200mV/cm.



Output

Scales:-
Hor. 2ns/cm.
Ver. 100mV/cm.

Figure 4.15:- Pulse response of delay line No. 4

PART 5

REGISTERS AND MEMORY ELEMENTS

A register or memory element incorporating a miniature delay line and two tunnel diodes was constructed and tested. It was decided to use bidirectional coupling* since this simplified the bias problem by permitting the diodes to be driven by the same clock phase. The configuration selected consisted of delay line No. 3 with a tunnel diode** at each end and a power feed through its mid point as illustrated in figure 5.1. The configuration was selected because of its basic simplicity and even though it could only hold 12 bits at about 320 megacycles it is nevertheless an extremely practical storage element. Input-output circuitory was excluded, but this could have been added in accordance with the directional connection rules of Part 3.***

Essentially, the circuitory was maintained as simple as possible primarily because this simple circuit would provide a good check on the validity of the τ parameter when tunnel diode circuits are integrated with miniature delay lines and partially because the required power could be easily supplied.

Using a sine wave and superimposed D. C. bias giving a total % bias of about 97.5% the circuit operated satisfactorily at its synchronous frequencies up to about 500 megacycles. If T is the line delay time (B to A of figure 5.1) and τ_1 is the diode delay (τ_1 = time interval between the maxima of the input and output signals) then the synchronous frequencies are

$$f_n = \frac{n}{2(T+\tau_1)} \qquad n = 2, 4, 6, \ldots$$

---

* See section on bi-directional coupling in Part 3.
** 20 mA, 10pF tunnel diodes were used (R. C. A. type T. D. 182)
*** An example of one possible input-output configuration is later given in this section.

and the number of bits (n) stored in the line increases almost linearly with the synchronous frequency f_n.

At the cut off frequency of 500 megacycles the one way attenuation factor in the line (see figures 4.14a and b) is about 2.0. Also the transmission coefficient (t) at C (figure 5.1) is 0.54 for pulses simultaneously emitted from A and B which then intersect at C and is 0.77 for a pulse emitted from A or B when the other remains low.

Hence the gains G^1 are

(a) $\frac{2}{0.54} = 3.7$ (pulses crossing over at C)

(b) $\frac{2}{0.77} = 2.6$ (pulses which do not cross over at C)

For a gain G^1 of 3.7 and 97.5% bias figure 2.14c predicts a value of τ of about 0.6 since the load line corresponded to a value of E_o of about 600 millivolts. The I_p/C ratio of the tunnel diodes was 2 so that the expected value of f_{max} from equation 3.13a is about 650 megacycles. This value compares reasonably well with the experimental value of 500 megacycles when it is remembered that no allowance was made for the capacity of the scope probes.*

With the operating frequency reduced to about 320 megacycles 12 bits of information could be stored in the line. Figure 5.2 shows some oscillographs of the voltages at the points A and B of figure 5.1 at this frequency. The signal to noise ratio is about 20 db. A close inspection of figure 5.2 will show that the pulses which simultaneously originate from the two diodes have a slightly lower amplitude than a pulse that originates from A (say) when B remains low. This is a consequence of the two possible values of the transmission coefficient (t) at the point C in figure 5.1.

---

* When an allowance is made for the 2pF capacity of the scope probes, and an additional 1pF stray capacitance the theoretical f_{max} is 515 megacycles.

As anticipated the performance of the circuit was critically dependent on the % bias and drift in the d. c. power supply frequently led to failure of the circuit. Also the diodes had to have their peak currents matched to within 1%.

The delay line volume per bits was about 0.06 cubic cms indicating that at best 1.3×10^7 bits of information could be stored in a cubic meter. Even if this number would have to be reduced by a factor of 10 to provide ventillation, space for power supply lines etc., a high packing density will still be obtained. Indeed, when there is no necessity to keep volume and weight "to a minimum" it would be possible to increase the linear dimensions of the delay line by a factor of about 2.7 and hence volume by a factor of 30 thus allowing the above circuit to operate at 320 megacycles and hold 32 bits.

Longer registers can be obtained by constructing a closed chain of OR gates phased to give directional operation as outlined in Part 3. With the four phase system 4n diodes must be employed where n is any integer. The OR gates would have one input and one output and so with terminated lines* and the diodes operating with a current gain of 8 an attenuation factor of 4 is permissible in the delay lines. Even if the attenuation factor is only 3 then with a delay line of the dimensions and length of No. 2 in Part 4 the number of bits stored in the register would be 48n. It is also feasible to include read, write and other logical elements at any of these OR gates. Figure 5.3 shows a possible logic configuration where the contests S of the register will be circulated (B low) or inhibited and the input A read in (B high). The circles indicate the tunnel diode positions and the number at the lower left of each circle is the phase number of that diode. The quantities in the circles are the logical outputs of the diodes. All the diodes are positive under biased except the one

---

* Since multiple reflection problems are not severe in this case it is feasible to operate with non terminated lines which essentially doubles the current gain of the diodes.

whose output is the mirror image of the compliment of the input ($\underline{\bar{A}}$). This latter diode is negative overbiased. On the connecting line the numbers $k_i \lambda$ or $(k_i + 1/2) \lambda$ indicate the length of the connecting lines where k_i is an integer or zero and λ is the wavelength in the dilectric at the synchronous frequency. The total number of bits (N) which can be held in this register is given by the equation

$$N = n(4k_o + 1) + 1 + \sum_{i=1}^{4} k_i$$

Apart from applications to general purpose computers there are equally attractive applications to digital differential analysers and special purpose computers.

Essentially the registers or memory elements are equivalent to drum storage when the peripheral velocity of the drum is equal to the velocity of light divided by the square root of the relative permeability of the insulator in the delay lines.

Finally the tolerances in the line delay times will not lead to cumulative effects since the clock phase will tend to pull the lines into synchronization. A brief investigation with the circuit of figure 5.1 indicated that the line could have a length tolerance of about 1/10 of a wavelength. Consequently if the line length between diodes is nominally 10 wavelengths the permissible tolerance is ±1%.

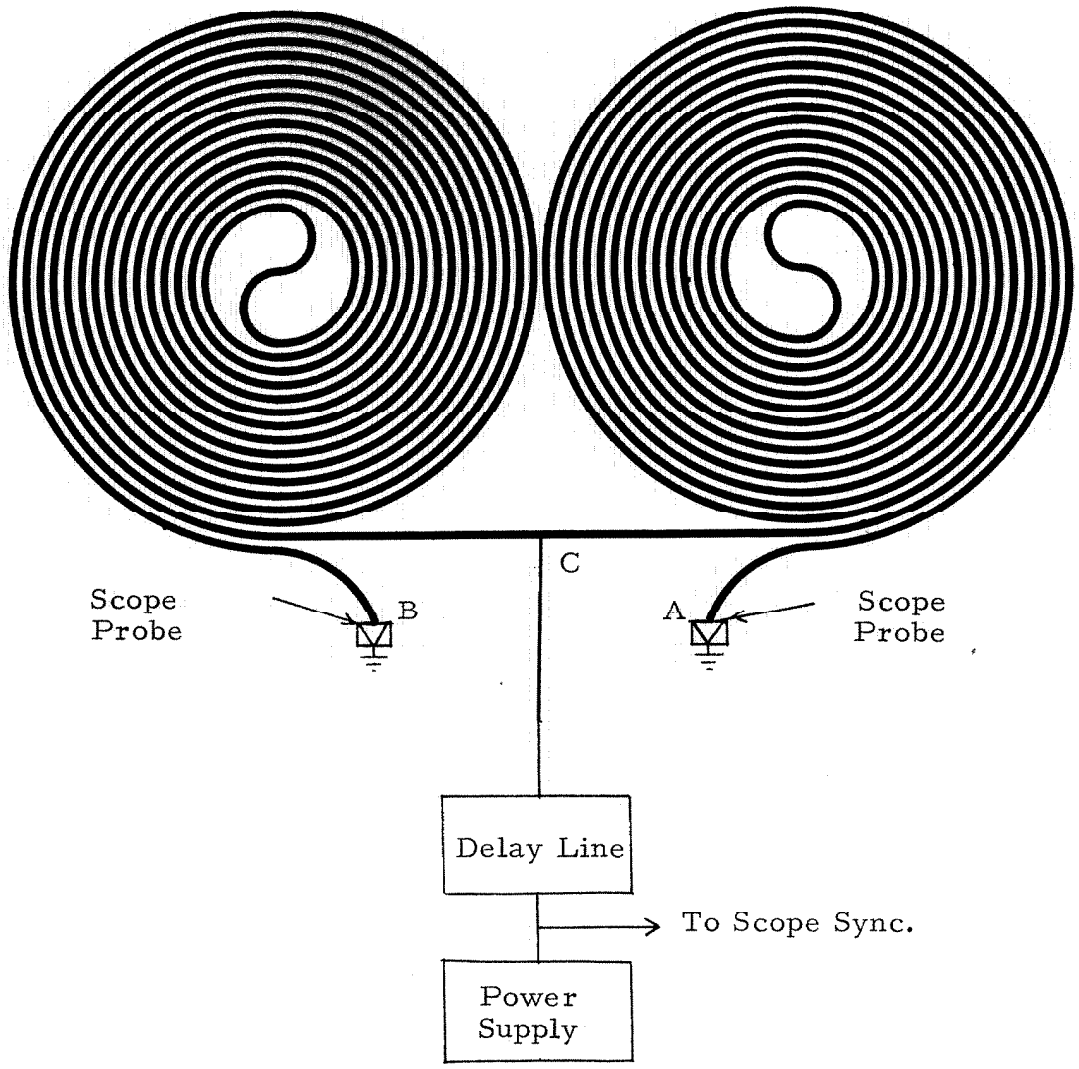
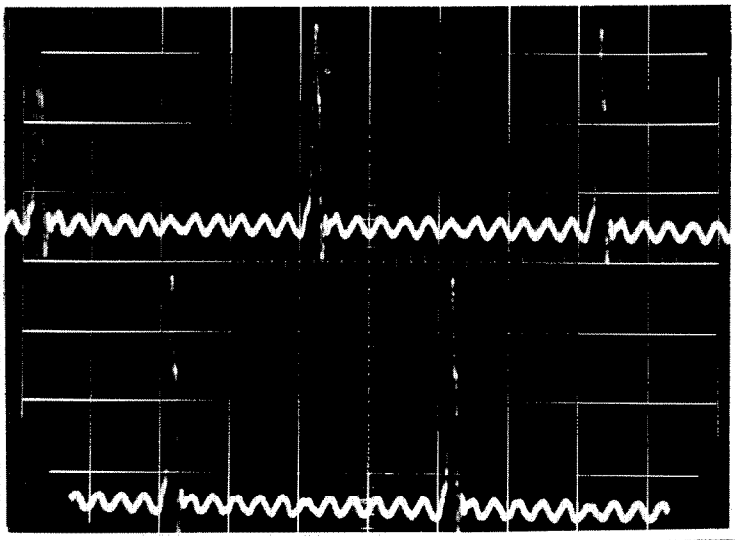
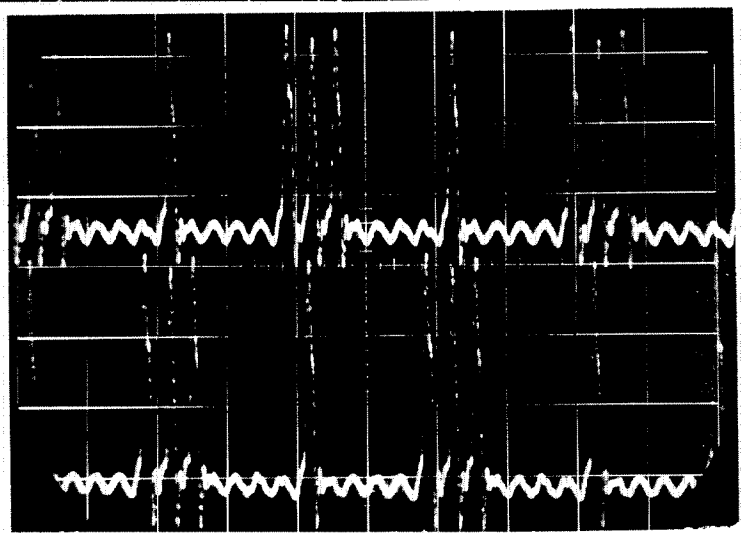


Figure 5.1:- Register or memory device



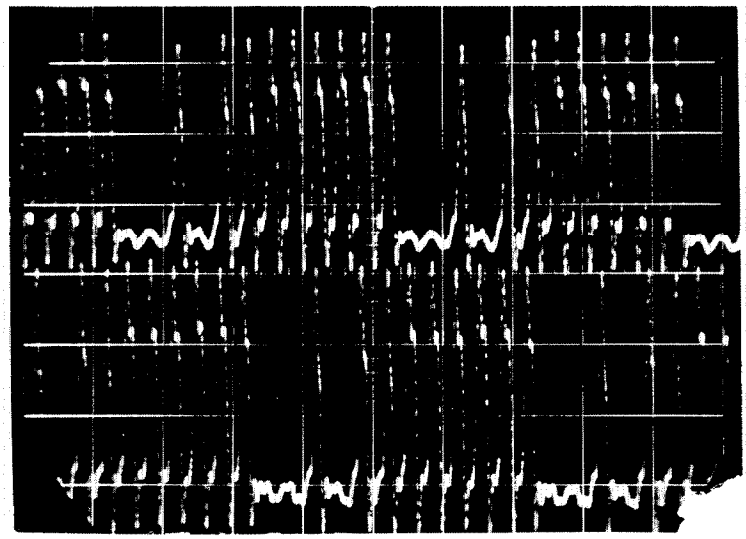
Voltage at A

Voltage at B



Voltage at A

Voltage at B



Voltage at A

Voltage at B

Scales:- Hor. 10ns/cm. Ver. 200mV/cm.

Figure 5.2:- Output voltages at points A and B of Figure 5.1

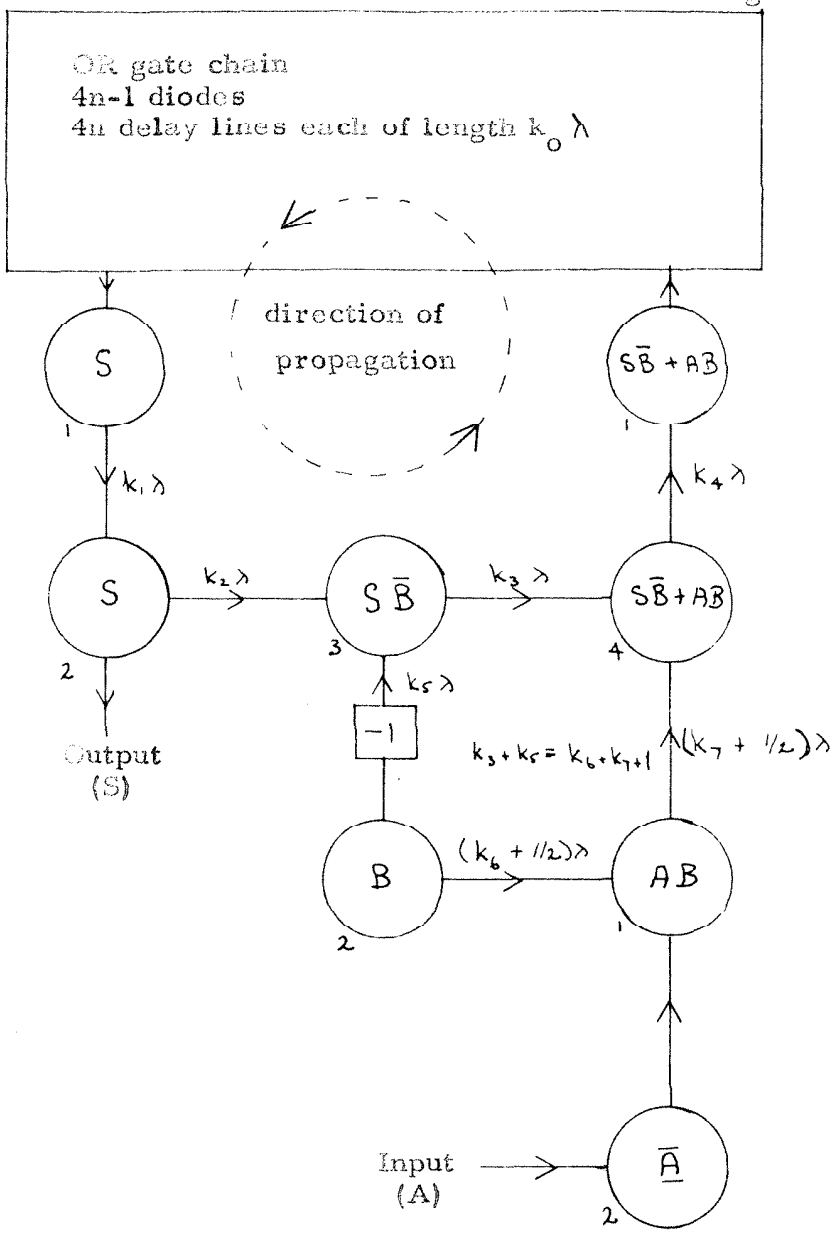


Figure 5.3:- Memory element with input-output logic

PART 6

SUMMARY AND CONCLUSIONS

This thesis can be divided into two major sections. In the first of these the parameters and parasitics which determine the switching speed of tunnel diode circuits were investigated and a non-linear computer analysis technique applicable to these circuits was developed. In the second section a set of logic elements, a method of connecting these elements and a high speed memory device were developed.

The non-linear analysis was performed by means of a special purpose compiler programmed to operate on the Burroughs 220 digital computer. This compiler or circuit analyzer was frequently employed to determine the performance of various circuits and obtain optimum parameter values.

Part 1 of the text deals with parameter measurement and justification of the equivalent electrical circuit of the tunnel diode. In Part 2 the quasi-dimensionless parameter τ was introduced. This parameter is a measure of the switching speed of a tunnel diode and can be employed to predict the maximum permissible repetition rate of a logical circuit. The dependence of τ on % bias, circuit gain, load line and parasitic inductance was investigated and some numerical values were obtained for germanium tunnel diodes. Also in Part 2, a complete set of logical elements (the OR, AND and COMPLEMENT gates) was derived from the single diode circuit. This latter circuit operated extremely well as a logical OR gate but it was not directly applicable as a COMPLEMENT gate and did not have sufficient discrimination to satisfactorily perform the AND operation. A modified AND gate design, which has the electrical sensitivity of the OR gate, and a COMPLEMENT circuit arrangement were obtained by means of mixed bias circuitry and an inverting one to one transformer.

Since the tunnel diode is a two terminal device logical elements must be made directional by some external means. In Part 3 blocking diodes were found to be at best marginally applicable since their capacity removes the major part of the directionality at the high operating frequency. In addition their non-linearity could not be advantageously utilized in the coupling of the mixed bias logic elements of Part 2. A method of direct connection using terminated transmission lines and clock phasing gave good directionality and in addition made the maximum operating frequency dependent only on the tunnel diode parameters and the required circuit gain. Although reasonable fan in and fan out ratios are obtainable this method imposes the necessity of certain connection rules. These connection rules permit a high degree of flexibility but it is probable that complete generality can only be obtained by the introduction of a bit time that is an integral multiple of the A. C. clock period.

In Part 4 compact miniature electrical delay lines were discussed and from their measured pulse response and delay times it was concluded that they could be successfully integrated with the tunnel diode logical elements to give low volume high speed memory devices. The upper limit of permissible attenuation in these delay lines was about 10 db at an operating frequency of 400 megacycles since higher values of the attenuation leads to considerable pulse distortion. One such memory device was constructed (report in Part 5). It had an upper frequency limit of about 500 megacycles and when operating at 320 megacycles it held twelve bits. Its total volume, excluding the volume of the two tunnel diodes, was approximately 0. 75 cubic centimeters.

Many problems will be encountered in the construction of complex systems. The apparent limitations resulting from the connection rules of Part 3 will demand further efforts in the field of logical design. The maintenance of the necessary fine tolerances not only in the tunnel diodes but also in the resistive elements, power supply voltages and the delay times of the electrical transmission lines will require careful quality control or a method of parameter

adjustment in constructed circuits. Input-output buffers must be developed and improvements in measuring or detecting devices are desirable since present day sampling oscilloscopes have a rise time about equal to that of tunnel diode circuits and a probe capacity of two picofarads can cause almost a 20% change in the rise time of a ten picofarad tunnel diode.

Since these difficulties are predominantly of a technological nature there can be little doubt that the high switching speeds of tunnel diode logic circuits and the availibility of a high speed memory device, which can be integrated with the logical elements, would lead to data processing systems with operational speeds a few orders of magnitude greater than that of those presently available.

PARTIAL TABLE OF SYMBOLS

C	Tunnel diode capacity $\left(C = C_v \text{ except in Part 1} \right)$
C_0	Tunnel diode capacity at zero bias
C_B	Blocking diode capacity
C_V	Tunnel diode capacity at the valley voltage
D	The directionality factor
E	The bias voltage
E_0	The Thevenin equivalent bias voltage
f_{KMC}	Frequency in kilomegacycles per second
f_{max}	The maximum permissible value of f_{KMC}
$\bar{f}$	A dimensionless frequency
G	The tunnel diode voltage gain for a single loop (Thevenin equivalent) circuit.
G_L	The minimum value of G at any load line and percentage bias
G_H	The maximum value of G at any load line and value of the percentage bias.
G_{max}	The maximum value of G_H at any value of the percentage bias
G^1	The voltage gain of the circuit
I	The current through the tunnel diode
I_c	The charging current ($I_c = I - I_d$)
I_d	The current which maintains constant voltage across the tunnel diode (Voltage dependent).
I_N	The static value of I when the diode is in the low state
I_p	The tunnel diode peak current
I_v	The tunnel diode valley current
k	Relative permeability

L	Total inductance ($L = L_m + L_s$)
L_m	The lumped inductance of the bias circuit
L_s	Tunnel diode series inductance
m	The number of outputs of a logic circuit (fan out)
mA	Milliamperes
mV	Millivolts
$m\mu H$	Milli-microhenries ($1m\mu H = 10^{-9}$ Henries)
$m\mu$ secs	Milli-microseconds ($1m\mu$ sec $= 10^{-9}$ seconds)
n	The number of inputs to a logic circuit (fan in)
nH	Nanohenries (1 nH $= 10^{-9}$ Henries)
nS	Nanoseconds (1 ns $= 10^{-9}$ seconds)
P	The power dissipation in a logic element in milliwatts
pF	Picofarads (i.e. Farads x 10^{-12})
R	The load line resistance
R_D	The reciprocal of the slope of the tunnel diode V-I characteristic.
R_S	The series resistance of the tunnel diode
R_0	The bias resistor
R_1	The parallel impedance of the input lines in the high state
R_2	The parallel impedance of the outputs
r	Resistance terminating a delay line
T	The clock period
V-I characteristic	Tunnel diode voltage current characteristic when the effects of the series resistance R_s are removed
V	The voltage across the capacitor of the tunnel diode equivalent circuit
V_f	The value of the voltage V when the diode has risen 90% of its total rise

V_N	The static value of V when the diode is in the low state
V_H	The static value of V when the diode is in the high state
V_p	The voltage on the V-I characteristic at $I = I_p$
V_v	The voltage on the V-I characteristic at $I = I_v$
V_g	The energy gap
V_I	The load line voltage corresponding to the current I
Z_0	The characteristic impedance of the transmission lines connecting the logic elements
Z	The characteristic impedance of the power supply lines
X	Attenuation factor in the transmission lines connecting the logic elements
τ	Dimensionless zero to 90% rise time parameter
ω	Angular frequency
% Bias	The % Bias is defined as $100\ I_N/I_p$.

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APPENDIX I

PROGRAM TO COMPUTE THE TRANSIENTS IN ELECTRICAL NETWORKS USING THE BURROUGHS 220 COMPUTER

by

Patrick G. O'Regan

ABSTRACT

The program will compute the transients in practically all linear networks provided an independent set of loop currents exists such that at most only two currents flow through any element and, if there are two, these currents are flowing in opposite directions. One type of nonlinear element is permitted and that is a nonlinear resistance in parallel with a linear capacitor.

TABLE OF CONTENTS

ABBREVIATIONS

h or H	The integration interval (also called the time interval or step interval)
n	The number of independent current loops in the circuit under consideration
m	The number of co-ordinate points taken on the V-I characteristic of a diode
q	The number of different (non-identical characteristics) diodes in the circuit
s	The number of integration intervals between printouts. [s is stored in 0475 (Relative).]

INTRODUCTION

This program is primarily intended to solve transients in electrical circuits in which diodes, and in particular tunnel diodes, are present but is equally efficient in the case of linear R-L-C networks. Solution is obtained by means of step-by-step integration using the fourth order Runge-Kutta method.

PROGRAM LIMITATIONS

1. The electrical circuit must be such that there is an independent set of loop currents with one or two, but no more than two, currents through any element, and if there are two, these must be flowing in opposite directions. All planar circuits and many non-planar circuits meet this requirement.

2. The loops must be selected so that the following types of loops are prohibited:

   a. k inductive loops (i. e., an inductance in each loop) where the number of inductors in these loops is less than k. $k = 2, 3, 4, 5, \ldots, n$.

   b. k noninductive loops where the number of resistors in these loops is less than k. $k = 2, 3, 4, 5, \ldots, n$.

3. All the driving sources must be voltages, but current sources may be simulated by means of a high voltage source with a high internal resistance. At present, the voltage sources are limited to step or ramp functions but may be extended by means of a subprogram.

4. The maximum number of different diodes (nonlinear resistance in parallel with a linear capacitor) is limited to 7, and each loop containing a diode must have an inductance in it.

5. The maximum number of loops is about 25 but is slightly dependent on the input statement. If n is the number of loops, q is the number of non-identical diodes and I is the length of the input statement, then the following inequality must be satisfied:

$$I + 4n^2 + 15n + 1374 + 40q \leq 5000 \quad \text{(core storage capacity)} .$$

MATHEMATICAL DISCOURSE

Assume that n independent current loops exist for the circuit under consideration and all the conditions imposed in the "Program Limitations" section are satisfied. Using Kirchhoff's second law, the dynamic equations of the circuit may be written in the following matrix form:

$$\left[L \right] \left(\frac{dI}{dt} \right) + \left[R \right] \ (I) \ + (\Sigma V_c) \ = \ (E) \qquad (1)$$

where

(1) $\left[L \right]$ is the inductance matrix.

(2) $\left[R \right]$ is the resistance matrix.

(3) (ΣV_c) is a vector whose i^{th} component is the sum of the capacitor voltages around the i^{th} loop when traversed in the opposite direction to the assumed direction of flow of the i^{th} current.

(4) (E) is the applied voltage vector whose i^{th} component is the applied voltage in the i^{th} loop when traversed in the assumed direction of flow of the i^{th} current.

(5) $\left(\frac{dI}{dt} \right)$ is a vector whose i^{th} element is the rate of change of the i^{th} loop current with time.

(6) (I) is the current vector whose i^{th} element is the i^{th} loop current.

The Inductance and Resistance Matrices

The inductance matrix takes the following form:

$$\begin{bmatrix} L_{00} & -L_{01} & & & -L_{0,\,(n-1)} \\ -L_{10} & L_{11} & & & \\ & & L_{ii} & -L_{ij} & \\ & & -L_{ji} & L_{jj} & \\ & & & & L_{(n-1),\,(n-1)} \end{bmatrix}$$

where L_{ii} is the sum of the inductances in the i^{th} loop and L_{ij} is the inductance common to the i^{th} and j^{th} loops. $(L_{ij} = L_{ji})$

The resistance matrix is to resistance as the inductance matrix is to inductance.

Solution of the Dynamic Equations

Assume, for the purpose of explanation only, that the inductance matrix is non-singular. Equation (1) may then be written:

$$\left(\frac{dI}{dt}\right) = \left[L\right]^{-1}\left\{-\left[R\right](I) - (\Sigma V_c) + (E)\right\} \qquad (2)$$

and so knowing the initial conditions $\left(\frac{dI}{dt}\right)$ may be obtained. The Runge-Kutta procedure can be employed to obtain $(I)_{t+h}$ once $(I)_t$ is known where h is the step increment of time. The only difference between (2) and the customary type of equation is that there is the (ΣV_c) vector appearing in (2) which is itself time dependent.

Suppose then that $\left(\frac{dI}{dt}\right)$ can be computed from (2) at time t. Using the Runge-Kutta procedure $\left(\frac{dI}{dt}\right)$ must be computed four times in all at times $T_{r.k.}$ where

$$T_{r.k.} = t$$

$$T_{r.k.} = t + \frac{h}{2} \quad \text{(twice)}$$

and

$$T_{r.k.} = t + h$$

before $(I)_{t+h}$ is computed. Thus (ΣV_c) is required at $T_{r.k.}$ but only known at time t. The approximation made is that

$$(\Sigma V_c)_{T_{r.k.}} = (\Sigma V_c)_t + (T_{r.k.} - t)\left(\frac{d\Sigma V_c}{dt}\right)_t ,$$

and so Equation (2) becomes

$$\left(\frac{dI}{dt}\right)_{T_{r.k.}} = \left[L\right]^{-1}\left\{-\left[R\right](I) - (\Sigma V_c)_t - (T_{r.k.} - t)\left(\frac{d(\Sigma V_c)}{dt}\right)_t + (E)_{T_{r.k.}}\right\}$$

(3)

The vector $\left(\frac{d(\Sigma V_c)}{dt}\right)_t$ may be computed at time t since the loop currents are known at t. The i^{th} element of $\frac{d(\Sigma V_c)}{dt}$ is

$$\frac{I_i - I'_i}{C_{ii}} + \sum_{\substack{j \\ j \neq i}} \frac{I_i - I_j - I'_{ij}}{C_{ij}}$$

where the summation is taken over all j that possess coupling capacitance with loop i. Here I'_i and I'_{ij} are the currents through the nonlinear resistors of the diode in loop i and the diode(s) common to loops i and j respectively. For an ideal capacitor $I'_i = I'_{ij} = 0$. C_{ij} is the capacitance (diode or otherwise) common to the i^{th} and j^{th} loops. C_{ii} is the capacitance in the i^{th} loop not common to any other loop.

Accordingly, using Equation (3) and the Runge-Kutta method, $(I)_{t+h}$ may be computed if $(I)_t$ is known.

Singular Inductance Matrix

The inductance matrix may be singular due to one of the following reasons:

(1) No inductance in one or more loops.

(2) Less than k inductors in k inductive loops.

k = 2, 3, . . ., n. Case (2) is not admissible by (a) of part 2 of "Program Limitations". In case (1) Equation (1) may be written (when loops are suitably renumbered):

$$\left[\begin{array}{c|c} L & 0 \\ \hline 0 & 0 \end{array}\right]\left(\begin{array}{c} \frac{dI^*}{dt} \\ \frac{dI^{**}}{dt} \end{array}\right) + \left[\begin{array}{c} R^* \\ \hline R^{**} \end{array}\right]\left(\begin{array}{c} I^* \\ I^{**} \end{array}\right) + \left(\begin{array}{c} \Sigma V_c{}^* \\ \Sigma V_c{}^{**} \end{array}\right) = \left(\begin{array}{c} E^* \\ E^{**} \end{array}\right)$$

Differentiating the dynamic equations corresponding to the noninductive loops and rearranging gives:

$$\left[\begin{array}{c|c} L^{*} & 0 \\ \hline & \\ R^{**} & \end{array}\right]\left(\frac{dI}{dt}\right)+\left[\begin{array}{c} R^{*} \\ \hline 0 \end{array}\right](I)+\left(\begin{array}{c} \Sigma V_c^{*} \\ \hline \frac{d}{dt}\Sigma V_c^{**} \end{array}\right)=\left(\begin{array}{c} E^{*} \\ \hline \frac{d}{dt}E^{**} \end{array}\right) \quad (4)$$

By (a) and (b) of part 2 of "Program Limitations", the "L" matrix of (4) is now nonsingular and so:

$$\left(\frac{dI}{dt}\right)=\left[\begin{array}{c|c} L^{*} & 0 \\ \hline & \\ R^{**} & \end{array}\right]^{-1}\left\{-\left[\begin{array}{c} R^{*} \\ \hline 0 \end{array}\right](I)-\left(\begin{array}{c} \Sigma V_c^{*} \\ \hline \frac{d}{dt}\Sigma V_c^{**} \end{array}\right)+\left(\begin{array}{c} E^{*} \\ \hline \frac{d}{dt}E^{**} \end{array}\right)\right\} \quad (4a)$$

Equation (4a) is now analogous to (2) and so the equivalent equation to (3) is:

$$\left(\frac{dI}{dt}\right)_{T_{r.k.}}=\left[\begin{array}{c|c} L^{*} & 0 \\ \hline & \\ R^{**} & \end{array}\right]^{-1}\left\{-\left[\begin{array}{c} R^{*} \\ \hline 0 \end{array}\right](I)-\left(\begin{array}{c} \Sigma V^{*} \\ \hline \frac{d}{dt}\Sigma V^{**} \end{array}\right)_t -(T_{r.k.}-t)\left(\begin{array}{c} \frac{d}{dt}\Sigma V^{*} \\ \hline \frac{d^2}{dt^2}\Sigma V^{**} \end{array}\right)_t+\left(\begin{array}{c} E^{*} \\ \hline \frac{d}{dt}E^{**} \end{array}\right)_{T_{r.k.}}\right\} \quad (5)$$

The only new term appearing in (5) is $\left(\frac{d^2}{dt^2}\Sigma V^{**}\right)$ which may be computed in the same manner as $\left(\frac{d\Sigma V_c}{dt}\right)$ except that current derivatives are substituted for currents.

Either Equation (3) or (5) applies to arbitrary circuits satisfying all the conditions specified in the "Program Limitation" section. Thus the Runge-Kutta method may be employed to obtain $(I)_{t+h}$ when conditions are known at time t. It should be remembered that each

diode must have an inductance in series with it (Program Limitation, part 4) so the second derivative of the voltage across a diode will never be required. Also, it should be noted that the derivative of the applied voltage is required in noninductive loops.

Calculation of New Conditions at Time t+h

The new conditions are

$$(1) \quad (I)_{t+h} \text{ and } \quad (I)_{t+h} = (I)_t + (\Delta I) \tag{6}$$

where ΔI is computed from (3) or (5) using the Runge-Kutta procedure.

(2) The new values of voltages across capacitors from which the new (ΣV_c) vector is computed.

$$V_c(t+h) = V_c(t) + \Delta V_c \tag{7}$$

where

$$\Delta V_c = \left[\frac{I_c(t+h) + I_c(t)}{2c} + \frac{-I' \text{ MEAN}}{c} \right] h \tag{8}$$

$I_c(t+h)$ and $I_c(t)$ are the capacitor currents at times $(t+h)$ and t respectively and are known. I'MEAN is the mean current through the nonlinear diode resistance during the time interval h between times t and $t+h$. I'MEAN = 0 for an ideal capacitor. In the case of a diode, I'MEAN may be obtained to a sufficiently good approximation by the following method:

(a) Compute ΔV_c as though I'MEAN = value of I' with the capacitor (diode) voltage equal to $V_c(t)$.

(b) Compute I' with capacitor (diode) voltage = $V_c(t) + \Delta V_c$ as obtained from (a).

(c) Take I'MEAN as the mean of the 2 I'(s) as computed in (a) and (b) and use Equations (8) and (7) to get $V_c(t+h)$.

THE INPUT STATEMENT

The input statement must define the circuit, the initial conditions (currents and capacitor voltages) and the driving voltages, if any. All the currents and capacitor voltages must be specified even though some or all of these may be zero, but only the non-zero driving voltages (non-zero derivatives of driving voltages in cases of non-inductive loops) need to be specified.

The following hierarchy of codes is used and explained below:

(1) 9999 99 9999

This is the END OF INPUT statement.

(2) 9999 99 99xx

The next word of the input statement is the initial value of I_{xx}.

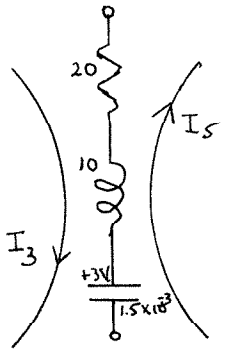
(3) 9999 99 xxyy

The words of the input statement between this code and the next code specify the elements common to loops xx and yy. In this statement xx $\leq$ yy and xx = yy if elements have only one loop current flowing through them. Immediately following this statement the type of element is specified and

0000 00 0001	classifies a resistor
0000 00 0002	classifies an inductor
0000 00 0003	classifies a capacitor

Immediately following the classification word the value of the element (in ohms, henries, or farads) appears and in the case of capacitance its initial voltage (which must be the voltage drop in the direction of I_{xx}) is the next word. Then the next element (also in loops xx and yy) is classified and its value, and initial voltage in case of a capacitor, is given. Only one of each type of element may be specified.

Example: Suppose that I_3 and I_5 flow through a resistance of 20 ohms, an inductance of 10 henries and a capacity of $1.5\ \ 10^{-3}$ farads (scaled values) and the capacity initially is charged to 3 volts as shown in sketch below.



The input statement is

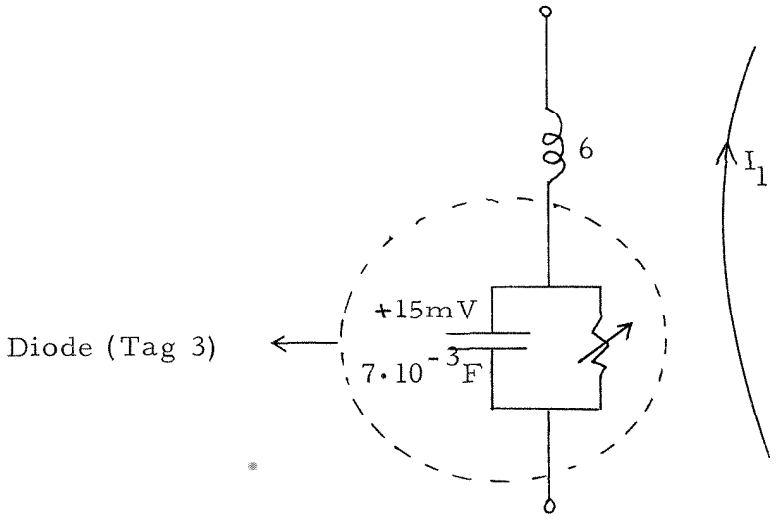
9999 99 0305	(I_3-I_5) flows in the following elements.
0 02	Inductance follows.
5210 00 0000	Value of inductance.
0 01	Resistance follows.
5220 00 0000	Value of resistance.
0 03	Capacitor follows.
4815 00 0000	Value of capacitor.
5130 00 0000	Initial voltage.

Diode Classification

It has been previously stated that 7 different diodes may be used. The word "different" here means that the diodes possess characteristic V-I curves that are not identical. Each different diode may be given one of the following numbers: 1, 2, 3, 4, 5, 8, and 9 - and this number is used as a tag to identify the diode. On the input statement the diode is classified as a capacitor except that the sign of the capacitor value bears the tag number associated with that diode. Tag numbers 8 and 9 are to be avoided if possible since there may be limited trouble in reading in 8's and 9's in the sign column.

Example:

Suppose I_1 flows through the following circuit:



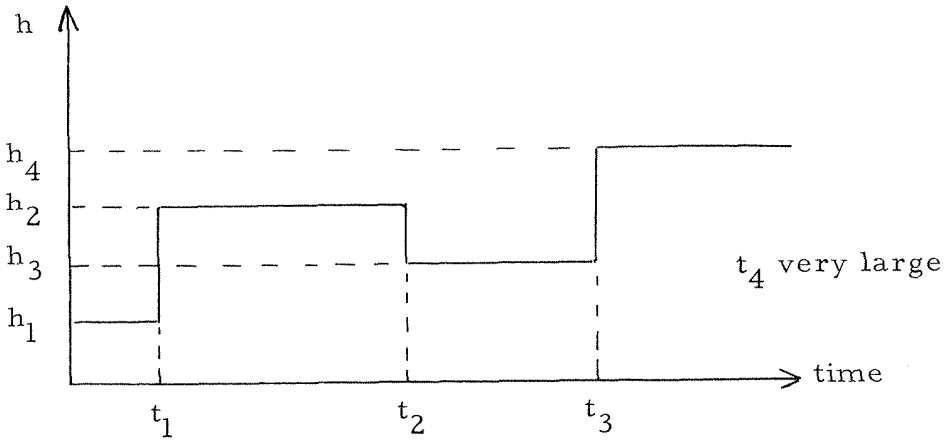
The input statement is

9999 99 0101	I_1 flows in the following elements.
02	Inductance follows.
5160 00 0000	Value of inductance.
03	Capacity follows.
3 4870 00 0000	Diode (Tag. 3) capacitance.
-4915 00 0000	INITIAL VOLTAGE (in volts).

Alternately it may be stated that an ideal capacitor has a Tag. 0 associated with it. The negative value of the initial voltage across the capacitor in the above example is due to the fact that, in the direction of I_1, the voltage drop across the capacitor is -15×10^{-3} volts (-15 millivolts).

(4) 9999 90 0000

The words of the input statement between this and the next code specify the value of h (time increment) which may be stepwise time dependent. Suppose the plot of h against time is:



The input statement is

9999 90 0000

h_1, t_1 } $h = h_1$, $0 \leq t < t_1$

h_2, t_2 } $h = h_2$, $t_1 \leq t < t_2$

h_3, t_3, h_4 } In floating point form

The next input statement (which is 999i ii iiii where i'(s) can have any value) immediately follows h_4 and is automatically used as t_4.

(5) 9999 00 0pXX

The words of the input statement between this and the next code relate to the driving voltage in loop XX ; i.e., E_{XX} (the time derivative of driving voltage in loop XX if there is no inductance in this loop) which is classified by p.

p = 1 means E_{XX} is a series of step functions.

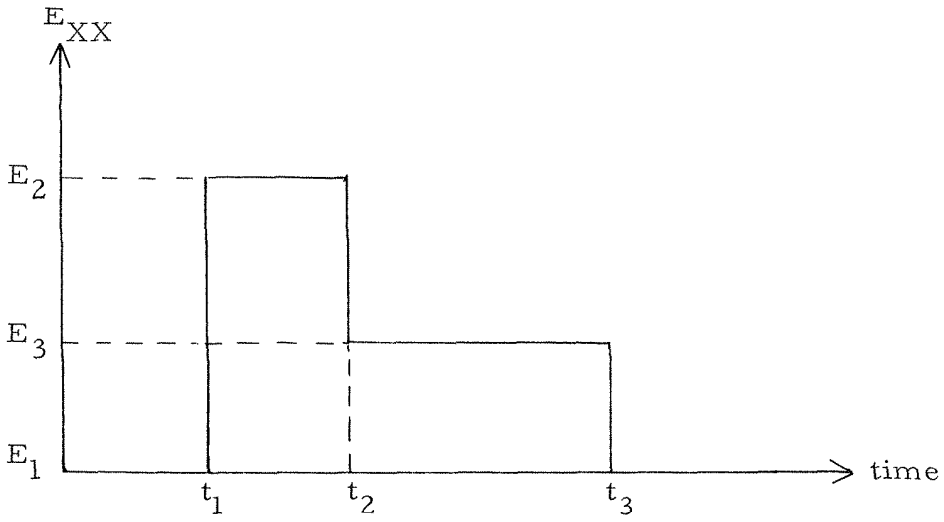
p = 2 means E_{XX} is a combination of step and ramp functions.

If p is not equal to 1 or 2 a subprogram must be included to compute E_{XX}. The exit to the subprogram is obtained by inserting the instruction BUN aaaa (unconditional transfer to location aaaa) into location 0494 (relative to the initial address of the compiler). Exit to location aaaa will occur with the number p in the 4th most significant digit position (sign excluded) of the A register. The time ($T_{r.k.}$) will be in location 1222 (relative). The subprogram must return to location 0505 (relative) with E_{XX} in the A register.

Note:- p can be replaced by a two digit number in the 7th and 8th most significant positions of the input format and these will be in the 3rd and 4th positions on exit to the subprogram

Example 1

Suppose E_{XX} has a time variation as shown below.



The input statement is

9999 00 01XX

E_1

t_1 } $0 \leq t < t_1$ $E = E_1$

E_2

t_2 } $t_1 < t < t_2$ $E = E_2$

E_3

t_3

E_1

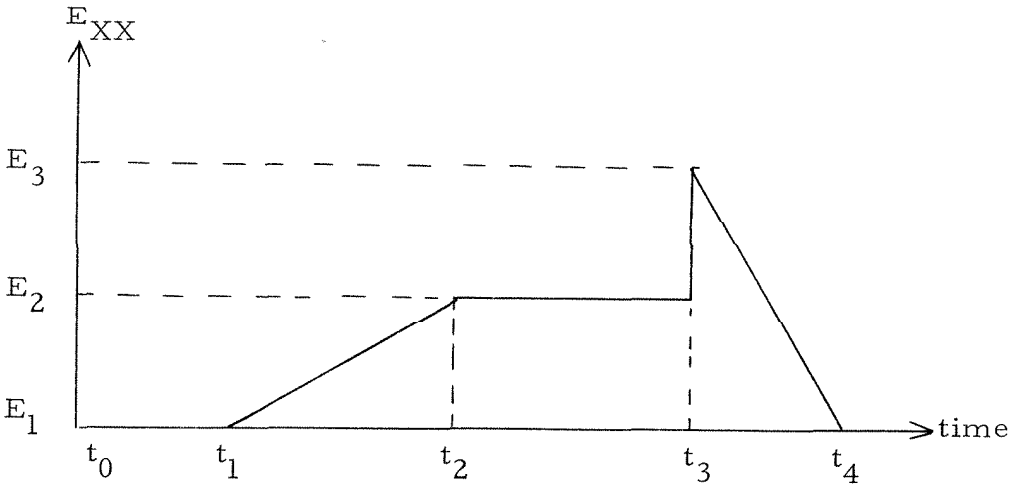
} Floating point form

Note: At $t = t_2$, $E = \frac{E_2 + E_3}{2}$; i.e., 1/2 step.

t_4 is again the next code which is 999i ii iiii.

Example 2

Suppose E_{XX} has the time variation as shown below.



The input statement is

9999 00 02XX

E_1
t_0 } 1st co-ordinate point on E_{XX} - t curve

E_1
t_1 } 2nd co-ordinate point on E_{XX} - t curve

E_2
t_2 } 3rd co-ordinate point on E_{XX} - t curve

E_2
t_3 } 4th co-ordinate point on E_{XX} - t curve

E_3
t_3 } 5th co-ordinate point on E_{XX} - t curve

E_1
t_4 } 6th co-ordinate point on E_{XX} - t curve

E_1 } 7th co-ordinate point on E_{XX} - t curve

There is no need to insert t_5 since the next word is 999i ii iiii.

(6) (a) 9991 00 xxyy

This is a print instruction and reads print I_{xx}-I_{yy} ($xx \leq yy$). If xx = yy it reads print I_{xx}.

Note: Only one word is required in the input statement to print the current in any element.

(b) 9990 00 xxyy
0p 0r0v

This is also a print instruction and specifies that the total voltage across some or all the elements common to loops xx and yy is to be printed.

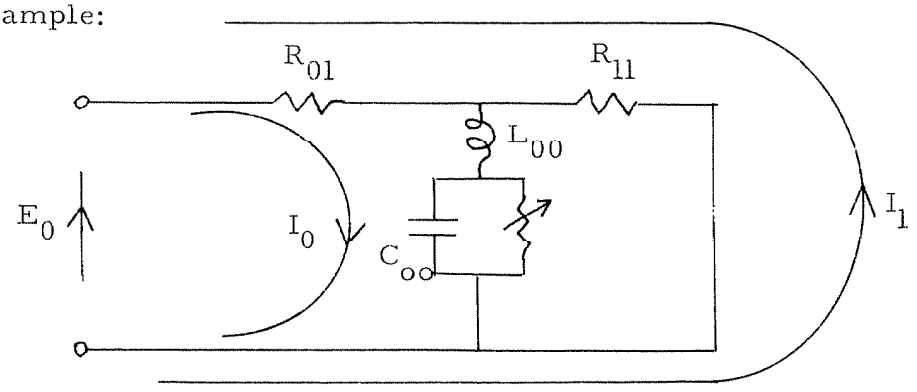
p = 3 voltage across capacitor (or diode) is included in printout.

r = 2 voltage across inductance is included in printout.

v = 1 voltage across resistor is included in printout.

If p, r, or v = 0, the corresponding voltage is not included.

Example:



Suppose we wish to print:

(1) The current I_o

(2) The current $(I_o - I_1)$

(3) The voltage across $L_{00} + C_{00}$

The input statement is

9991 00 0000	Print I_o
9991 00 0001	Print $(I_o - I_1)$
9990 00 0000	
03 0200	Print voltage across L_{00} and C_{00}

Comment

It is not always possible to print the voltage across a resistor. If the L matrix was originally singular the resistance element may have been transferred from the R to the L matrix and the resistance in the R matrix may now be zero. The result is that a voltage may sometimes be printed as a zero when in point of fact this is not so.

Printout occurs after every S iterations where S may be preset $\left[S \times 10^{-10}\right.$ in location 0475 (Relative)$\left.\right]$.

Concluding Remarks About the Input Statement

The input statement must be read into consecutive locations beginning at 0000. Consequently on tape the input statement should be preceded by a

6 0000 PRB 0000

command and followed by a

6 0000 HALT 0000

command.

DIODE CHARACTERISTIC

Every diode with a different tag number must have its V-I characteristic specified. A maximum of 20 points on the characteristic may be specified and between consecutive points (consecutive values of V) the V-I curve is interpolated as a straight line. The

voltage coordinates of the m($m \leq 20$) points on the characteristic are arranged in the order in which they appear on the real line starting from the left and must be read in that order into the m consecutive cells beginning at the relative location

(a) 1274 + 40 (k-1) where k is the tag number of the diode and k = 1, 2, 3, 4, or 5.

(b) 1274 + 40 (k - 3), k = 8 or 9.

The corresponding currents must be read into addresses 20 greater than their respective voltages.

In tunnel diode circuits a convenient time scaling is to let 1 second computer time be equivalent to 1 mμsecond real time.

The inductance and capacitance is 10^9 times that of real time and resistance is unchanged.

It is, perhaps, simpler to use milliamps and millivolts rather than volts and amps. This has no effect on element values. However, it is important to remember that the V-I diode characteristic must be in a consistent system of units with the driving sources and the initial conditions.

PREPARATION OF DATA TAPE

Assume m given points (V_i , I_i) have been selected from the diode characteristic and the diode has tag k where $m \leq 20$, $i = 1, 2, 3, \ldots, m$, and $V_{(i+1)} > V_i$.

The data tape is

6 PRB aaaa aaaa = $\begin{cases} 1274 + 40(k-1), & k = 1, 2 \ldots 5. \\ 1274 + 40(k-3), & k = 8, 9. \end{cases}$

V_1

V_2

V_3

.

.

.

V_m

} In floating point form

6 PRB (aaaa + 20)

I_1
I_2
I_3
.
.
.
I_m

} In floating point form

6 0000 HALT 0000

The above input must be repeated for every different diode except that the 6 0000 HALT 0000 need not be included until all the data has been read in.

OPERATING INSTRUCTIONS

The program tape may be read into any location aaaa such that

$I + aaaa + 4n^2 + 15n + 1274 + 40q \leq 5000$ and $aaaa \geq I$

where n is the number of loops, I is the length of the input statement, and q is the number of different diodes.

Having decided on aaaa the procedure is:

(1) Set the B-Register to aaaa and start read in of program tape with a PRB 0000 command. Following the read in of the program tape, a sum check routine is read into location 4981 to 4997 and this routine is immediately executed. The computer then halts with one of the following commands in the C-Register:

(a) The command

0000 HALT 0000

(b) The command

0000 HALT 5555

This indicated a read in error or an error on the tape. The error, Mod 1, is in the A-Register.

(2) If the computer halts on (a) above, read in the input statement tape and the data tape (s). The input statement tape goes into 0000 and up.

(3) Using the keyboard, key into location 0910 (Relative) of the program the maximum allowable diode voltage.

(4) The print out routine will be executed after every S steps where $(S - 1) \times 10^{-10}$ is in location 0475 (Relative). S is set = 10 on read in. Change S if necessary.

(5) Transfer control to 0000 (Relative).

(6) In case of computer halt, consult the section on error halts below.

(7) The time increment (h) may be altered if desired in the following way:

(a) Set the S register to 0476 (Relative).

(b) Set S to P switch on and when computer halts change the input statement so that new h will be obtained.

(c) Depress start switch.

(8) By the same process as in (7) applied voltages may be changed at any time.

(9) The program may be stopped at any time and started over again with new circuit parameters, etc. in the following way:

(a) Press clear.

(b) Make necessary changes to the input statement and/or the diode characteristics.

(c) Operate as indicated in (3) and up. [No need to execute (3) or (4) unless there is a change in the maximum diode voltage or in the number of iterations between print outs] .

ERROR HALTS

(1) Halt on the command

HALT 0000

after printing one word. The word printed is an error in the input statement and the B-Register contains the address of the error.

(2) Overflow halt with the P-Register set to aaaa where $975 < aaaa < 1155$ (relative).

Failure is due to either

(a) Part 2 of program limitations not satisfied.

(b) Error in the input statement.

(c) The matrix

$$\left[\begin{array}{c|c} L^{*} & 0 \\ \hline & \\ R^{**} & \end{array}\right]$$

is poorly conditioned.

(3) Halt on command

HALT 3333

This means that a diode voltage has gone below the minimum value specified by its characteristic. The A-Register contains the voltage across this diode and the B-Register setting deterimines the tag-number of the diode.

B Register	Tag Number
0000	1
0040	2
0080	3
0120	4
0160	5
0200	8
0240	9

(4) Halt on the command

HALT 0240

This means a diode voltage is greater than the maximum specified by its characteristic. Again the A-Register contains the voltage and the diode tag number may be obtained as in (3).

Procedure Following an Error Halt

In cases (1) and (2) the error must be corrected and the program may be again entered at 0000 (Relative).

In cases (3) and (4) the error is due to either

(a) The iterative procedure is unstable due to a too large h. In this case change h in the input statement and re-enter program at 0000 (Relative).

(b) An error in the diode characteristic or that step 3 of "Operating Instructions" was not correctly performed. When error has been located and corrected, re-enter program at 0000 (Relative).

(c) An error in the input statement.

OUTPUT FORMAT

The output will be those voltages and currents as specified by the input statement. Their initial values and their values after every s steps will be printed. The print out will occur in the order in which they are requested in the input statement and will be always preceded by the values of time (T) and time increment h.

In cases of apparent error in print out, see "Comment" under 6(b) of the "Input Statement".