ANALOG GAAS OPTOELECTRONIC INTEGRATED CIRCUITS FOR LARGE SCALE ARRAYS

Thesis By

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Abstract

This thesis focuses on the design and fabrication of large arrays of analog optoelectronic circuits where transistors and optoelectronic devices such as photodetectors and LEDs are monolithically integrated on a single substrate. This optoelectronic approach allows one to design complex functions with the transistors and use the optoelectronic devices to couple the optical signals in and out of the circuit.

The specific application for the analog optoelectronic circuits is large scale neuron arrays for optical neural networks. A neural network has two main elements: nonlinear elements (neurons) and interconnections (synapses). The neurons perform a nonlinear operation on their incoming signals while the synapses provide the weighted connection between neurons. In an optical neural network, the neurons are arranged as two-dimensional arrays that are optically interconnected using the third dimension.

Two approaches to the design and fabrication of a variety of optoelectronic GaAs neuron circuits will be described. In the first approach, GaAs MESFETs (Metal-Semiconductor-Field-Effect Transistors), double heterostructure GaAs/AlGaAs LEDs, and photodetectors are fabricated on a GaAs substrate containing epitaxial layers for the different devices. In the other approach, the detector/transistor portion of the circuit is fabricated by Vitesse through MOSIS and the LEDs are integrated afterwards using MBE regrowth. This second approach produces circuits with high uniformity and allows one to fabricate more complex optoelectronic circuits at a reasonable cost and turn-around-time. Most of the circuits are based on high responsiv-

ity optical FET detectors, which make it possible to build high optical gain circuit with little electrical power dissipation and small surface area.

Contents

Chapter 1

Introduction

1.1 Optoelectronic Computing

As the complexity and speed of computation increases, the performance of serial electronic processors becomes limited by interconnect delays, power dissipation, and input/output pins [49, 14]. By using optical input/output signals and optical interconnects rather than electrical signals, we can eliminate the electronic bottlenecks, thereby increasing the processing speed and interconnect density [13]. The optoelectronic processor –which replaces the electrical processor – has optical signals as inputs, performs the required nonlinear computation electronically, and produces optical outputs which can be fed to other processing elements. The optical signals can easily be processed in parallel because the optical signals do not interact with each other the way electrical signals do. Since the processors in an optical computer are connected optically, these processors must be able to accept optical inputs and produce optical outputs. So an optoelectronic processor is an integration of photodetectors, transistors, and an active optical output device. Typically the optoelectronic processing units are arranged in a two-dimensional

array, and connection between processors is done through the third dimension. The interconnections can be implemented using lenses for some specific interconnection patterns or, for full flexibility in the interconnection pattern, holograms. The connections are typically lossy, so each processing unit must also provide optical gain while at the same time dissipating as little electrical power as possible so that overheating is not a problem. These factors – optical input/output, large optical gain, and low electrical power consumption– will be considered throughout this thesis.

1.2 Application: Optical Neural Networks

One type of computing architecture which suffers greatly from electronic bottlenecks, due to the large number of interconnections required, is the highly parallel neural network architecture. Using biological systems as a model, a neural network is a collection of a large number of simple processing units which are called neurons. The human brain consists of about 10^{11} neurons [24]. Each neuron receives inputs from many other neurons, computes a simple nonlinear function, and produces an output signal which is passed to each of the many neurons in the next layer of the network or to neurons within the same layer. In a purely electronic implementation, the number of neurons is limited to a few hundred because of the area required for the interconnection wires [3]. In an optical neural network, the neuron function can be implemented with a simple optoelectronic circuit, requiring only a few transistors per neuron circuit along with photodetectors and a light emitting diode (LED) to couple the light in and out of the circuit. The density to

which these optoelectronic circuits can be fabricated is limited by power dissipation and uniformity. This thesis will focus primarily on optoelectronic ciruits for neural networks, because neural network architectures represent the extreme in number of processing units and interconnections required.

The most common neuron function in a neural network is a threshold operation. Each neuron in a given layer sums the inputs from many neurons of a previous layer and compares the summation to a threshold. If the summation is larger than the threshold, the output of the neuron is on, otherwise it is off. The transition between off and on does not have to be very sharp. The hyperbolic tangent is often used as a closed form expression for the neuron response. It is expressed as

$$Y_j = A \tanh(\sum_{i=1}^{N} w_{ij} X_i) \tag{1.1}$$

where X_i are the inputs to the network, w_{ij} are the interconnection weights, A is the gain, N is the number of input neurons, and Y_j is the output of the jth neuron. A processing element that performs a hard threshold on its weighted inputs is called a McCulloch-Pitts neuron [34]. The function of the entire network, whether it be face-recognition or processing control calculations, is stored in the connection strengths between neurons. By adjusting the interconnections weights dependent on the comparison of the output of the system with the desired response, the neural network can be trained to perform a specific task. In theory, a two layer network can implement any function, but it is sometimes difficult to find an efficient algorithm with which to train the network [1, 2].

One of the first neural networks to be implemented optically was a content

addressable memory trained using a Hopfield model network [21, 12]. The system computed the vector matrix multiplication in Eq 1.1 optically. The network had 32 inputs and 32 outputs where the inputs were represented by LEDs and the outputs were detected on Si detector arrays. Because the detectors, LEDs, and the electronic circuits were not integrated the system was rather bulky. Monolithic integration of these components offers the advantage of high circuit density and thus overall compactness.

1.3 Considerations for Optoelectronic Circuit Implementation

In addition to compactness, by implementing the nonlinear neuron response in an optoelectronic circuit, one can provide optical gain as well as flexibility in the function implemented. The integration of the photonic devices and the electronic devices can be done either monolithically or in a hybrid manner. Currently there are a number of different hybrid integration approaches being investigated, where one integrates the optical output device, either modulator or source, with Si electronic circuitry. For instance, by coating a Si CMOS chip with liquid crystal, one can integrate optical modulators with CMOS circuitry [25]. This technique takes advantage of the highly developed silicon CMOS circuitry as well as research done on liquid crystal modulators for displays. Current Si/LC chips use ferroelectric liquid crystals modulators which can produce a contrast ration of 10:1 with switching speeds on the order of 100μsec[35].

Flip-chip bonding is a technique used to connect two different substrates

together. Typically the detector and electronic circuitry are fabricated on one substrate and then a different substrate is used for the optical output device [22, 15]. The two substrates are electrically and physically connected together using indium solder bumps. Flip-chip bonding has the advantage that one can optimize the performance of each individual component, and then assemble the entire array using the bonding pads for electrical connection. Some of the main problems with this technology are: the reliability of the solder bumps due to contact with air or to different thermal expansion coefficients of the two materials, the need for either the optical or electrical signals to be able to penetrate at least one of the substrates, and the need for the bond pads to be planar with the top surface of the substrate [32].

Epitaxial lift-off is a relatively new technique for hybrid integration [62, 10]. The active optical devices are fabricated on a substrate with epitaxial layers. A sacrificial AlAs layer is added between the desired epilayers and the substrate. When this layer is removed by wet chemical etching, the epilayers are released from the substrate. These epilayers can then be placed in contact with a different substrate, such as a silicon chip [6]. Using this technique, the optical devices can be optimized in GaAs and the electronic circuits fabricated in Si. The epi device is typically transferred under water and held in place by Van der Waals forces. This technique suffers from low transfer yield, and reliability problems with the electrical contact over time.

All of these hybrid integration techniques suffer from reliability and stability problems from the mechanical assembly, as well as degradation in the contacts between the two materials. The alternative approach is to monolithi-

cally integrate all the devices on a single wafer. The concept of monolithically integrating photonic devices with electronic devices was first demonstrated by Yariv *et al.*, where they integrated a Field Effect Transistor with a laser diode in GaAs [65]. Monolithic integration of photodetectors, electronic circuitry, and optical modulators or LEDs in GaAs offers several advantages over many of the hybrid integrations, but in some sense, the difficulty in assembly and packaging in hybrid integrations is replaced by compromises in the device structures in monolithic integrations.

This thesis addresses the design and fabrication of high density optoelectronic neuron arrays monolithically integrated in GaAs. In Chapter 2, the requirements of the electronic circuit and how they influence the circuit design are discussed. Chapter 3 describes the design, fabrication, and performance of two different neuron circuits fabricated on a semi-insulating GaAs substrate with GaAs/AlGaAs epitaxial layers. Chapter 4 describes a method to build high density optoelectronic circuits by integrating LEDs on processed GaAs electronic circuits fabricated by Vitesse. Finally, Chapter 5 discusses the results from integrating LEDs on GaAs Vitesse chips using Molecular Beam Epitaxy (MBE) regrowth and results from some specific high density optoelectronic neuron circuits.

Chapter 2

Requirements of the Optoelectronic Circuit

There are four important characteristics which determine the performance of a particular optoelectronic circuit – power dissipation, optical gain, switching speed, and uniformity. Electrical power dissipation can be a limiting factor at the high integration densities for circuits which integrate active optical devices such as laser diodes or LEDs. As we will see in Section 2.2, the electrical power dissipation of the optoelectronic circuit is due mostly to the electrical power dissipated by the LED or laser diode. It is therefore important to be able to operate the circuit with very little current.

Optical gain refers to the ratio of the optical output power to the optical input power required to implement the desired neuron response. It is necessary because optical interconnections are generally lossy – the signal level must be restored by the neural planes at each stage in order to make the implementation of multilayer networks possible. The optical gain required depends on the optical interconnection loss in the system and is architecture dependent. The interconnection loss will be discussed in section 2.3.

Switching speed is also important in designing optical neural network systems. To some extent one can give up on the performance in one area, either power dissipation, optical gain or speed, to increase performance of another characteristic. The number of connections per second per unit area can be used as a figure of merit which describes the performance of a particular circuit integration. This is expressed as

$$F = \frac{NG}{\tau}, \qquad \frac{\text{connections}}{\text{cm}^2\text{sec}} \tag{2.1}$$

where N is the number of neurons per unit area, G the optical gain, and τ the switching time of the circuit. The product NG determines the number of neuron connections achievable because the optical gain, G, limits the possible signal fan-out. The figure of merit will be derived in the following section for specific circuit implementations .

The last important characteristic of the optoelectronic circuit is the uniformity of the fabricated array. Without good uniformity, the computation will not be accurate. Section 2.5 will discuss how the probability of making an error in the threshold circuit depends on uniformity.

2.1 GaAs Optoelectronic Circuit

The circuit shown in Fig. 2.1 implements a sigmoidal threshold response and serves as our optical neuron. The LED or laser diode is driven by a Metal-Semiconductor-Field-Effect-Transistor (MESFET) whose gate voltage is controlled by an input photodetector and biasing element. The issues concerning the choices for the photodectors and the active optical output

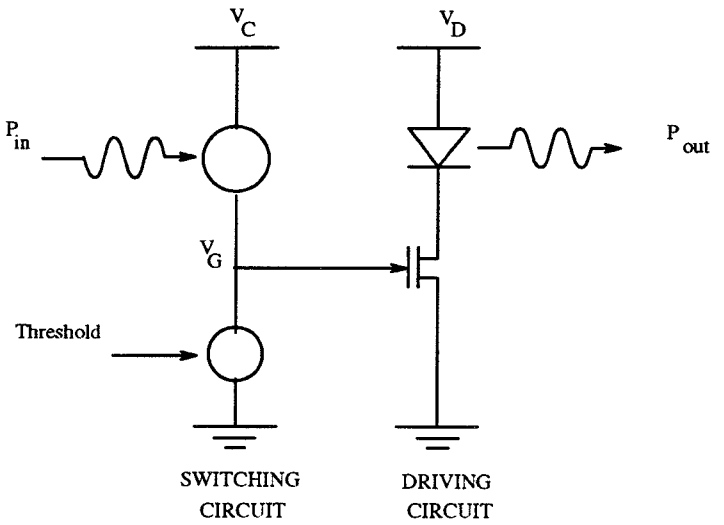


Figure 2.1: Basic optoelectronic threshold neuron circuit

are discussed in Sections 2.4 and 2.2. We choose MESFETs over bipolar junction transistors (BJT) because BJTs suffer from carrier recombination at low current levels and therefore have reduced current gain. The static common emitter current gain, β_0, of a BJT (where I_c is the dc collector current and I_B is the dc base current) increases with collector cuurent as follows

$$\beta_0 \sim (I_C)^{1-1/m} \tag{2.2}$$

where m is the base-emitter junction ideality factor [56]. When there is no recombination current $m = 1$ and when the recombination current is dominant $m = 2$. In GaAs, the recombination current is quite large, so BJTs are undesirable for low current circuits.

On the other hand, MESFETs are voltage controlled devices and have

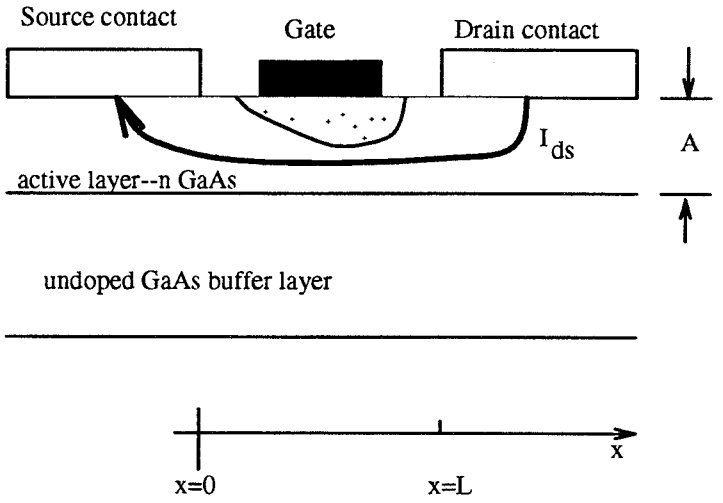


Figure 2.2: Cross-section of a GaAs MESFET

good performance even at low current levels. A brief description of a GaAs MESFET is given below to illustrate the basic operation of the device. For a more comprehensive study, the reader is referred to "Physics of Semiconductor Devices" by Shur [52]. A MESFET consists of two ohmic contacts, one is called the source and the other is the drain, with a thin resistive channel in between. The cross-section of a GaAs MESFET is shown in Figure 2.2. For this discussion, we will assume that the channel is a uniformly doped n-type epitaxial layer grown on top of an undoped buffer layer. A Schottky gate electrode placed on the channel modulates the conductance of the channel by applying an electric field. The applied gate voltage changes the depletion width of the Schottky junction which changes the thickness of the conducting channel. The depletion width, $A_d(x)$, at any point along the channel is determined by the potential at that particular point and is expressed as follows:

$$A_d(x) = \frac{(2\epsilon[V(x) + V_{bi} - V_g])^{1/2}}{qN_D} \tag{2.3}$$

where N_D is the donor concentration, V_{bi} in the built-in potential due to the Schottky contact, V_g is the applied gate voltage and $V(x)$ is the channel potential due to the voltage applied between the drain and the source. The boundary conditions for the channel potential are : $V(L) = V_D$ and $V(0) =$ 0V, where L is the channel length. The voltage required to fully deplete the channel at any point along x is called the pinch-off voltage,

$$V_p = V(x) + V_{bi} - V_g = \frac{qN_D A^2}{2\epsilon}. \tag{2.4}$$

The gate voltage required to fully deplete the channel when $V_{ds} = 0V$ is called the threshold voltage, V_T. If a negative gate voltage is required to fully deplete the channel ($V_T <$ 0V), the MESFET is called a depletion-mode MESFET, because the applied gate voltage depletes the channel. If the channel is fully depleted for $V_g = 0V$ ($V_T >$ 0V), then the MESFET is called an enhancement-mode MESFET, because the applied gate voltage creates or enhances the conducting channel.

We shall assume that the channel potential does not vary significantly for small changes (less than the active layer thickness, A) in the x direction. At each point, then, along the x, we can determine the change in the potential from the change in the channel thickness.

$$dV = I_{ds}dR = \frac{I_{ds}dx}{q\mu_n N_D W[A - A_d(x)]} \tag{2.5}$$

where dR is the differential change in the channel resistance, and μ_n is the mobility of the electrons. In the linear regime, the drain-source current is given by

$$I_{ds} = g_0[V_D - \frac{2[(V_D + V_{bi} - V_g)^{3/2} - (V_{bi} - V_g)^{3/2}]}{3V_p^{1/2}}] \tag{2.6}$$

where $g_0 = q\mu_n N_D W A/L$ is the conductance of the undepleted doped channel, and L is the gate length. This relationship holds only when there is a conducting channel. As the drain-source voltage, V_D, increases the channel thickness decreases. As the channel thickness approaches zero, the current begins to saturate. The drain-source voltage for which the current saturates is called V_{sat} and is expressed as $V_{sat} = V_p - V_{bi} + V_g$.

The drain-source saturation current is

$$I_{sat} = g_0[\frac{V_p}{3} + \frac{(2(V_{bi} - V_g)^{3/2})}{3V_p^{1/2}} - V_{bi} + V_g] \tag{2.7}$$

and the transconductance of the device in the saturation region:

$$(g_m)_s = g_0(1 - (\frac{V_{bi} - V_g}{V_p})^{1/2}). \tag{2.8}$$

This model assumes no velocity saturation. In GaAs, the electron velocity saturates when the electric field exceeds 3.5kV/cm which corresponds to gate lengths less than 5μm for MESFETs. The saturation current can be modeled fairly accurately with the following equation

$$(I_{ds})_{sat} = \beta(V_g - V_T)^2 \quad \text{where} \quad \beta = \frac{2\epsilon\mu_n v_s W}{A(\mu_n v_{p0} + 3v_s L)} \tag{2.9}$$

and the transconductance is given by [53]

$$(g_m)_s = 2\beta(V_g - V_T), \tag{2.10}$$

where $\beta = \frac{2\epsilon\mu_n v_s W}{A(\mu_n V_p + 3v_s L)}$ and v_s is the saturate velocity which is approximately 2×10^7cm/s. Eq (2.9) and (2.10) are used extensively to model to first order the behavior of MESFETs. For circuit design, more accurate models which required numerical analysis are used.

2.2 Choice of the Optical Output Device

LEDs and laser diodes are the two choices for on-chip light sources. Laser diodes have higher quantum efficiency and a more directed beam than LEDs which means higher light efficiency[64, 40]. Unfortunately, electrical power dissipation is a limiting factor for high density circuits. The power dissipation of the optoelectronic neuron circuit shown in Figure 2.1 is

$$P = I_{LED}V_D + I_{ph}V_C \approx I_{LED}V_D \tag{2.11}$$

where I is the current through the LED or laser diode and I_{ph} is the photocurrent is the input branch of the circuit. Since $I >> I_{ph}$, we can neglect the power dissipated in the input branch. The power dissipation of an individual neuron circuit sets the maximum density. The maximum neuron circuit density, N, is given by

$$N = \frac{P_{max}}{P} = \frac{P_{max}}{IV_D} \tag{2.12}$$

where P_{max} is the maximum heat dissipation of the material. For GaAs P_{max}=10W/cm^2. The optical power generated by each laser diode is

$$P_{opt,LD} = \eta_{LD}(I - I_{th}), \tag{2.13}$$

where η_{LD} is the external efficiency and I_{th} is the threshold current of the laser diode. Substituting in the expression for the maximum current, we obtain the total optical power output by the chip:

$$P_{opt,LD}N = \eta_{LD}(\frac{P_{max}A}{V_D} - I_{th}N). \tag{2.14}$$

For typical values ($P_{max} = 1\ W/cm^2$, $V_D = 2\ Volts$, $I_{th} = 500\mu A$) the total output power falls to zero when N=1000, and A=1cm^2. This is clearly the maximum density of neurons we can achieve if we opt for laser diodes.

The optical power out of the LED is given as

$$P_{out} = \eta_{LED}I_{LED} \tag{2.15}$$

where η_{LED} is the external efficiency of the LED. If the interconnection loss is η_h and the required optical gain is G, then the optical power at the input (assuming similar neural planes are cascaded) is

$$P_{in} = \eta_{LED}\eta_h I_{LED}/G. \tag{2.16}$$

The photocurrent available to charge up the gate of the MESFET capacitor, C_g, if the responsivity of the detector is η_D, is

$$I_{ph} = \eta_D P_{in}. \tag{2.17}$$

The switching time of circuit is

$$\tau = \frac{C_g V_c}{2I_{ph}}. \tag{2.18}$$

Therefore we can express the figure of merit, F, in terms of parameters of the devices in the circuit and not of the particular operating conditions. If we do this, we find that

$$\mathrm{F} = \frac{\eta_{LED}\eta_h\eta_D P_{max}}{2C_g V_C V_D}. \tag{2.19}$$

Figure 2.3 shows the figure of merit, F, plotted against the switching speed of a threshold circuit for the laser diode and the light emitting diode. The switching speed is determined by the time required to charge the gate to a certain voltage. The drop in F for the laser diode as the switching time increases is due to the threshold current in the laser diode. At the slow switching speeds, the optical power is very low and the integration time of the circuit long. Because of the absence of a threshold current, LEDs can operate with very small currents allowing a density of up to 100,000/cm^2. The conclusion, therefore, is that if one is interested in high density arrays that operate with relatively slow switching times then LEDs are the preferred choice.

The other option for the optical output is an optical modulator[37, 8, 27]. The principle advantages of modulators derive from the fact that the light source is off-chip so that optical gain can be increased simply by making the source brighter without increasing appreciably the power consumption on the chip. This allows us to build a higher density array or have a faster switching time. Moreover, the external source makes a spatially coherent ar-

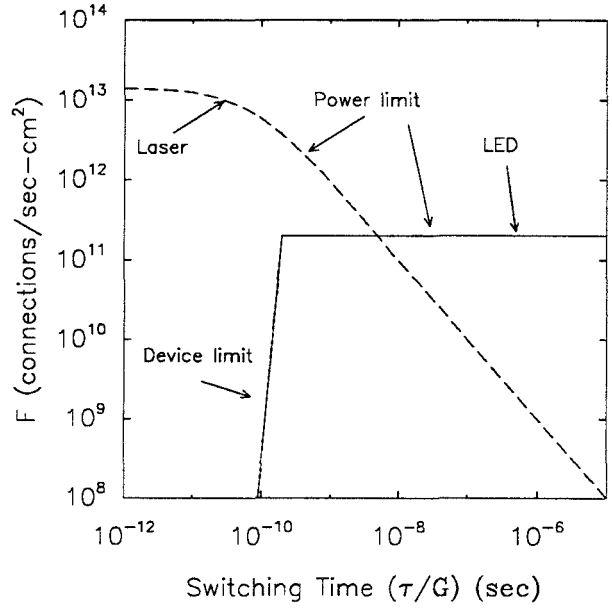


Figure 2.3: Figure of Merit as a function of the switching speed for laser diodes and LEDs

ray possible, which is a necessary property for most adaptive neural network architectures[45].

On the other hand, on-chip light sources, such as LEDs or laser diodes, have high contrast ratios, and require small driving voltages, simpler epitaxial structures, and less critical fabrication steps[37]. Moreover, with on-chip light sources it is generally much easier to build a system because the external light source, accompanying beamsplitter, and beam forming optics are not required, nor is it necessary to tune the source wavelength to match the modulators. Therefore, in comparing quantum well modulators with LEDs for building optoelectronic neuron arrays, in principle, modulators outperform LEDs in most respects. However, in practical terms, both for building a system and fabricating a large array, LEDs have strong advantages. Therefore, LED-based neurons can make it possible to fabricate in the near term

large, dense neuron arrays for applications such as early vision processing that do not require holographic adaptation [33].

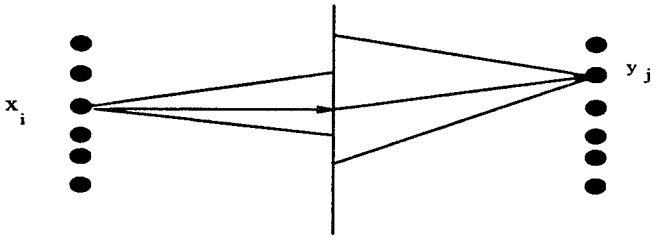
2.3 Interconnection Loss for Coherent vs Incoherent Optical Systems

The interconnection loss is determined by a number of factors including the type of light source used (coherent versus incoherent), interconnection medium used (e.g., holographic versus non-holographic), and the architecture of the network (e.g. number of connections per neuron). The LED circuits that we describe produce spatially incoherent illumination.

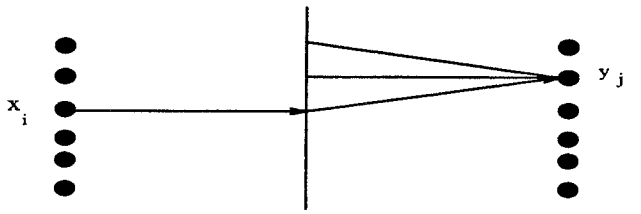
In general, incoherent systems are relatively inefficient because they radiate energy into a large cone angle and only a portion of the radiated energy is captured by the numerical aperture of the optical system. To determine the dependence of the light efficiency on the number of connections per neuron, C, we write the strength of the optical interconnection between the i-th and j-th neurons, η_{ij}, as follows:

$$\eta_{ij} = \eta_0 H(C) w_{ij}, \tag{2.20}$$

where η_0 is the optical loss (in intensity) obtained when only two neurons are connected, including the numerical aperture loss mentioned above as well as reflections, insertion loss of spatial light modulators, and the limitation on diffraction efficiency due to the holographic medium. H(C) (H(1) = 1) is a function that contains the dependence on the number of connections per neuron and $0 \leq w_{ij} \leq 1$ is the normalized weight of the connection[45].



(a) Nonholographic implementation



(b) Holographic implementation

Figure 2.4: Coherent and incoherent optical implementation schemes

The non-holographic interconnection system is shown in Fig. 2.4a. Light with intensity x_i is emitted from the i-th LED and is divided into C beams that impinge on C different spatial locations on the interconnection medium, one location for each neuron connected to the i-th unit. The interconnection strength w_{ij} is the intensity transmittance of the medium at each location. The j-th neuron collects light from C spatial locations on the interconnect medium to form its input as follows:

$$z_j = \sum_{i=1}^{C} \eta_{ij} x_i = \eta_0 H(C) \sum_{i=1}^{C} w_{ij} x_i. \tag{2.21}$$

In this case H(C)=1/C, since the light from each LED is evenly divided. The output is maximized when $x_i = P$ and $W_{ij} = 1$ for all i and j. Then $z_j = \eta_0 P$ which implies that the maximum efficiency of the optical connection

is essentially limited by the loss due to the finite numerical aperture of the system. The best known example of such an interconnection scheme is the vector-matrix realization of a neural network[12].

A schematic diagram for holographic interconnections is shown in Fig. 2.4b. Here, light from the i-th input LED is collimated and illuminates a hologram where K gratings are superimposed. The interconnection between the i-th and j-th neurons is realized by one of the gratings stored in the hologram by redirecting the light that is incident from the i-th neuron towards the j-th neuron. The interconnection weight w_{ij} is encoded in the strength of the grating. For a planar, amplitude hologram, its effective amplitude transmittance as a function of position x is

$$t_H(x) = \sum_K \sqrt{w_{ij} H(C)} \exp\left(j 2\pi u_{ij} x\right) \tag{2.22}$$

where u_{ij} is the spatial frequency of the holographic grating that connects the i-th and j-th neurons. The amplitude of each grating must be small enough to enforce the constraint that $0 \leq t_H \leq 1$. Since the hologram is formed as an incoherent sum of K variables, t_H grows in proportion to $\sqrt{K}$[46]. The requirement that $t_H \leq 1$ is enforced if

$$H(C) \leq 1/K. \tag{2.23}$$

In the simplest case, the total number of gratings K that are superimposed on the hologram equals C. This is the case of a completely shift invariant interconnection pattern with each neuron connected to C others with the same set of weights. In this case, the efficiency of the connections is identical to the

non-holographic efficiency. On the other hand, if each neuron connected by the hologram has a distinct receptive field then we need to record a separate grating for each pair of neurons. Therefore, K=CN, where N is the number of neurons. In this case, holographic interconnections are inferior to the non-holographic interconnections in terms of light efficiency by a factor N which is typically in excess of one thousand. Since holographic interconnections are more efficient with coherent illumination[46], the LED neuron circuits that we describe in this paper are best suited for holographic shift invariant circuits (e.g., early vision tasks) or for non-holographic interconnection schemes for which spatial incoherence is actually preferable. For the remainder of the discussion, we will make the assumption that H(C)=1/C.

2.4 Choice of Detectors

There are a number of different choices for the detector used in the circuit. In order to have the best circuit performance, one would like to integrate a detector with high detector responsivity and fast response time. Because the circuit is a monolithic integration, the detector structure and operating parameters must be compatible with the other devices in the circuit. The epilayers for the MESFET are quite simple: a thin n^+ layer for the ohmic contacts, an n channel layer, and a thick (0.5μm) undoped buffer layer under the channel. On the other hand, the LED is a double heterostructure GaAs/AlGaAs p-n junction with five distinct layer. The efficiency of the LED is determined largely by the thicknesses and doping concentrations of each layer. Among the choices are the bipolar phototransistor, the p-i-n photo-

diode, the Metal-Semiconductor-Metal (MSM) detector, and the photoconductor or optical Field-Effect-Transistor (OPFET). Because the avalanche photodiode (APD) detector requires large reverse bias, it is not a suitable candidate for integration.

The structure for the bipolar phototransistor is a double heterojunction N-p-N transistor. One can use the same epitaxial layers for the phototransistor and the LED, but the thicknesses and doping levels of the different layers conflict. While the phototransistor has current gain at high input levels, the responsivity at low optical intensities is reduced. For these reasons, the phototransistor is not a good choice for integration with the rest of the circuit.

Though the p-i-n photodiode and the LED also have very similar epitaxial layers, the optimal thicknesses and doping levels of the layers again conflict. However, the biggest drawback of the p-i-n photodiode is that the responsivity is always less than 1A/W. High responsivity is important for two reasons. The switching time of the circuit depends on the photocurrent. The larger the responsivity, the larger the photocurrent will be for a given input intensity. The larger the photocurrent, the faster the circuit switching. The second reason is that there is a gate-source leakage current in the MESFET which must be supplied by the photodetector. This leakage current can be as large as 1nA if the gate-source junction is forward biased, as is the case for enhancement-mode MESFETs. This leakage current sets the minimum input optical power for the circuit.

The Metal-Semiconductor-Metal (MSM) detector is made by depositing

two Schottky contacts on undoped GaAs. When a small voltage is applied, the GaAs layer between the contacts is depleted. Photocarriers generated in the depletion region are swept out to the contacts. While the responsivity of this detector is always less than 1A/W, the detectors can be integrated in the bottom undoped buffer layer of the complete epitaxial layers. Thus there are no competing design issues. MSM detectors also have very uniform response and fast response times. They also have a symmetric I-V curve, useful for applications which require bipolar weights.

The structure of an optical FET is very similar to a conventional MESFET. The device has two ohmic contacts (the source and drain) with a thin channel in between. Unlike the MESFET, there is no gate electrode. The mechanism of operation of an optical FET is based on photoconductivity [19]. Electron-hole pairs generated by the incident optical signal increase the conductivity of the channel. If the transit time for the electrons to cross the channel is short compared to the lifetime of the holes, then the detector responsivity can be much greater than 1 A/W. The expression for optical FET drain-source current is given by

$$I = \frac{\tau_h}{\tau_t}\eta' P_{in}, \tag{2.24}$$

where τ_h is the hole lifetime, τ_t is the electron transit time, and η' is the quantum efficiency. The gain of the optical FET detector is maximized if the gap between the source and the drain is small. However, there is a trade-off since this same gap is the optical window of the device, and we want this to be large enough to allow sufficient input light to be detected. The optical

FET is described in further detail in Section 3.5.

Chapter 3 investigates the design and circuit performance of the opto-electronic neuron circuit using two different detectors: the MSM detector because of its simple device structure and uniform response, and the optical FET because of its high responsivity.

2.5 Uniformity

Since the electrical power dissipation is mostly due to LED current, we must be able to work with low currents, hence low optical power from the LED. Consequently, the input light should be designed to be as low as possible. The minimum acceptable light level at the input of each neuron is determined by two factors: the noise level at the input (detector) part of the circuit, and the non-uniformity in the threshold level due to fabrication imperfections. In what follows, we will present a simple statistical analysis that illustrates how the proper input light level can be determined and provides us with an estimate for the maximum neuron density.

We will estimate the minimum acceptable input power level by calculating the probability that a neuron makes an error, P_e, as a function of the optical power levels in the system. As the optical input power is reduced, we eventually reach the noise plateau of the circuit and P_e will increase beyond an acceptable level. We make the assumption that the noise can be modeled as a Gaussian random variable with zero mean and standard deviation σ_n that is added to the signal photocurrent. To calculate P_e we need to statistically characterize the input signal as well. We assume that each element

in the previous layer is on, with probability p and intensity P. The strength of a connection, w_{ij}, is 1 with probability q, and zero with probability $1-q$. The input signal photocurrent, $y_j = \eta_D z_j$, is the sum of C independent random variables. For large C, its distribution can be approximated by a Gaussian due to the central limit theorem[44]. η_D is the detector efficiency in Amperes/Watt. Using Eq. 2.21, we can then calculate the mean, μ_y, and variance, σ_y^2 of the photocurrent as follows:

$$\begin{aligned} \mu_y &= \frac{\eta_D \eta_0}{C} E\{\sum_{i=1}^{C} w_{ij} x_i\} = \eta_D \eta_0 P p q \\ \sigma_y^2 &= (\frac{\eta_D \eta_0}{C})^2 E\{(\sum_{i=1}^{C} w_{ij} x_i)^2\} - \mu_y^2 = \frac{(\eta_D \eta_0 P)^2}{C} pq(1-pq). \end{aligned} \quad (2.25)$$

Error will be made when $t < y < n$ or when $n < y < t$. Since both y and n are random variables, to find all possible errors, we need to integrate over n and y. With these assumptions, P_e can be written as follows:

$$P_e = \frac{1}{2\pi\sigma_n\sigma_y}\Big[\int_t^{\infty} e^{-\frac{(n-t)^2}{2\sigma_n^2}} \int_t^{n} e^{-\frac{(y-\mu_y)^2}{2\sigma_y^2}} dydn + \int_{-\infty}^{t} e^{-\frac{(n-t)^2}{2\sigma_n^2}} \int_n^{t} e^{-\frac{(y-\mu_y)^2}{2\sigma_y^2}} dydn\Big] \quad (2.26)$$

where t is the threshold level for the photocurrent. We can find a closed form solution for Eq. 2.26 for the special case (which incidentally is the worst case) where the threshold, t, is set at the mean of the input distribution, μ_y. In this case, the probability of error is

$$P_e = \frac{1}{\pi} \tan^{-1} \frac{\sigma_n}{\sigma_y}. \quad (2.27)$$

The P_e required by the system is specified by algorithmic considerations, whereas σ_n is affected by the device fabrication process. Given P_e and σ_n, we can either numerically solve Eq. 2.26 or use Eq. 2.27 to determine the necessary σ_y. From Eq. 2.25, we see that with η_0, η_D, p and q given, we can adjust σ_y so that it satisfies the required probability of error, P_e, by selecting the appropriate value for the quotient $P/\sqrt{C}$. The variables N and P are also interrelated by the maximum allowable electrical power dissipation per unit area, P_{max}:

$$P_{max}A = NPV_D/\eta_{LED}, \tag{2.28}$$

where V_D is the power supply voltage in the LED circuit, A is the area of the array and η_{LED} is the LED efficiency in W/A. From Eqs. 2.25,2.27, and 2.28, the maximum density of neuron circuits, N/A, is given by

$$N/A = [\frac{\eta_0\eta_D\eta_{LED}P_{max}}{V\sigma_n\sqrt{C}}\sqrt{pq(1-pq)}\tan(\pi P_e)]. \tag{2.29}$$

For a fully connected feed-forward network, each neuron is connected to all neurons in the previous layer, i.e., C=N. In this case,

$$N/A = [\frac{\eta_0\eta_D\eta_{LED}P_{max}}{V\sigma_n\sqrt{A}}\sqrt{pq(1-pq)}\tan(\pi P_e)]^{2/3}. \tag{2.30}$$

The above equations allow us to determine the maximum density of neurons that can be fabricated with LED circuits given the device limitations (σ_n, P_{max}, V_D, A, η_D, η_0, and η_{LED}) and the algorithmic specifications (P_e, p, and q). As an example, suppose we want to build a network with N=10,000 neurons and C=1000 connections per neuron in an area A=1 cm^2. Suppose

further that η_0 =0.1, η_{LED} =0.01 W/A, η_D =500 A/W, P_{max} =10 W/cm^2, V=2 Volts, $p = q$ =0.5, and P_e =0.1. Then we must have the capability to fabricate the neuron arrays with sufficient uniformity and low enough noise so that $\sigma_n \approx 1\mu$A with a corresponding P=5μW. Recall that Eq (2.30) is for the worse-case scenario where the mean of the inputs is equal to the threshold value. A more realistic distribution would have a bimodal distribution not centered at the threshold value.

2.6 Summary

In this chapter, we have described the basic optoelectronic threshold circuit used to implement the nonlinear response required in an optical neural network, investigated a number of important parameters which determine the neuron density and performance, and have found that not only are electrical power dissipation and optical gain are important, but because of the large scale of circuit integration, uniformity is important as well. Because the operating currents need to be small in order to reduce the electrical power dissipation, we chose to integrate LEDs and MESFETs over laser diodes and bipolar transistors. Chapter 3 describes the design, fabrication, and performance of two different integrations on wafers with epitaxial layers. Chapters 4 and 5 discuss the integration of LEDs using Molecular Beam Epitaxy (MBE) regrowth on GaAs MESFET circuits fabricated by a foundry. This technique takes advantage of the highly uniform ion-implant based MESFET process developed by Vitesse Semiconductor Corp. to fabricate complex custom-designed optoelectronic circuits with high yield and fast turn-around time.

The second half of Chapter 5 discusses some specific optoelectronic neural circuits fabricated using this technique.

Chapter 3

Optoelectronic Circuit Design and Fabrication

In this chapter we describe the design, fabrication, and performance of two different implementations of the optoelectronic neuron threshold circuit described in chapter 2. The first uses MSM (Metal-Semiconductor-Metal) photodetectors, while the second implementation incorporates optical FET detectors.

3.1 Circuit Description

The basic circuit for implementing a thresholding function with optical inputs and optical outputs is shown in Fig. 2.1. The gate voltage, V_g, on the driving MESFET is controlled by the input circuit, consisting of a photodetector acting as an optical input port and a biasing element, which can either be a second photodetector or a transistor. The switching characteristics of the circuit are determined by the I-V characteristics of the photodetector and the biasing element. Figure 3.1a shows the loadline curves for four different light intensities illuminating the photodetector at one particular bias level.

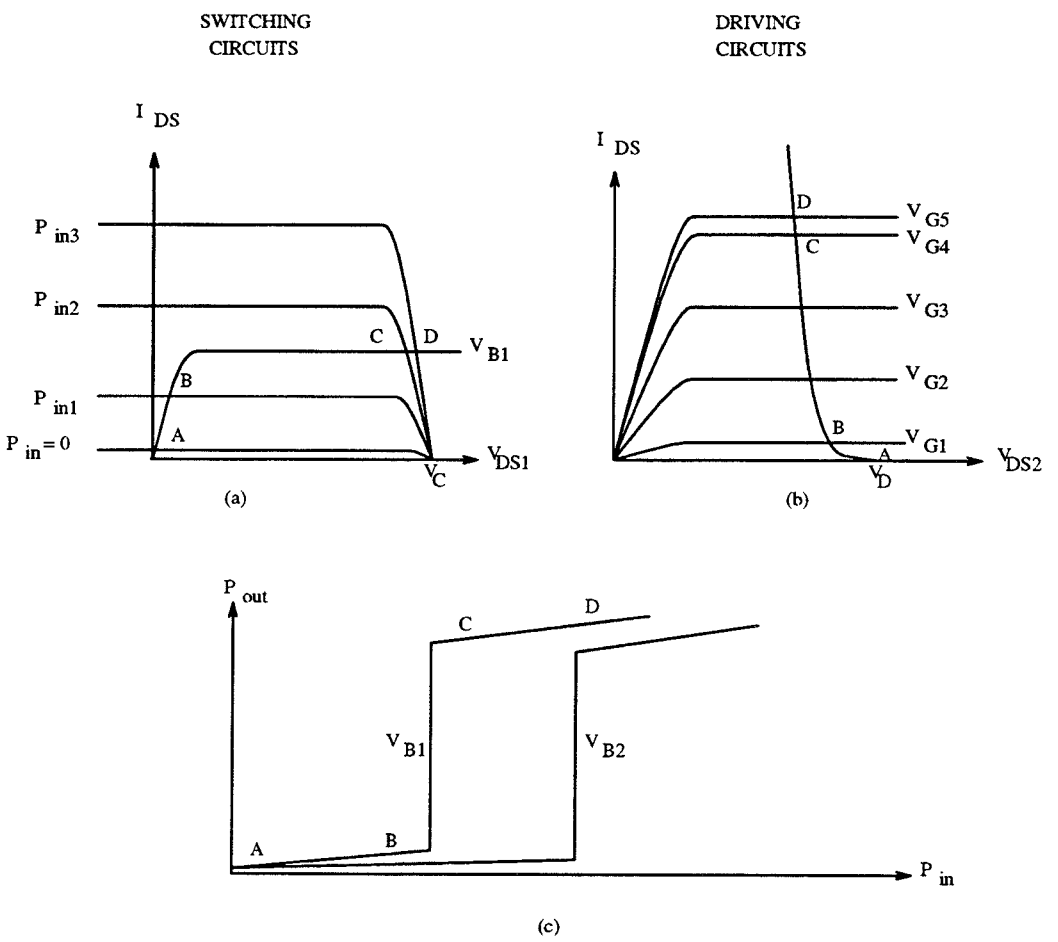


Figure 3.1: Loadline curves for the input branch of the optoelectronic neuron circuit

The intersection point of the I-V curves for the photodetector and for the biasing element determines the node voltage, V_g. When the current in the photodetector exceeds the threshold current set by the biasing element, the node voltage switches from ground to V_{cc} and turns on the driving MESFET. This causes current to flow through the LED and the output light intensity to increase to its high value.

Since the current through the LED is roughly proportional to V_g, the

nonlinear input-output relationship is determined almost exclusively by the input circuit. The sharpness of the threshold function shown in Fig. 3.1c is determined by the relative flatness of the I-V curves of the two input devices in the saturation regime. The threshold becomes sharper as the output impedance of the devices in the saturation regime becomes larger. Specifically, the transition region of the threshold function is approximately

$$\Delta V_g \approx \frac{R_D R_B}{R_D + R_B} \Delta P_{in}, \tag{3.1}$$

where ΔV_g (up to 0.5 Volts) is the voltage swing on the gate of the driving MESFET, R_D and R_B the output impedances of the photodetector and biasing element respectively, and ΔP_{in} the change in the optical input power. The leakage current through the gate of the driving MESFET also affects the switching characteristics of the circuit. The additional current that is drawn through the gate needs to be supplied by extra photocurrent which tends to increase the optical threshold level. The gate-source leakage current that we measure in our MESFETs (using Ti/Pt/Au Schottky contacts) is between 1 and 100 nA for gate voltages up to 0.5 Volt. From our discussion in Sec. 2.5, noise considerations dictate the minimum workable photocurrent to be several μA. The gate-source leakage current becomes the limiting factor for circuits with low detector efficiency and high leakage currents.

In most neural network implementations the neuron outputs and/or the weights are bipolar. Since the LEDs are incoherent light sources, only positive values can be directly implemented with these circuits. In most cases, it is possible to work with unipolar neuron activation functions. But it is necessary to have bipolar weights[48, 21]. There are two ways for representing

bipolar signals in an incoherent system. The first method is to add a constant bias to all the bipolar weights before they are recorded in the optical system. In this case, the input signal to each neuron is a positive quantity with the desired bipolar signal riding on a bias. In our circuits, the control signal (either optical or electronic) on the biasing element, adjusts the threshold of the circuit.

The second method for representing bipolar signals consists of spatially separating the recorded positive and negative weights. The inner products between the input vector to the neuron and each of the two sets of weights are formed separately and the results electronically subtracted before thresholding. The circuits we describe can be used in this mode since the biasing element can be a photodetector, identical to the input detector. The positive signal, P^+, is routed to the "signal" port and the negative signal, P^-, is routed to the "biasing" port. The gate voltage V_g saturates at V_D (or ground) as $P^+ - P^-$ gets large and positive (or negative). When $P^+ = P^-$, then V_g=$V_D/2$. Therefore, the circuit implements a sigmoidal function on the difference $P^+ - P^-$, as desired.

3.2 LED Fabrication

The basic structure of a double heterostructure GaAs light emitting diode is shown in Figure 3.2. The active layer is the middle undoped GaAs layer. Surrounding the active layer are two $Al_{0.3}Ga_{0.7}As$ layers. Because the band gap energy for these $Al_{0.3}Ga_{0.7}As$ layers is higher than GaAs, the two AlGaAs layers help confine the electrons and holes to the active layer so that recom-

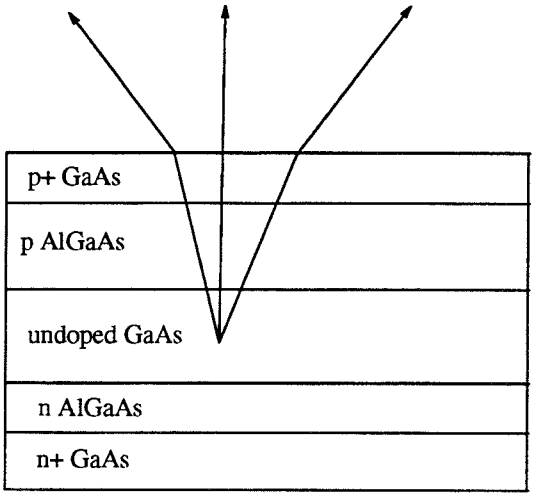


Figure 3.2: Epitaxial structure for a double heterostructure GaAs/AlGaAs LED

bination will be radiative. The outer n^+ and p^+ GaAs layers are needed to make good ohmic contact to the device. Light is generated at the n-AlGaAs/undoped GaAs interface.

The efficiency of the LED is determined by the ratio of the radiative recombination rate, (τ_r^{-1}), to the overall recombination rate, (τ^{-1}). The internal quantum efficiency (the number of photons produced from the forward biased junction current ,I_r) is given by

$$\eta_q = \frac{P}{I_r} = \frac{h\nu}{q}\eta_{DH}\frac{\tau}{\tau_r} \tag{3.2}$$

where $h\nu$ is the energy of an emitted photon, q is the electron charge, and η_{DH} a factor which depends on the LED active region thickness and doping concentration as well as the parameters of the material such as diffusion length and absorption length [30]. τ includes both radiative and nonradiative recombination in the active region. The nonradiative recombination occurs at the GaAs/AlGaAs interfaces due to deep level traps or defects. To determine

the external efficiency (how much light is emitted from the LED), we must include the surface recombination current and the effect of the GaAs/air interface.

Because of the large index of refraction (n=3.3) of GaAs, most of the light generated does not escape the device. The critical angle at the GaAs/air interface is 16.7°. Thus the highest external efficiency achievable is only 2% even if the internal quantum efficiency is 100% [56]. The surface recombination current, I_s, is due to defects and impurities at the surface of the device and depends on the perimeter of the device geometry as well as the device processing. The external LED efficiency can be expressed as

$$\eta = \frac{\tau}{\tau_r}\frac{h\nu}{q}\eta_{esc}\frac{I_r}{I_r + I_s} \tag{3.3}$$

where η_{esc} is the fraction of photons escaping the device.

The overall recombination rate in the active region is given as

$$\tau^{-1} = \tau_{nr}^{-1} + \tau_r^{-1} + \frac{2s}{w} \approx \tau_r^{-1} + \frac{2s}{w} \tag{3.4}$$

where s is the heterojunction interface recombination velocity and w the thickness of the active layer. Typically the nonradiative recombination time, τ_{nr}, is much longer than τ_r or $\frac{2s}{w}$ so it can be neglected. The radiative recombination lifetime is given as

$$\tau_r = \frac{qw(-N_A + \sqrt{N_A^2 + \frac{4J}{qwB}}}{2J} \tag{3.5}$$

where N_A is the active layer doping, J the junction current density, and B radiative recombination probability [30]. From the above equations, we see that we should increase the active layer width to reduce the effect of the

interface recombination, and increase the current density by decreasing the device area. Unfortunately we must also consider re-absorption of the light in the active region as w increases. As a result, there exists an optimal thickness for the active region.

The surface recombination current, $I_s = 2\pi r I_{s0} e^{\frac{qV}{2kT}}$, is proportional to the perimeter of the device, while $I_r = \pi r^2 I_{r0} e^{\frac{qV}{kT}}$, is proportional to the area of the device. So in order to reduce the effect of the surface recombination current, we should make the device very large. If the device is very large, the current density will be small and the efficiency low. One method to increase the perimeter and not the current density is to channel the junction current into a small area. This can be accomplished either by ion-implant or by diffusion. In the ion-implant method, the outer area of the device is made nonconducting by high energy proton bombardment. The junction current is then confined to the center of the device, thereby increasing the current density. The other method is to increase the conductivity of the center portion of the LED by Zn diffusion. With this method, the outer area of the LED mesa is masked off with a thin layer of Si_3N_4 (100nm) and the chip is placed in a vacuum sealed ampoule along with small granules of $ZnAs_2$. The ampoule is placed in a furnace at 630° for a few minutes to allow the Zn to diffuse. This diffusion dopes the center of the LED mesa strongly p type thereby directing the current away from the perimeter and into a narrow channel.

The improvement from ion-implantation or Zn diffusion can be seen in the LED L-I plot shown in Figure 3.3. As the current increases so does

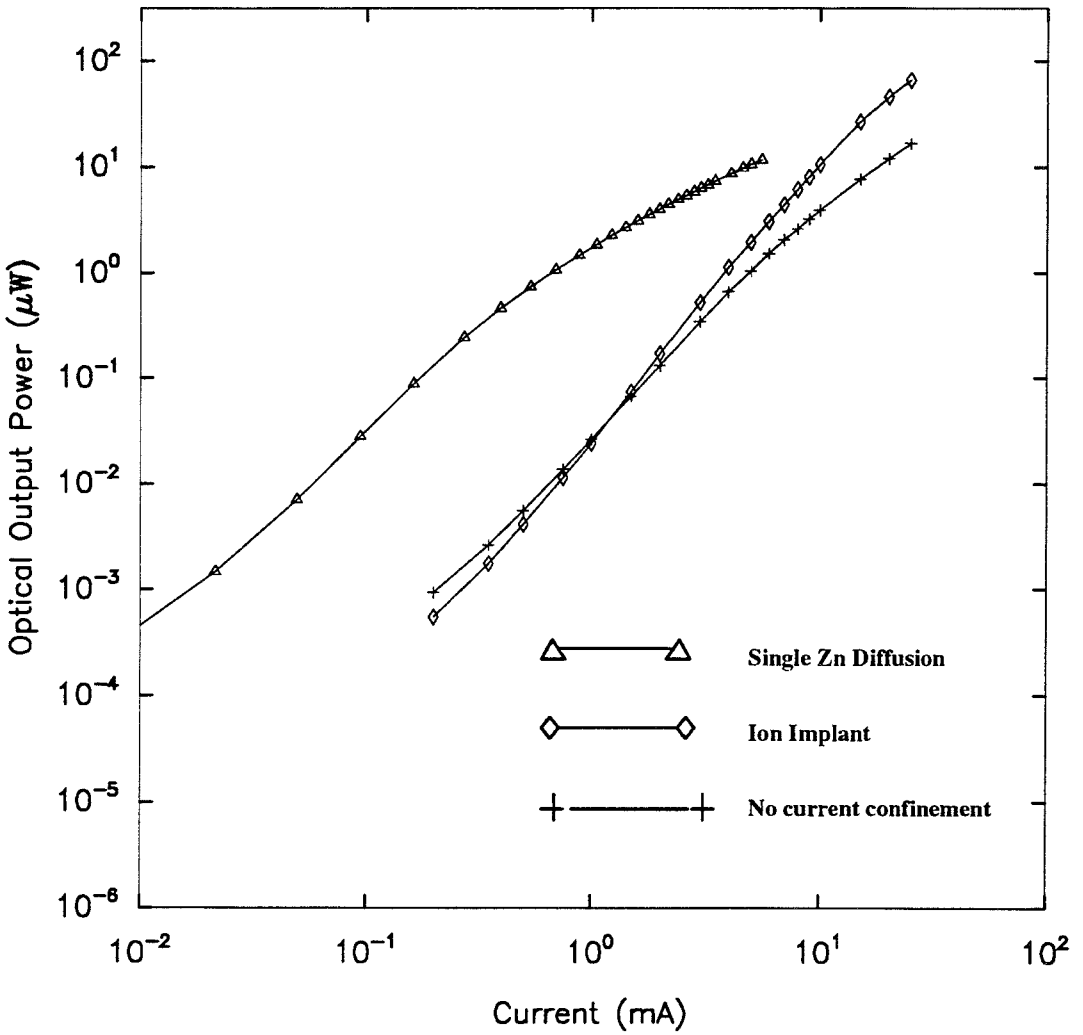


Figure 3.3: Light out versus LED current for different types of double heterostructure LEDs

the efficiency. The highest efficiency at 1mA was 0.001W/A where the LED current was confined by Zn diffusion.

3.3 MESFET Fabrication

Figure 3.4 shows the epilayers for the recessed gate MESFET used in our circuits. The top n^+GaAs layer is added to make ohmic contacts and to reduce the parasitic gate-source resistance. The channel region is etched through the n^+ layer to the n^- layer below it, and the depth of this etch determines the desired MESFET threshold voltage, *i.e.*, a positive threshold voltage for an enhancement-mode MESFET, and a negative threshold voltage for a depletion-mode MESFET.

To fabricate the MESFET, a uniform layer (1000Å) of Si_3N_4 is deposited and then three windows in the silicon nitride are opened with a CF_4 plasma etcher: two for the source and drain ohmic contact regions and one for the MESFET channel region. AuGe/Ni/Au metals are evaporated onto the wafer for the source and drain contacts using a standard lift-off technique for patterning. The ohmic contacts are alloyed at 430°C for 4 minutes. Using the silicon nitride as the mask, a wet chemical etchant, consisting of NH_4OH, H_2O_2, and H_2O (3:1:140), is used to remove the n^+ layer in the gate region and recess the n-channel.

Approximately 50nm of GaAs are removed during each etch step. The exact etch depth at which the channel is pinched off at zero gate bias is determined by periodically examing the I-V characteristics of the FET. Surface states in the channel form a depletion region in the FET. If the channel is

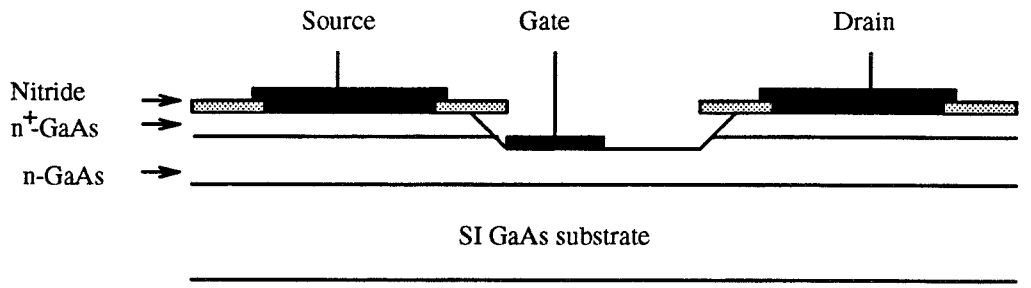


Figure 3.4: Epilayers for a recessed gate MESFET

etched too far, the FET will be pinched off, and it will be impossible to turn on the FET with a small positive gate voltage. Thus, it is crucial to avoid etching too far. Figure 3.5 shows the I-V curve of a MESFET before and after the Schottky gate contact was deposited. The data for the I-V curve for the FET before the gate deposition were taken while the FET was illuminated by a lamp, while I-V curve after the gate deposition was taken with the gate voltage set to 0.4V. Notice that the drain-source current has a much larger saturation voltage before the gate was deposited. After the gate was deposited, the threshold voltage was $\approx$0.1V.

The Si_3N_4 overhang over the recess etch is used as a mask for the gate deposition. By doing so, one can place the gate close to the source and make the gate length slightly smaller than the length of the gate metal deposition. The minimum feature size possible with the Karl Suss MJB3 contact mask aligner is approximately 5μm. By allowing some of the metal to be deposited on the silicon nitride, the MESFET gate length can be made smaller than this minimum feature size.

Guaranteeing that each MESFET contact can be electrically connected to

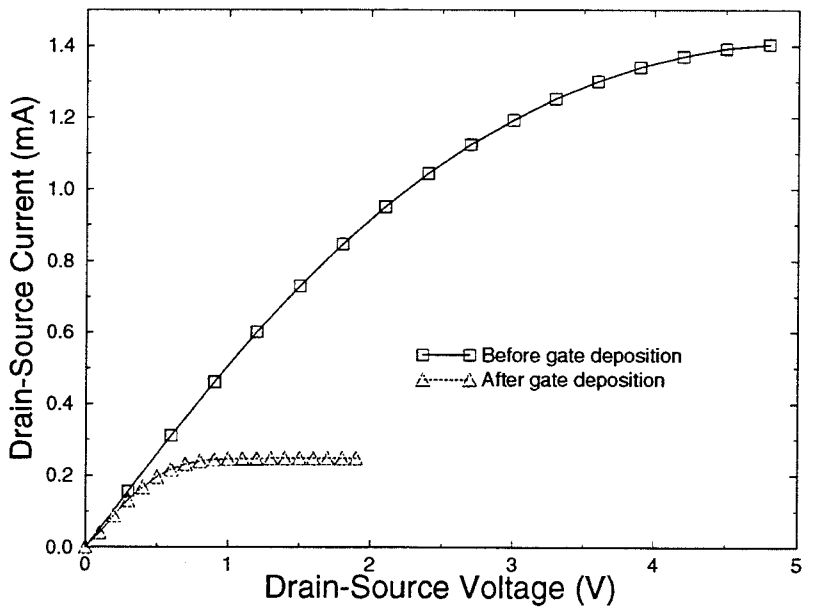


Figure 3.5: IV Curves for MESFET before and after gate deposition

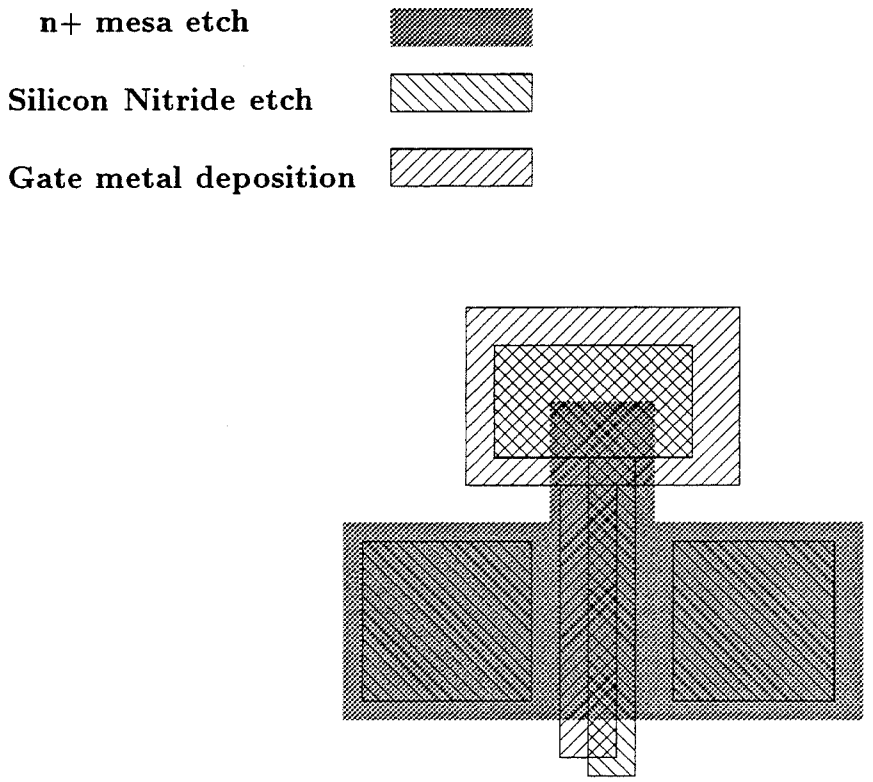


Figure 3.6: Masks for gate-recess MESFET to insure proper step coverage of the gate metal

other devices in the circuit requires special consideration in the mask layout. This is because of undercutting at the sidewalls of the MESFET mesas during wet chemical etching. In the [110] direction, the sidewall profile after etching is dovetailed so that it is easy to provide step coverage for metals from the mesa to the substrate. In the $[1\bar{1}0]$ direction, the undercutting prevents easy step coverage. Because of the gate recess etch a special mask has to be used to insure that the gate metal will be able to connect to other devices. Figure 3.6 shows the layout of the MESFET mesa, the silicon nitride opening, and the gate recess etch masks. Without the gate recess etch mask, silicon nitride would hang over the GaAs and prevent a smooth coverage.

The final step is to evaporate Ti/Pt/Au to form the gate contact in a self-aligned manner with respect to the source. The I-V curves for the FET at several different gate voltages are shown in Figure 3.7. The transconductance of this device at V_g=0.4V is 13mS/mm, which is rather low. There are a number of factors contributing to the low transconductance. One factor is the thin channel thickness required to make an enhancement mode FET. The second factor is the high source resistance due to the deep etch. The transconductance, g_m, is lower by a factor of $\frac{1}{(1+g_m R_s)}$ because of the high source resistance, R_s. Figure 3.8 shows the IV curve of a depletion mode FET with a transconductance of 200mS/mm. The only difference between the two FETs is the channel recess etch depth. For the depletion mode FET, the drain-source current before gate deposition was 4mA without external illumination and with 1V applied across the drain-source.

For the neuron circuits that we are building, the required LED current is less than 1mA per element which can be easily supplied by a single MESFET with a 0.3V swing in the node voltage of the input branch of the circuit. Therefore, a single MESFET is sufficient to drive the LED. Moreover, the transconductance of the MESFET can be easily increased by increasing the gate width if needed. For this reason, MESFETs are excellent candidates as LED drivers.

3.4 MSM-Based Neuron Circuit

The MSM detectors are fabricated by depositing Ti/Pt/Au metal Schottky contacts on the undoped GaAs. This forms two Schottky diodes back to

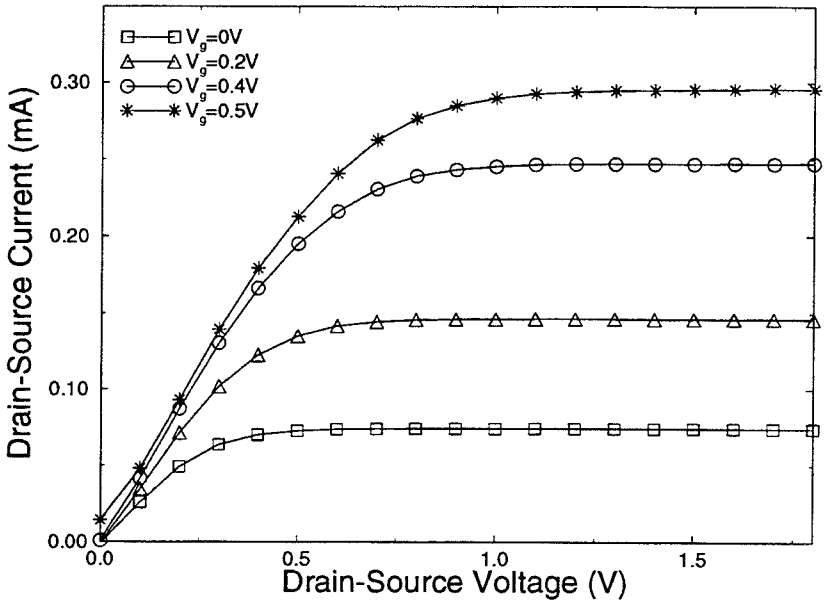


Figure 3.7: IV Curve for enhancement-mode MESFET at different gate voltages

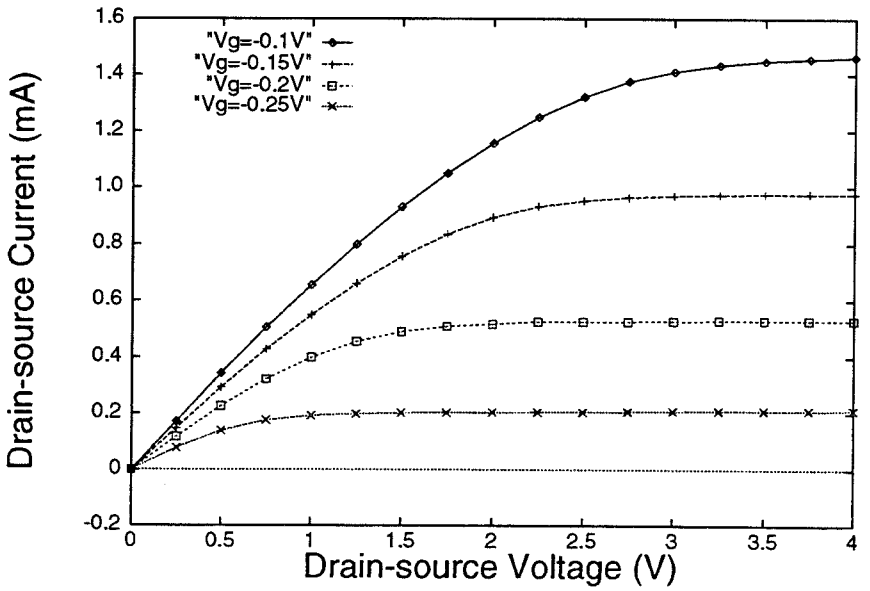


Figure 3.8: IV Curve for depletion-mode MESFET at different gate voltages

back. Optically generated electron-hole pairs from the depletion region of the reverse biased Schottky diode are collected at the electrodes. Therefore, the MSM detector operation is similar to that of a p-i-n diode. As is the case for the p-i-n diode, the external efficiency of the MSM detector cannot be larger than 100%. The MSM detector has the advantage that the only epilayer required is the buffer layer, which is not shared by any other devices in the neuron circuit.

The electrodes are patterned as interdigitated fingers, 4μm wide and 6μm apart with an active area of 40 μm $\times$ 40 μm. With 3V applied to the detector, the measured external efficiency was 0.3A/W. Figure 3.9 shows the I-V curve of an MSM detector under illumination from a laser diode at two different optical intensities. As the voltage increases the current increases as well because the depletion region increases and can therefore collect more carriers.

Figure 3.10 shows the threshold circuit with two MSM photodetectors, one for the optical input signal and the other for the optically controlled bias level. The cross-section of the processed epilayers is shown in Fig. 3.11. To fabricate the circuit, the LED, MESFET and MSM detectors were first defined through a series of wet chemical etches. Then a layer of Si_3N_4 was deposited for surface passivation and insulation. The Si_3N_4 was selectively removed for the MESFET channel region, LED window, and the ohmic contacts. AuGe/Ni/Au was deposited for the n-ohmic contact, followed by a deposition of AuZn/Au for the p-ohmic contact. After deposition, the contacts were alloyed at 430°C. The gate region of the driving MESFET was recessed as described in the previous section so that the MESFET operated

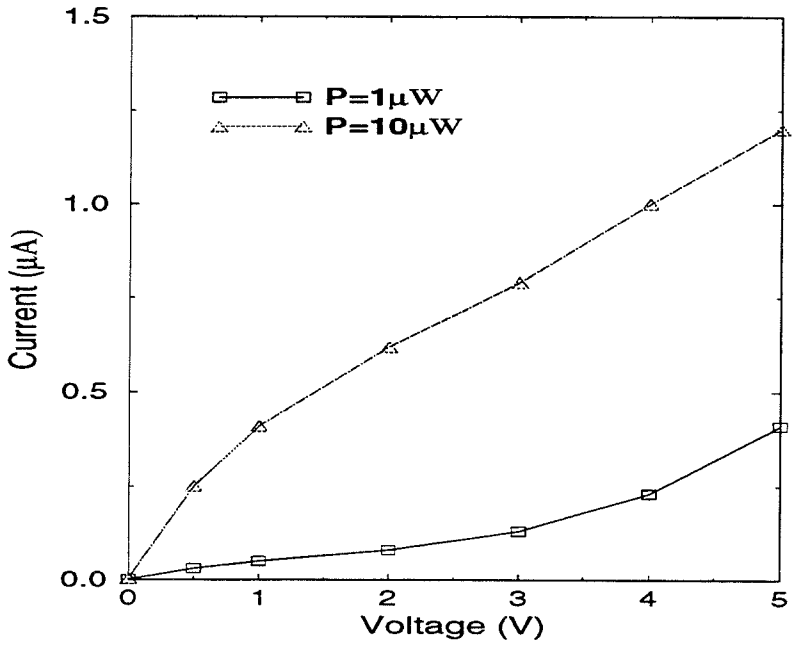


Figure 3.9: IV curve for MSM photodetector at different optical input powers

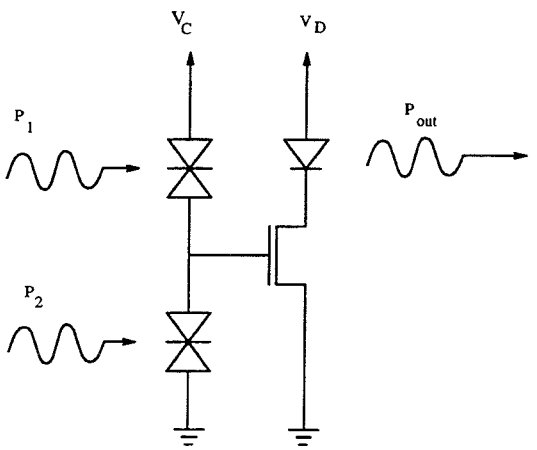


Figure 3.10: Circuit diagram for MSM based optoelectronic circuit

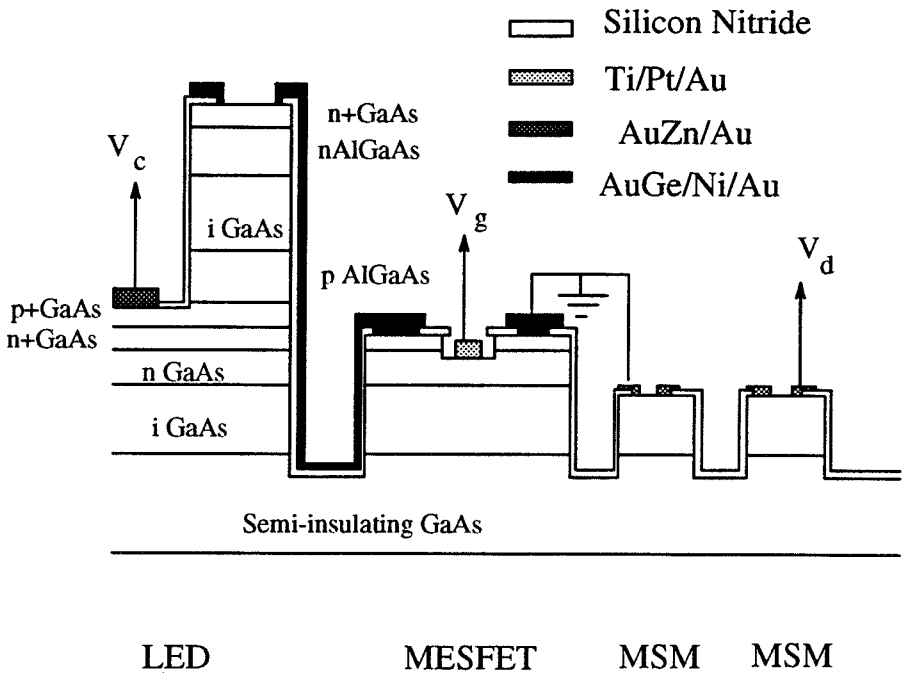


Figure 3.11: Epilayer cross-section of the processed optoelectronic circuit

in the enhancement mode. The entire fabrication process requires nine masking steps. Figure 3.12 shows a photograph of the MSM-based optoelectronic neuron circuit. The LED in this MSM detector based neuron is fabricated directly on a double heterojunction P-i-N structure without the Zn diffusion process. The maximum efficiency obtained was 0.001 W/A due to the lack of current confinement. The size of the gate region was 6x60μm^2, the LED window was 30$\times$30μm^2, and the overall neuron area was 200$\times$150μm^2, including the area for probe pads.

To test the circuit, we measured the output as a function of one of the optical inputs while we held the other input constant. Figure 3.13 shows the results where P1 and P2 are the optical signals as shown in Fig. 3.10.

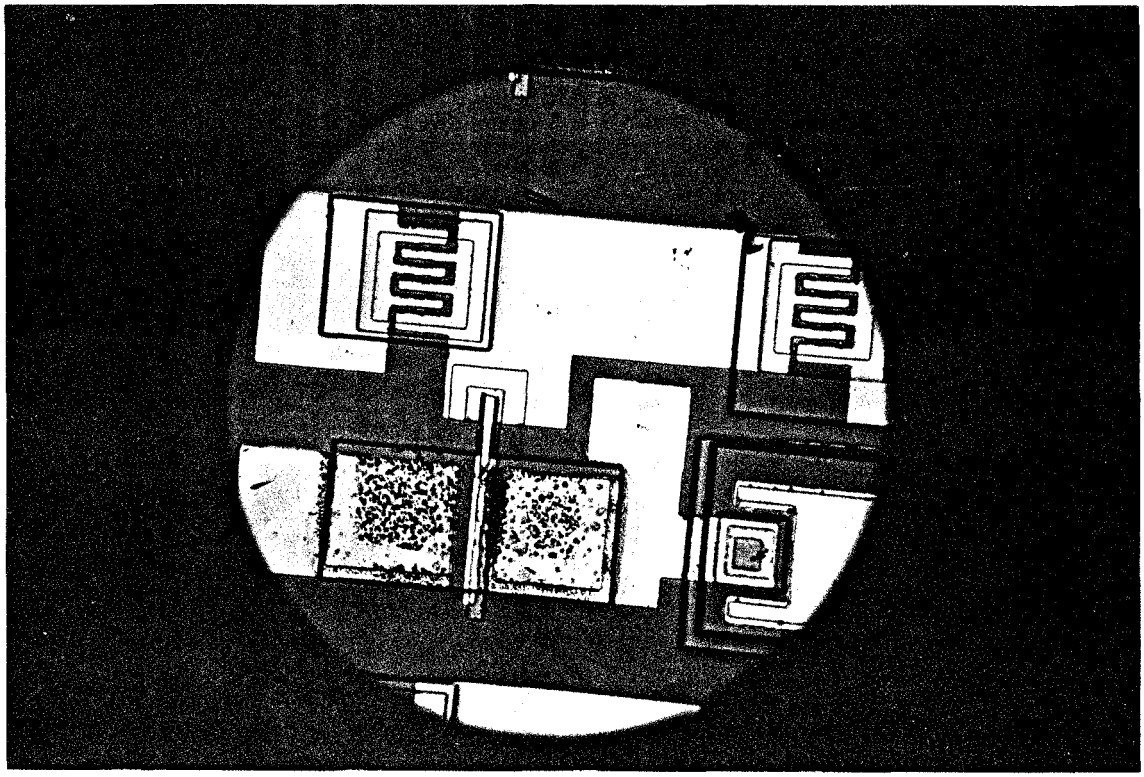


Figure 3.12: Photograph of MSM based optoelectronic threshold circuit

When the two optical input powers are equal, the output light level switches. The differential optical input power, P_{in}, required to turn the LED on, was $0.2\mu W$. The relatively low output current in the circuit is due to the fact that the MESFET channel was etched too far and therefore was an enhancement -mode FET with low transconductance. The reason for the low optical gain is two fold. First, the transconductance of the MESFET was very low, so the output current was small. This can be easily increased by using a depletion mode MESFET which has much higher transconductance instead of the enhancement mode MESFET. This would increase the output current by almost an order of magnitude from 0.2mA to 1.5mA. The other reason for the low optical gain is the low detector responsivity. Because the MESFET required positive gate voltages to turn the device on, the gate source leakage current was rather high. This current had to be supplied by the MSM detectors. By increasing the responsivity of the detectors we can reduce the minimum required input power of the circuit. As we will see in the next section, optical FETs have responsivities on the order of 100-1000A/W which means we should be able to lower the input power to 1-10nW.

3.5 Optical-FET Based Neuron Circuits

One of the disadvantages of the MSM detector is that it does not have gain. Thus the neurons required relatively high optical input intensities (approximately $1\mu W$). In order to increase the density, we need to be able to reduce the optical input light level. This can be accomplished by using a detector, such as the optical FET, that has gain. The optical FET can be easily fab-

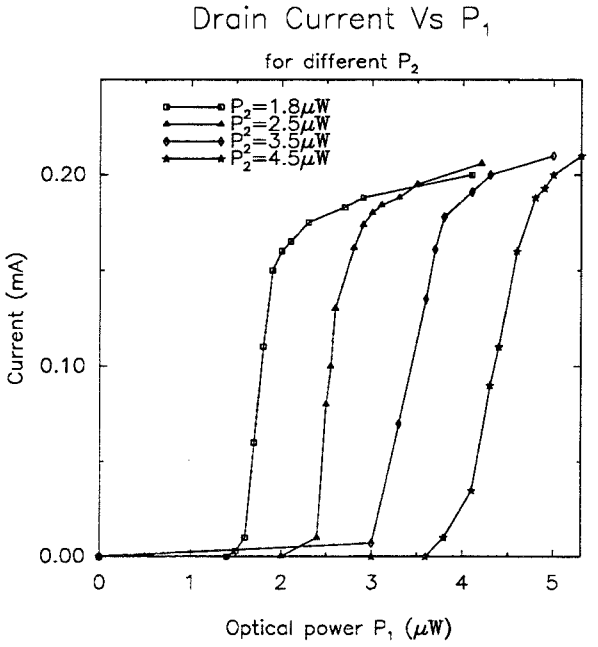


Figure 3.13: Response of the MSM based optoelectronic threshold circuit

ricated in the same epilayers as the MESFET with responsivity as high as 10^4A/W[18].

3.5.1 Optical FET Characteristics

Figure 3.14 shows the cross sectional structure of an optical FET. Since it is very similar to the conventional MESFET, its fabrication is identical to that of a MESFET, except the gate metalization is not defined. The channel thickness, determined by the recessed etch, controls the sensitivity and the dark current. The thinner the channel is the lower the dark current will be. At the same time the sensitivity will decrease with decreasing channel thickness, because less photons are absorbed. So there is an optimal channel thickness depending on how much dark current can be tolerated and how much gain is required.

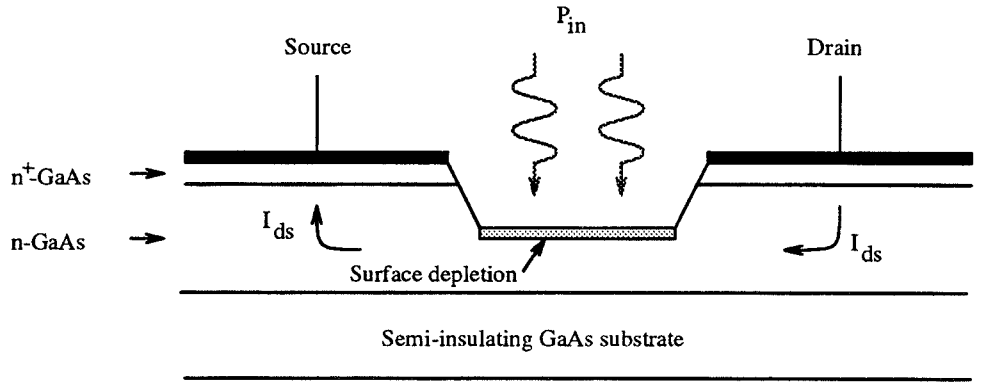


Figure 3.14: Cross-section of a recessed channel optical FET photodetector

There are two mechanisms for optical gain in this device. The first is the photoconductor gain, as described in section 1.3.5 and the other mechanism is a field effect where the channel thickness is modulated by changing the surface state potential. Even without a gate electrode, the channel can be fully depleted if it is thin enough because of the surface states. When the channel is illuminated, some of the electrons trapped at the surface are released lowering the surface potential. This causes the depletion region in the channel to shrink, which allows more electrons to flow from the source to the drain. This is the predominant effect when the dark current is low ($< 1\mu$A) and at low frequencies.

Surface states in GaAs are created because GaAs does not have a native oxide (in fact GaAs forms many oxides such as AsO and GaO), thus atoms at the surface have dangling bonds. These dangling bonds have energy levels in the band gap of the semiconductor and thus act as traps. The trap level is

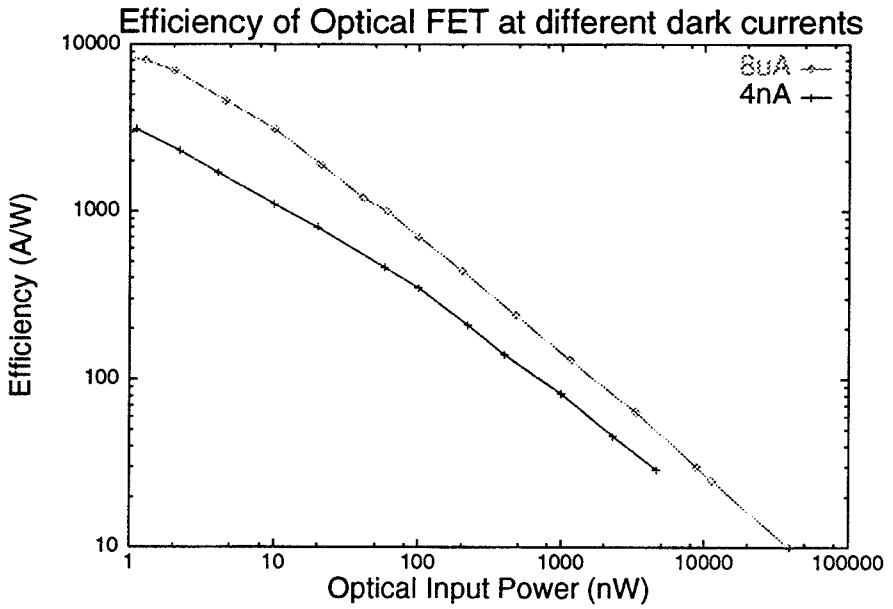


Figure 3.15: Efficiency of a recessed channel optical FET detector at two different dark currents

usually 0.7eV below the conduction band and the density can be quite high. The net effect for the band diagram is that the Fermi level at the surface is fixed or "pinned" at 0.7eV below the conduction band. If the active n-layer of the device is lightly doped, the depletion layer from these traps can be quite large. The surface states in GaAs are typically deep acceptor traps. Thus, the surface of an n- layer is depleted of majority carriers and only ionized donors remain. To complicate matters, the surface state density is a function of the chemical etches and the method of preparation as well as storage conditions [63].

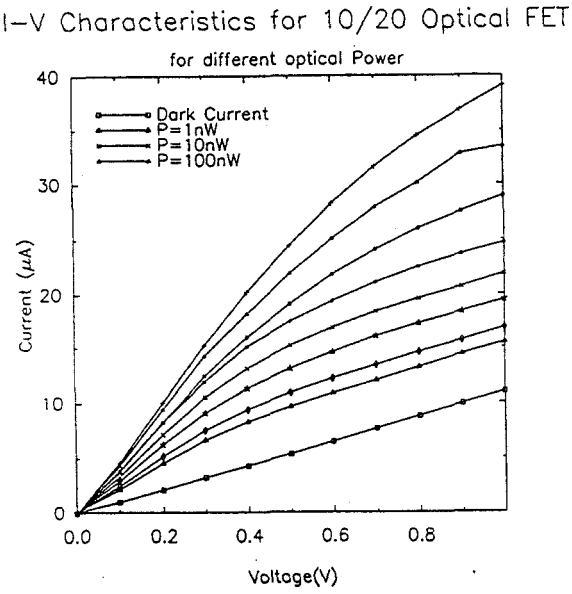
3.5.2 Responsivity of the Optical FET

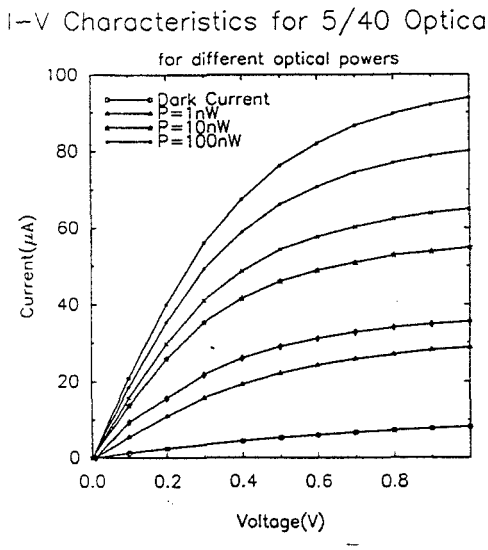
Figure 3.15 shows the measured efficiency as a function of the input optical power for two different dark currents, which corresponds to two different channel thicknesses. To calculate the efficiency, the current due to the incident light, that is the total current minus the dark current for a particular applied voltage, was divided by the incident intensity. The optical source was a collimated AlGaAs/GaAs laser diode, operating at 850nm, which was focused onto the detector with a 6mm focal length lens. Vilcot *et al.* attribute the decrease in gain to the lowered surface state potential which decreases the lifetime of the trapped holes at the surface [58]. As the dark current is reduced, by etching the channel region, the gain decreases. This is due to the decrease in the absorption area as well as the fact the channel becomes more depleted making it more difficult to induce a conducting channel. The responsivity is proportional to the channel width divided by the channel length, but is mostly determined by the lifetime and density of the surface state traps.

3.5.3 I-V Characteristics and Circuit Design Considerations

The photocurrent gain is not the only important parameter in designing circuits with optical FETs. In order to make a sharp threshold function, we need the output conductances and saturation voltages of the FET to be very low. Figure 3.16(a),(b) shows the I-V characteristics for different device geometries and illumination powers.

If the saturation voltage is large, the circuit operates in the resistive region of the FET where the conductance is very high. From Equation (2.1)





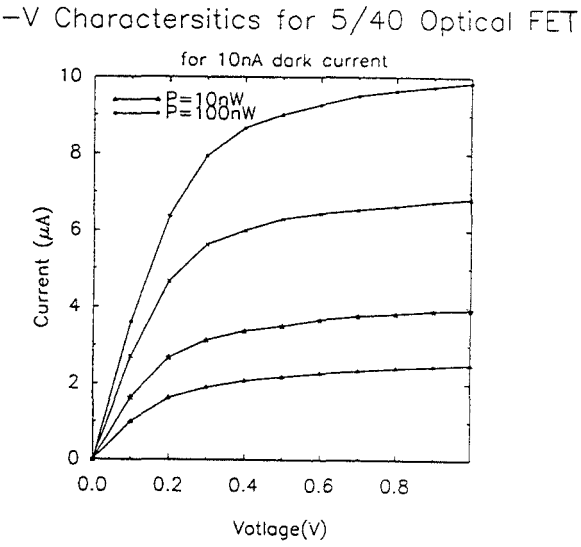


Figure 3.16: I-V characteristics of optical FET detectors with different geometries

$$\Delta V_g = \frac{\Delta I}{(\sigma_1+\sigma_2)} \qquad (2.1)$$

where σ_1 and σ_2 are the conductances of the two photodetectors. If σ_1 is very large, then the change in V_g is small for a given ΔI. For optical FETs the saturation current is proportional to $P^{1/2}$. This means that the node voltage will not saturate very quickly. We can enhance the thresholding characteristics by setting the threshold voltage of the drive MESFET closer to V_{CC}. From the plots in Figure 3.16, we see that to achieve a sharp thresholding function, the detector must be a narrow rectangle (W>>L). Unfortunately the optical input beam shape is typically circular so there will be a mismatch between the detector geometry and the optical input. Because the drain-source saturation voltage varies linearly with the pinch-off voltage, the saturation voltage decreases as the dark current decreases. So it is possible to fabricate Optical FETs which have high responsivity and which saturate quickly. Figure 3.16(c) shows the I-V characteristics of an optical FET with dimensions 5μm x 40μm and 10nA dark current. Notice that the saturation voltages are much lower, but the responsivity is also smaller.

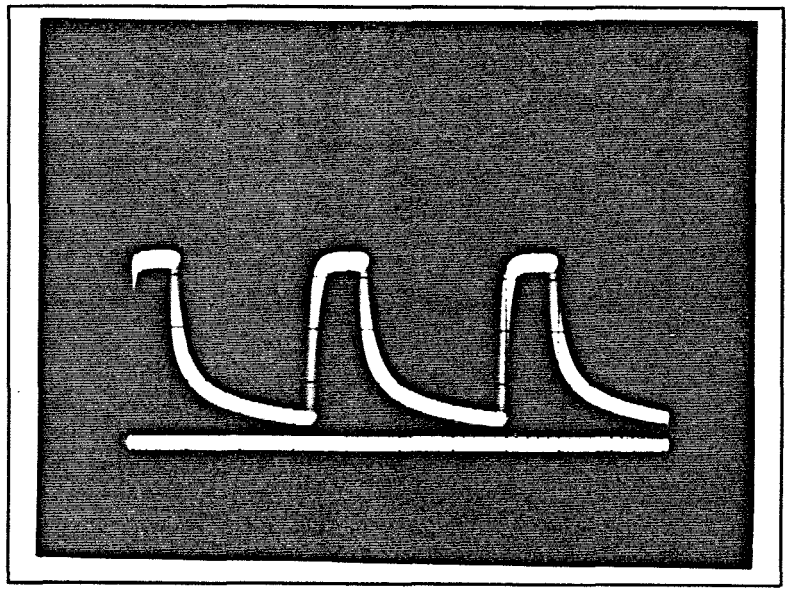
3.5.4 Time Response of Optical FETs

The Optical FET gain depends on the lifetime of the minority carriers. If a hole gets trapped in one of the surface states, its lifetime can be very long. Slow response time means that the figure of merit will be small even if the responsivity of the detectors is large. Figure 3.17(a) shows the photocurrent of a recessed channel optical FET when an optical pulse is applied. Notice that the rise time is very fast but the fall time is quite slow. This is due to the

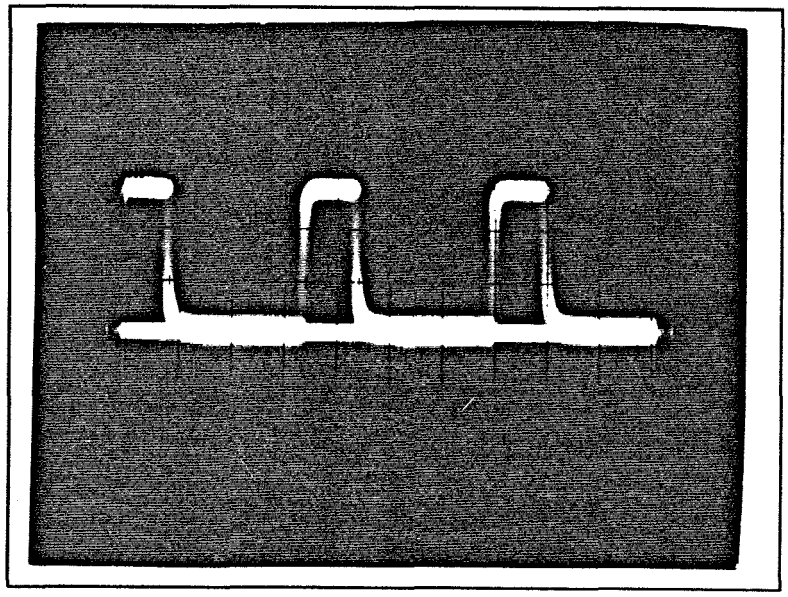
long lifetime of the traps. In figure 3.17(b) the optical FET is illuminated with a low level background light source to keep all the slow traps filled. When we apply an optical pulse in addition to the background light, the fall time is much faster. The disadvantage of having a background illumination to keep the slow traps occupied is that the dark current increases and the responsivity decreases.

3.5.5 Fabrication of Optical FET-based Neuron Circuit

The fabricational steps incorporating the optical FET as the two photodetectors are similar to those of the MSM based neuron circuit. The only difference is the definition of the optical FET. The complete fabrication process required nine masking steps as shown in the cross-section view of the circuit in Fig. 3.18. The first two steps are wet chemical etches to define the LED mesas (etch to n+ MESFET layer) and to define the MESFET and optical FETs areas (etch to substrate). After the wet etches, 100nm of silicon nitride is deposited using CVD (chemical vapor deposition) at 610°C. The silicon nitride is removed for the ohmic contacts and the gate recess in the MESFETs and detectors. After the ohmic contacts are evaporated and patterned using lift-off, the MESFET channel is recessed as described earlier. Even though the MESFETs and the optical FETs share the same epilayers, the recess etch for each device was performed separately to insure that the MESFET is correctly pinched off and that the optical FET has the proper dark current. The MESFET channel was etched so that its threshold voltage was negative. The IV characteristics of the depletion mode MESFET were



(a) Without background illumination 0.1msec/div 0.1V/div



(b) With background illumination 0.1msec/div 0.05V/div

Figure 3.17: Step Response of Optical FET with and without background illumination

shown in section 3.2. Figure 3.19 shows the switching characteristics of the optical FET based neuron circuit. On one of the detectors the optical input power was fixed at 10nW while the optical power on the other detector varied. Notice that the output LED current starts to sharply increase when optical input power exceed 10nW. The reduction in the minimum light required to switch the circuit is due to the high responsivity of the optical FETs as compared to the MSM detectors. The increase in the output current is due to the higher transconductance of the depletion-mode FET as compared to the enhancement mode FET used in the MSM based circuit. A photograph of the detector/FET portion of the circuit is shown in Figure 3.20. The dimensions of the optical FETs are L=5μm and W=40μm. The dimensions of the MESFET are 5μmx60μm. The major drawback of this circuit is the nonuniformity in the MESFET and detectors, due to the deep etch required to reach the n+ layer. Although there are several improvements in the design and processing which can be made, uniformity is always a major issue when dealing with recessed channel FETs.

3.5.6 Possible Improvements in Design

When we consider a large two-dimensional array, nonuniformity from device to device becomes an important consideration. The material structure for the complete circuit has the epilayers for the LED on top of the MESFET structure described above. Therefore we need to etch through 2.55μm of material just to reach the n^+ layer of the MESFET. This deep etch introduces nonuniformity in the MESFET channel thickness which in turn produces gain

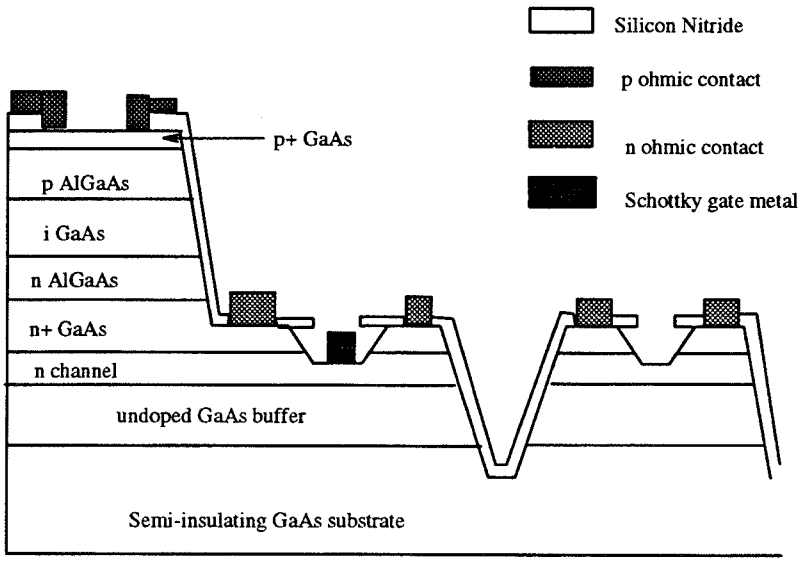


Figure 3.18: Cross-section of processed epiwafer for the optoelectronic threshold circuit integrating optical FET photodetectors

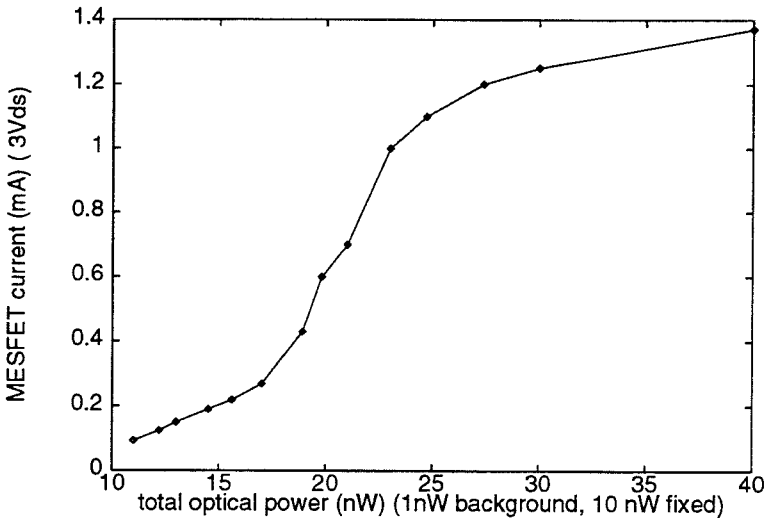


Figure 3.19: Thresholding curve for Optical FET based optoelectronic neuron function

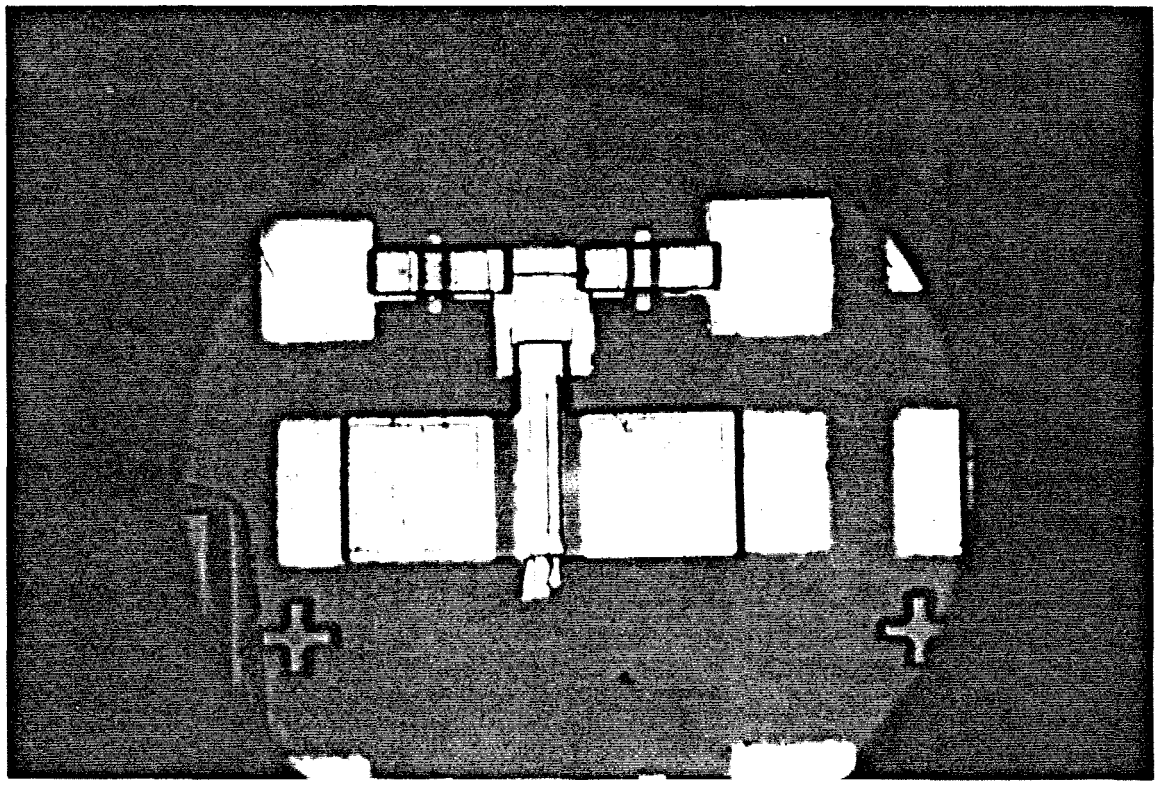


Figure 3.20: Photograph of the Optical FET-based threshold circuit

variations. This can be improved by more carefully controlling the etch, or by inserting an AlAs stop-etch epilayer above the MESFET structure[26]. The n+ AlAs is sandwiched in between two n+ GaAs layers which form the ohmic source and drain contacts for the MESFET. The bottom n+ GaAs layer is needed in order to make a good ohmic contact. Because of the large band offsets between AlAs and n GaAs, it is not possible to make an ohmic contact without adding an extra n+ GaAs layer. It is important to make the bottom n+ GaAs as thin as possible so that the recess etch is not too big. With the proper ratio of citric acid to hydrogen peroxide, the differential etch rate of GaAs to AlAs can be as high as 100:1. AlAs can be etched with a phosphoric etch or it can be selectively removed with HF. While this method is very effective at uniformly etching down to the n^+ layer, there will still be significant variation in the threshold voltage of the MESFETs due to surface states created during the wet chemical etching process.

Another possible method to improve the uniformity is to place the MESFET/detector structure on top of the LED structure to avoid the deep etch. Figure 3.21 shows the epitaxial structure where the MESFET/detector layers are on top. The undoped AlGaAs layer must be thick enough to isolate the LED layers from the MESFET. If the layer is too thin, the n^+ layer of the LED can act as a backgate to the MESFET.

3.6 Summary

In this chapter, we described how we can monolithically integrate various photonic and electronic devices together to fabricate an optoelectronic

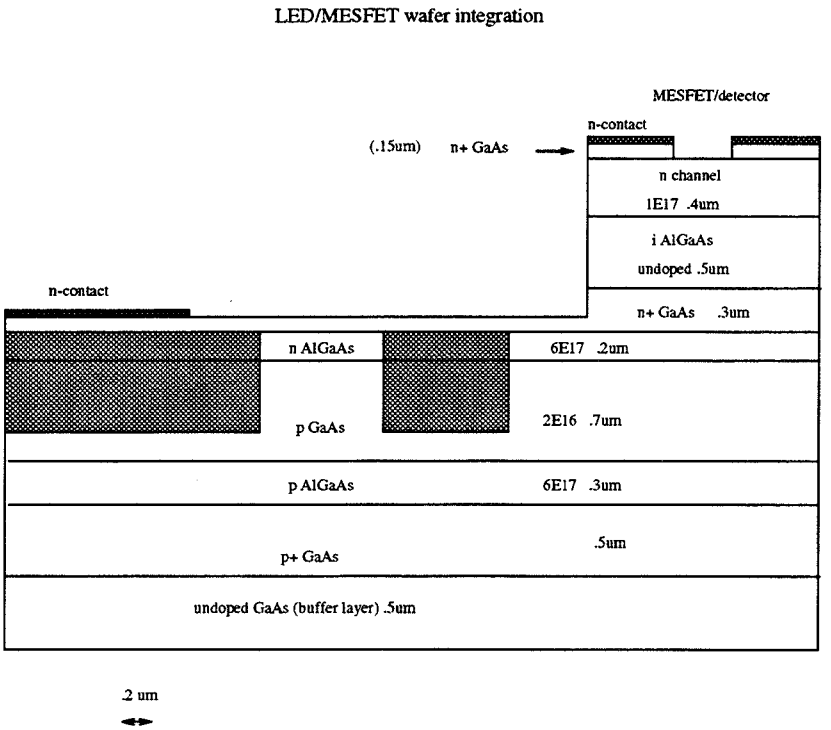


Figure 3.21: Epitaxial structure of an Optoelectronic Neuron Circuit with the MESFET/detector layers on top of the LED

thresholding circuit. The devices are not optimized for individual peak performance, but instead they are designed so that the overall circuit performance is optimized. Two different circuit designs were investigated: one was based on the MSM photodetector and the other one was based on the optical FET photodetector. The advantage of the MSM detector was that it was simple to fabricate and does not share its epilayers with the other devices in the circuit. Unfortunately, the overall circuit performance was poor because of the low responsivity of the MSM. The optical FET on the other hand has very high responsivity which means that the minimum input power required in the optical threshold circuit is very small (10nW). The main difficulty with this detector is the variation in the responsivity due to the wet chemical etching. To achieve the required uniformity for large arrays, we need to look at circuits available from a commercial foundry. The following chapter will describe how LEDs can be integrated with MESFET circuits fabricated by Vitesse Semiconductor Corporation through MOSIS.

Chapter 4

GaAs MESFET Circuits Available Through MOSIS

As we saw in the last chapter, nonuniformity in MESFETs is a major problem in fabricating large arrays of optoelectronic circuits. This nonuniformity arose from the deep etches required to place the gate metal on the channel. Through MOSIS (MOS Integration Service), one can have custom-designed GaAs MESFET circuits fabricated at reasonable cost and turn-around time [39]. The GaAs MESFET circuits available through MOSIS are fabricated by Vitesse Semiconductor Corporation, and are made by doping the substrate of the semi-insulating GaAs substrate using ion-implantation rather than etching mesas in the epitaxial layers. This produces MESFETs with very good uniformity. The circuit components are limited to only electronic devices (MESFETs and Schottky diodes) and photodetectors. It is possible however to grow heterostructures on the processed Vitesse chip by Molecular Beam Epitaxy (MBE)[17].

In this chapter, we describe the Vitesse GaAs MESFET process, the performance of the MESFETs and photodetectors, and the types of analog

optoelectronic circuits which can be fabricated through MOSIS. The next chapter will describe how LEDs can be integrated with the MOSIS chips.

4.1 The Vitesse HGAAS3 Process

Through MOSIS one can receive fully packaged GaAs MESFET circuitry on die sizes up to 15mm $\times$ 15mm for \$450/mm^2. There is currently a MOSIS run every 3 months and it takes usually 8-10 weeks to receive the chips after submission. The HGAAS3 process available through MOSIS includes enhancement-mode (V_T=0.25V) and depletion-mode (V_T=-0.6V) MESFETs, and Schottky diodes. The minimum gate length is 0.6μm.

The fabrication starts out by lightly doping the semi-insulating GaAs substrate p-type by ion-implantation. The depth of this ion-implantation is approximately 1μm. This step ensures that the background doping is uniform and constant from substrate to substrate. GaAs substrates grown by Liquid Encapsulated Czochralski (LEC) contain mid-band gap traps which make the material semi-insulating by pinning the Fermi level near the middle of the band-gap [11]. The density of these traps varies from wafer to wafer and even across a single wafer. Because the concentration of the p doping is much higher than the concentration of the naturally occuring mid-band traps, the nonuniformity in the substrate is suppressed. The disadvantage of the p implant step is that it produces a rather strong backgating effect. This will be discussed in section 4.3.

After the p implant, a thin layer of Si_3N_4 and SiO_2 is deposited on the surface of the substrate. This layer, also known as the field oxide, is then etched

off in the areas specified as transistors to convert the substrate to n-type by Si ion-implant. The first n ion-implant specifies the depletion-mode FETs and a second n ion-implant specifies the enhnacement-mode FETs. The next step is to deposit the gate metal. The gate metal along with the field oxide serve as a mask for the n^+ source and drain ion implants. A tungsten based alloy is used for the gate metal so that it can withstand the high temperature anneal. This produces a self-aligned MESFET process. The depth of the source/drain ion implant, the enhancement-mode MESFET channel, and the depletion mode implant are 600nm, 300nm, and 500nm, respectively. After the source-drain ion implant, a layer of SiN/SiO_2 is deposited to protect the surface during the implant anneal. The anneal is necessary to correct for crystal damage during the ion implantation. The next step is to remove the dielectrics and deposit the ohmic contact in the areas specified. The ohmic metal contact consists of a composition of several metals including nickel but not gold. It is important that the contacts do not contain any gold, because the gold would diffuse into the substrate during the epitaxial regrowth and destroy the electronic circuits. Figure 4.1 shows the different layers in the ion-implant based MESFET. The small dielectric spacers between the gate and the n^+ source/drain implants are artifacts of the field oxide and are needed to increase the gate-drain breakdown voltage.

After the ohmic contacts are deposited, a fairly thick layer of SiO_2 is deposited before the first layer of Aluminum is deposited. Alternating layers of SiO_2 and Aluminum are deposited for the four levels of interconnections. To connect one level of metalization to another, a via in the dielectric is

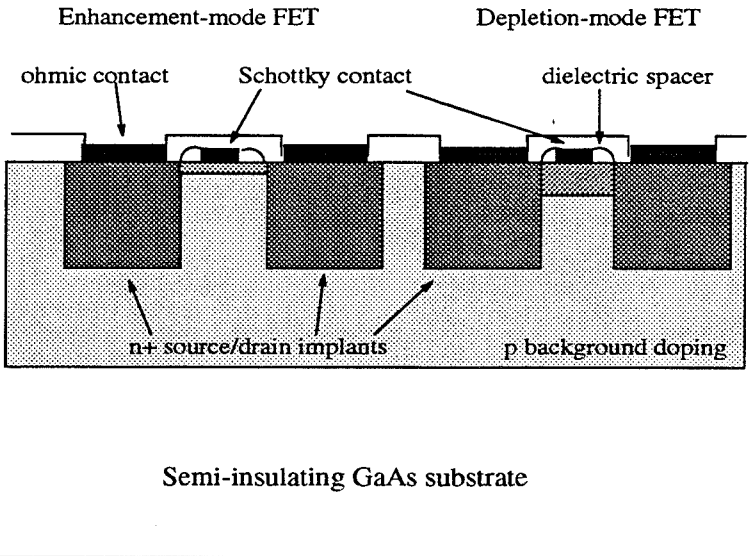


Figure 4.1: Cross-section of the ion-implant based MESFETs in the Vitesse HGAAS3 process

etched. Figure 4.2 shows the cross-section of a processed Vitesse chip. The top layer is a thick layer of SiO_2, called the overglass or passivation layer, which protects the devices and the interconnect metal. The bonding pads consists of overlapping metal 2,3 and 4 and an etch in the overglass layer.

The circuit layout is done using MAGIC with the edgaas3.tech technology file available from MOSIS [20]. Depletion-mode FETs are distinguished from enhancement-mode FETs by depletion ion-implant layer, which specifies an extra Si ion implant to extend the channel thickness. There are two choices for photodetectors in the Vitesse process– either Metal-Semiconductor-Metal (MSM) detectors or optical FET detectors. MSM detectors in the Vitesse process are specified by placing interdigitated gate metal contacts on active area. Unfortunately the efficiency of MSM detectors in the Vitesse process is very small (0.01A/W) because the region where the photons are detected is

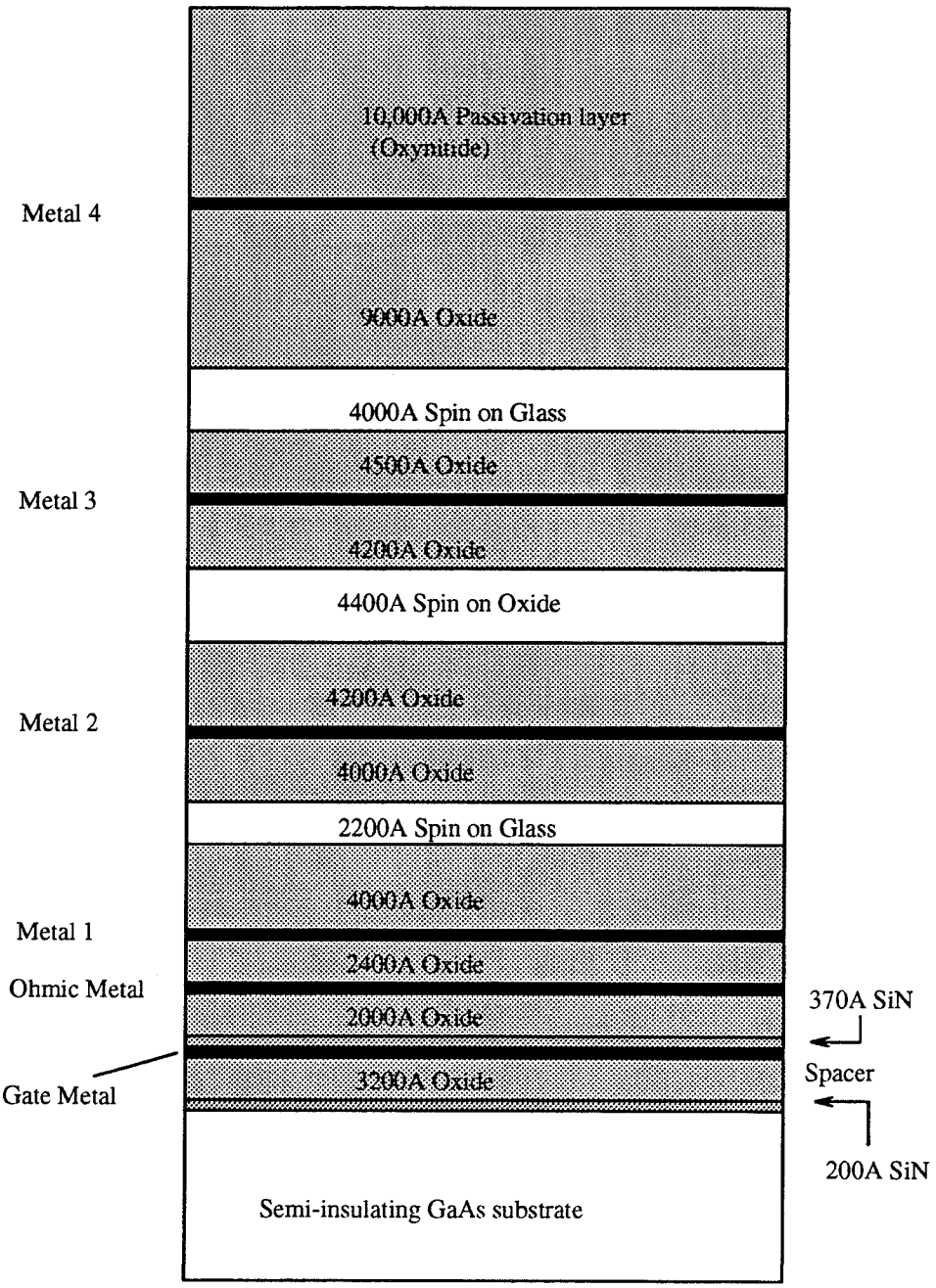


Figure 4.2: Cross-section of Vitesse Chip with 4 levels of Al interconnects

thin and highly doped. For this reason, MSM detectors will not be discussed in this chapter. The optical FET detector is specified as an enhancement-mode MESFET with the gate metal left floating. The design and performance of enhancement mode FETs used as photodetectors is discussed in Section 4.3.

4.2 MESFET Performance

Table 1 shows some of the parameters of the MESFETs fabricated by Vitesse through MOSIS on run N35U. V_T is the threshold voltage for the different transistors. The slight variation in V_T for one type of transistor is due to second-order effects, such as edge effects. The convention used to measure the threshold voltage follows the definition used by Vitesse [59]. The threshold voltage is defined as:

$$V_T = V_{gs}@I_{ds} = 0.6\mu A \times W/L \quad \text{(EFET)} \tag{4.1}$$

$$V_T = V_{gs}@I_{ds} = 0.65\mu A \times W/L \quad \text{(DFET)} \tag{4.2}$$

where the drain-source voltage is fixed at V_{ds}=0.15V. The transconductance, g_m, and the drain-source current, I_{ds}, were measured for eight FETs on different chips from the same run. The transconductance, normalized with respect to the gate width and the drain-source currents are for V_g=0V for the DFETs and V_g=0.4V for the EFETs. Notice that high transconductance does not necessarily indicate high drain-source current. The drain-source currents are considerably smaller for the enhancement mode FETs than for the depletion mode FETs. This is because the EFET gate voltage was not biased well above

	DFET 1/58	DFET 5/58	DFET 20/58	EFET 1/20	EFET 1/40
V_t(V)	-0.733	-0.64	-0.61	0.282	0.304
g_m(mS/mm)	158	49.6	13.8	79	86
g_0(mS/mm)	6.4	0.44	0.27	2.4	0.87
I_{ds}(mA)	5.06	1.03	0.228	0.108	0.271
σ(mA)	0.5 (10%)	0.074 (7%)	0.034 (15%)	0.033 (33%)	0.08 (30%)

Table 4.1: Table of the parameters of the Vitesse Depletion-mode FETs and Enhancement-mode FETs

the threshold voltage due to the forward biased gate source Schottky junction. The gate-source junction forward bias current becomes significant for gate-source voltages above 0.5V. Despite gate-source leakage current, EFETs are useful for implementing Direct Coupled FET Logic (DCFL) where the output voltage of one logic gate circuit is to be directly coupled to the input of another circuit.

The output conductance, g_0, determines how sharp the threshold response will be. The voltage gain of a simple electrical inverter circuit is the ratio of the transconductance over the output conductance. The standard deviation, σ, in the drain-source current for V_g=0V in the DFETs and V_g=0.4V in the EFETs shows the uniformity of the FETs across the run. The uniformity in the Vitesse process is significantly better than in the recessed gate epitaxial MESFETs described in the previous chapter where the yield was one working circuit per chip. The variation in the EFETs is slightly higher than the DFETs because the channel thickness is smaller and therefore the EFET is

more sensitive to the substrate doping.

4.3 Optical FET Response

High responsivity photodetectors can be made using enhancement-mode FETs as photodetectors. The responsivity of ion-implant based MESFET to optical illumination has been studied extensively [41, 7, 61]. The main mechanisms responsible for the photosensitivity of the MESFETs are traps in the substrate, photoconductivity, and the photovoltaic effect if the substrate or gate potentials are not fixed. The geometry of an optical FET photodetector and an enhancement mode FET differs only in the space left between the gate metal and the ohmic source-drain contacts (5-10μm) to absorb more photons. Although most of the absorption happens in the n^+ region or the substrate, adding extra space improves the responsivity. The discussion below details the performance of the optical FET detector available in the Vitesse process.

4.3.1 IV Curves and Responsivity

The I-V characteristics of an optical FET under illumination are quite similar to a normal EFET with a voltage applied to the gate electrode. Figure 4.3 shows the IV curve for an EFET with L_g=1μm and W_g=40μm under illumination from a laser(λ=830nm) diode and with an electrical gate voltage applied. The gate electrode was left floating when the FET was used as a photodetector. The optical input powers are 10nW, and 1μW, and the gate voltages are 0.3V and 0.4V. The dark current of this FET was 10nA. Notice that with only 10nW illuminating the device, the drain-source current is

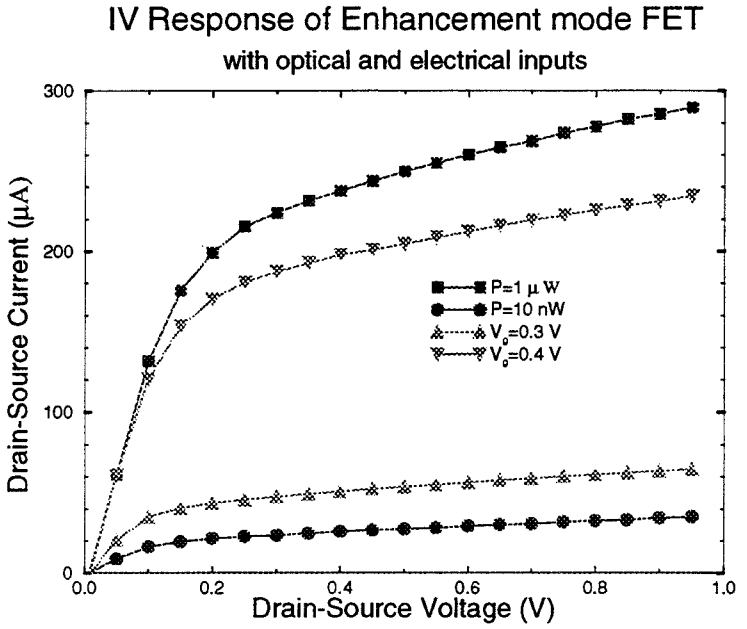


Figure 4.3: I vs V*ds* for EFET on N35U for different optical input and different electrical gate voltages

20μA. This corresponds to a responsivity of 2000A/W.

Figure 4.4 shows the drain-source current of the detector as a function of the optical input intensity on a log-log scale. For the upper curve the gate electrode was left floating while for the lower curve the gate was tied to the source ($V_{gs} = 0V$). The responsivity is not constant but decreases as the optical power increases. Notice that the responsivity is greatly reduced when the gate electrode is tied to the source. To understand the cause for this nonlinear response we must look at the subthreshold characteristics of the enhancement mode MESFET.

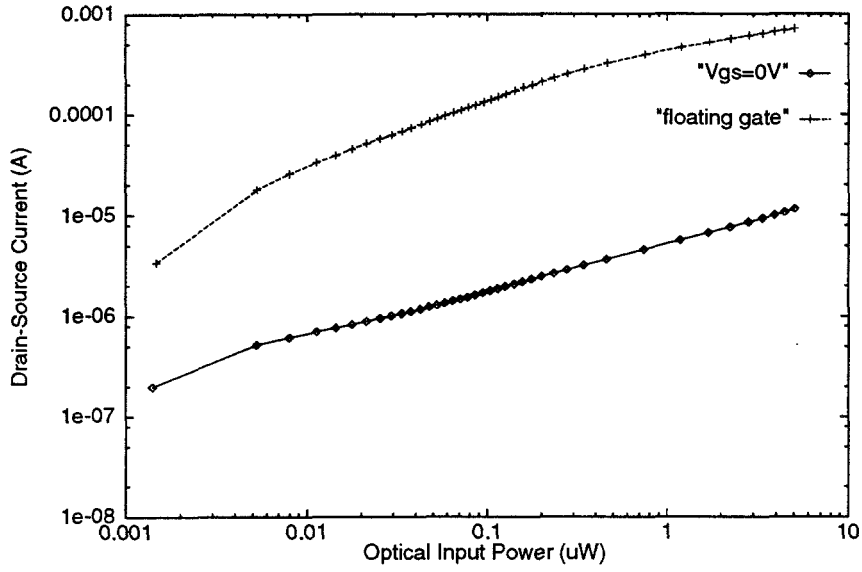
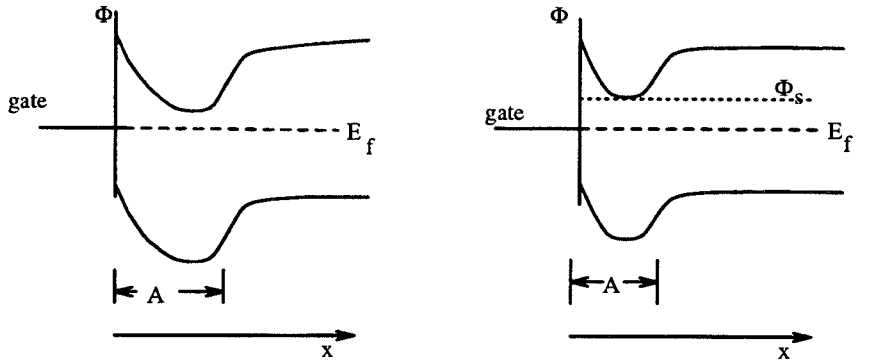


Figure 4.4: Responsivity of EFET N38K fo V_{ds}=0.5V with the gate floating and the gate tied to the source

4.3.2 Subthreshold Response

The subthreshold regime for a FET refers to the condition where the applied gate voltage is less than the threshold voltage for the device. Ideally the drain-source current should be zero because the channel is totally depleted of carriers. In reality a small current will flow due to diffusion of carriers from the source to the drain. The potential barrier that the electrons have to surmount to diffuse through the channel to the drain is determined by the gate potential.

Figure 4.5 shows the band diagram of an enhancement mode MESFET above and below threshold plotted against x, the distance into the substrate from the surface [47]. Above threshold there is a conducting channel, but below threshold, the channel is totally depleted. Electrons from the source



(a) Above threshold (b) Below threshold

Figure 4.5: Band diagram for a MESFET above (a) and below (b) threshold

diffuse through the channel to the drain electrode. The diffusion barrier height, and therefore the current, is determined by the minimum electron potential in the channel, Φ_s. As the gate voltage becomes more positive, the potential barrier is lowered. Because of the p background doping in the substrate, the voltage applied to the gate is divided between the channel and the substrate. Therefore, the change in Φ_s is smaller than the chnage in the applied gate voltage. For small changes in the gate potential we can approximate the change in Φ_s as

$$\Delta\Phi_s = -\kappa V_g \tag{4.3}$$

where κ reflects the effectiveness of the gate electrode to change Φ_s. κ can be expressed in terms of the gate-channel capacitance, C_{gc}, and the channel-substrate capacitance, C_{cb}, as follows [9]

$$\frac{1}{\kappa} = 1 + \frac{C_{gc}}{C_{cb}}. \tag{4.4}$$

As the substrate doping concentration increases the channel-substrate capacitance decreases which lowers κ. In the ideal case where the substrate is undoped, the channel-substrate capacitance is much less than the gate-channel capacitance and therefore κ approaches 1.

The diffusion current is given by

$$I = -wqD\frac{\delta N}{\delta z} = -wqD\frac{N_d - N_s}{l} \tag{4.5}$$

where w is the width of the FET, D the diffusion constant, and N the density of carriers in the channel [36]. Because the diffusion length of the electrons is much longer than the channel length, no carriers recombine, thus the carrier density varies linearly across the channel. N_s and N_d are the carrier densities at the source and drain boundaries. The drain-source current in the subthreshold regime is thus given as

$$I_{ds} = I_0 e^{\frac{q\kappa V_g}{kT}} e^{\frac{-qV_s}{kT}} (1 - e^{\frac{-qV_{ds}}{kT}}) \tag{4.6}$$

where I_0 is a scaling factor which depends on the gate length and width, the electron mobility and the temperature. Typical values for κ for EFETs in the Vitesse process are between 0.5 and 0.7.

When the enhancement-mode FET is illuminated, a positive voltage appears across the channel-substrate junction, because no ohmic contact is made to the substrate. This positive voltage reduces the diffusion potential barrier for the electrons in the source. The open-circuit voltage that appears of the substrate is given by

$$V_{oc} = \frac{kT}{q}\ln(\frac{P_{in}}{P_{th}}) \qquad \text{for} P_{in} >> P_{th} \tag{4.7}$$

where P_{th} is the thermal generation rate in the channel [55]. Thus, the substrate acts as another gate electrode controlling the current through the FET channel. If we substitute the expression for the open-circuit voltage in the subthreshold FET equation, we see that the drain-source current is proportional to P_{in}^{κ}. This derivation corresponds well to experimental data. On the N35U run, $\kappa = 0.5$ for the EFET detectors and as shown in Figure 4.4, the drain-source current is proportional to the square-root of the optical input intensity. If the gate electrode is left floating, the gate voltage will follow the substrate voltage. Thus the FET channel is enhanced from both sides when the gate and substrate are floating. This condition results in the largest photoresponsivity of the optical FET.

Figure 4.6 shows the floating voltage for the electrical gate of the optical FET detector and the voltage of the floating substrate. To measure the potential of the substrate, the chip was placed on an isolated conducting surface, namely the bottom of a 40 pin DIP package, and the voltage was measured with a high impedance voltmeter (Keithley 617).

Because we can modulate the substrate potential as well as the gate potential, we can still detect an optical signal even when the gate voltage is held at a fixed potential. By adjusting the applied gate voltage, we can change the minimum channel potential and thereby change the responsivity of the detector. In other words, the optical responsivity can be thought of as equivalent to the electrical transconductance. In subthreshold, the transconductance varies exponentially with the applied gate voltage. Figure 4.7 shows the drain-source current as a function of gate voltage for different

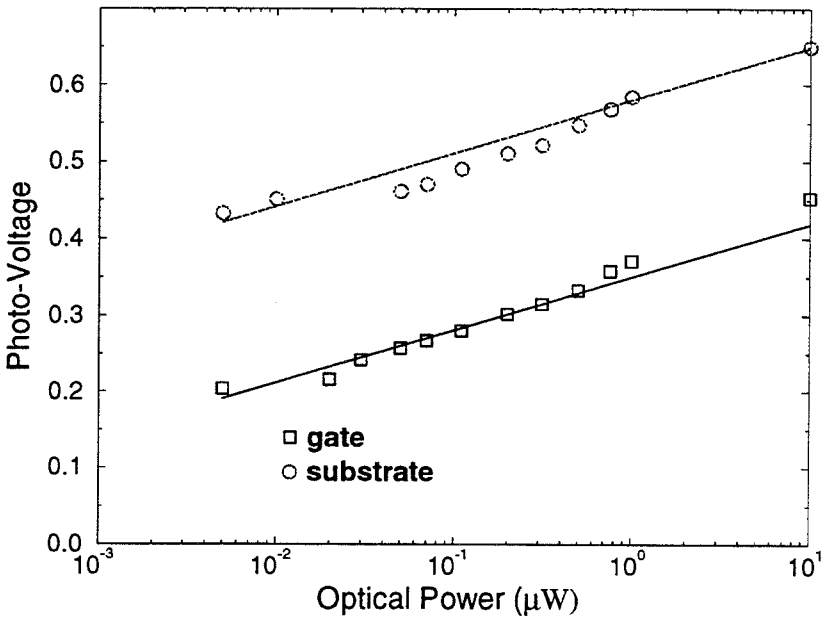


Figure 4.6: Open-circuit voltage for the gate and substrate of an optical FET photodetector as a function of the incident optical power.

optical input powers.

The curves in the figure 4.7 can be fit to the following equation

$$I_{ds} = (4.0 \times 10^{-8} P^{1/2} + 1 \times 10^{-7}) e^{\frac{q\kappa}{kT} V_g}. \tag{4.8}$$

The responsivity of the detector, $\frac{\partial I}{\partial P}$, is given as

$$\frac{\partial I}{\partial P} = \frac{2 \times 10^{-8}}{P^{1/2}} e^{\frac{q\kappa}{kT} V_g}. \tag{4.9}$$

As V_g increases, the responsivity as well as the dark current increases.

4.3.3 Modeling the Optical FET

The I-V characteristics of an optical FET are quite similar to that of a regular MESFET. In fact, from Figure 4.8, one can see that the IV curves for optical illumination (P=0.4μW) and electrical gate voltage (V_g=0.4V)

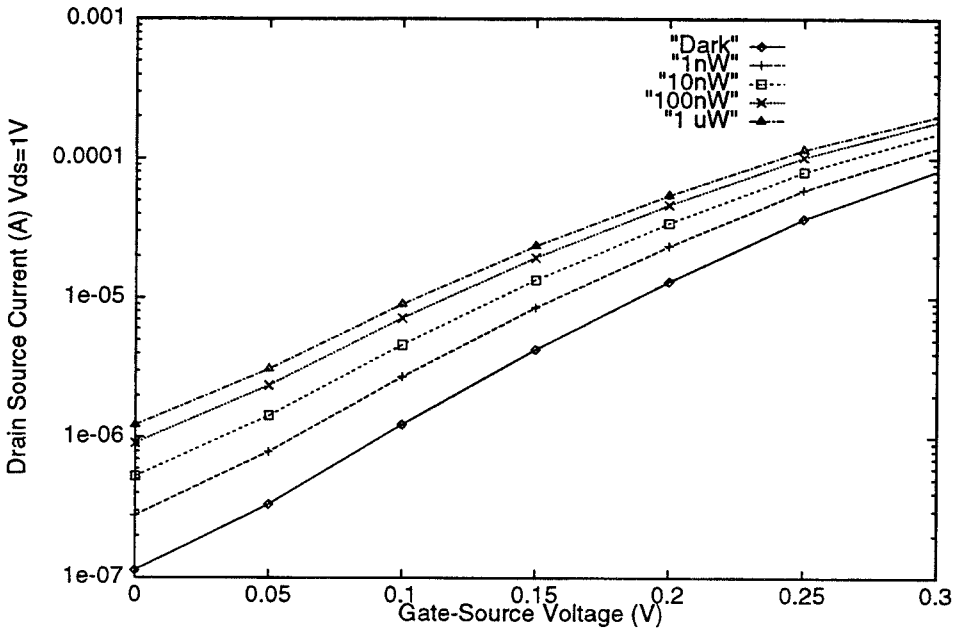


Figure 4.7: Drain-source current vs gate voltage for different light intensities N35U EFET 1/40

are essentially identical. This means that we can model the optical FET as a regular MESFET when simulating circuits. The relationship between the optical input power and the equivalent electrical gate voltage is determined in the following manner. The subthreshold characteristics were measured for an EFET when the FET was in the dark. Then, with the gate floating, the drain-source current was measured as a function of the optical input intensity. By equating the two measurements, a relationship between V_g and P_{in} can be determined.

From experimental data on the EFET photodetectors on run N35U, the following relationship was measured.

$$V_g = \frac{kT}{q} \ln \frac{P_{in}\eta_0}{I_0} \tag{4.10}$$

where P_{in} is expressed in units of W, $\eta_0 = 340A/W$, and $I_0 = 20nA$.

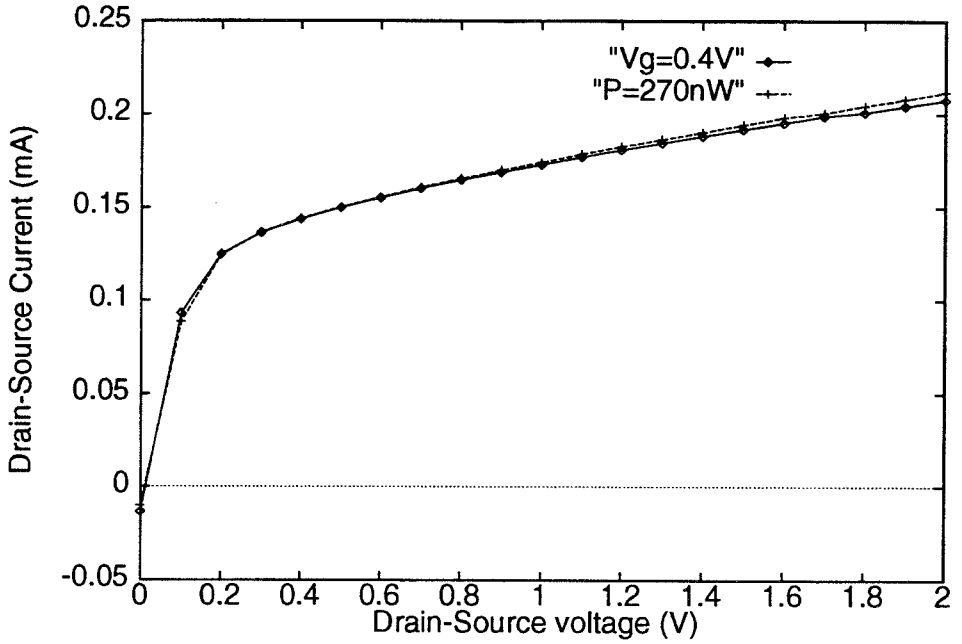


Figure 4.8: Similarity between optical and electrical control over drain-source current on an EFET.

4.3.4 Optical FET Geometry

The drain-source current for the rectangular FET is proportional to the ratio of the gate width to the gate length. For an optical FET detector, the gate voltage for a given optical intensity will be essentially independent of gate width and gate length. So the responsivity is also proportional to W/L, where W is the gate width and L is the gate length. Because the optical beam is typically circular, there is a geometrical mismatch as W/L becomes large. A rectangular FET detector with 10μm space between the gate and the ohmic metals and gate width equal to 40μm collects 60% of the incoming signal if the diameter of the optical beam in 40μm.

It is also possible to make a FET where the gate circles around the drain. The responsivity, shown in figure 4.9 (a), is linear in P. Because the gate

was left floating, the dark current is quite high, 0.9μA. The responsivity is comparable to the rectangular EFET photodetector (see Figure 4.4). Figure 4.9(b) shows the I-V characteristics of a ring-geometry FET. The gate was a rectangular annulus with a width of 1μ and 30μm on each side. The space between the gate and the source was 13μm. The output conductance of the ring FET is rather high. It is possible that as the drain-source voltage increases, the gate voltage increases as well.

4.3.5 Time Response

The time response of the optical FETs on the MOSIS chips was measured by applying a square wave optical pulse to the detector and measuring the photocurrent on the oscilloscope. The gate on the optical FET was left floating in order to have high gain.

To measure the small currents on the oscilloscope, a current sensing amplifier was built. The circuit diagram is shown in figure 4.10. Through the feedback resistor the op-amp forces the negative input to equal the positive input voltage which is the drain-source voltage across the FET. Any current flowing through the FET will come from the output of the op-amp through the feedback resistor. The output voltage will be the current through the optical FET scaled by the resistor. The response of the EFET was compared against the response of a Photodyne detector. The Photodyne detector has a limited frequency response when the gain is high, so the gain was kept low. The photodyne was used to determine the rise and fall times of the laser diode and to make sure that the laser diode switched completely off.

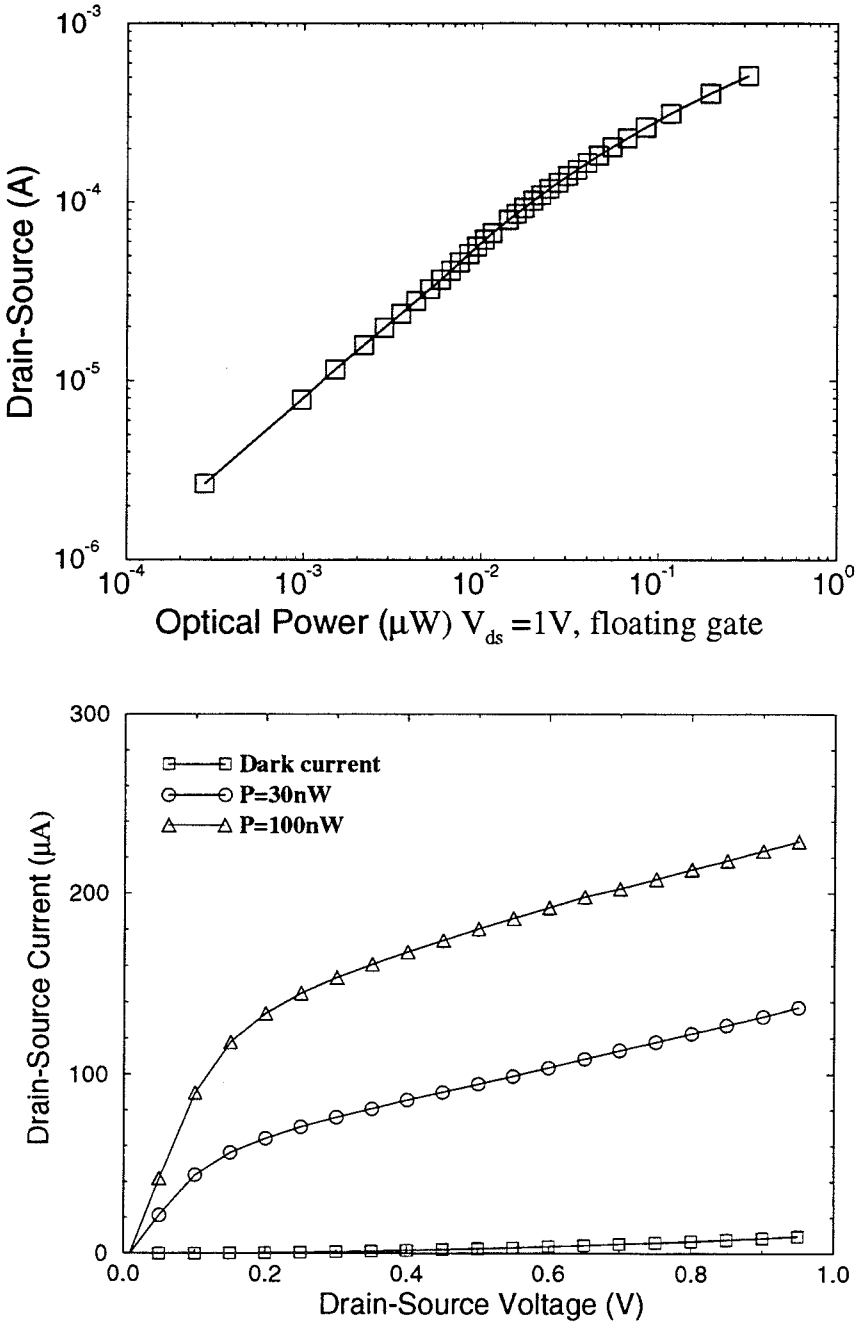


Figure 4.9: (a) Responsivity of ring shaped EFET photodetector. (b) IV Characterisitic of ring shaped EFET photodetector under different illumination intensities

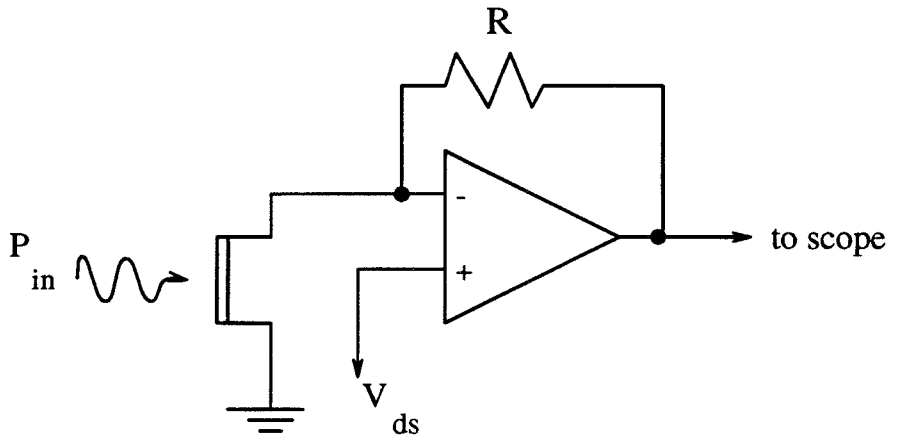


Figure 4.10: Circuit diagram for current sensing amplifier to measure the time response of optical FETs

The slew rate of the 741 op-amp is $2V/\mu s$. For the response curves at high optical powers the gain had to be reduced so that the voltage swing was not too large. Figures 4.11 and 4.12 show the response to high ($40\mu W$) and low (40nW) optical signals. We do not see the long fall times like we saw in the recess-etch optical FETs made on the epi-wafers. The long fall times on the epi-wafer came from deep traps on the surface due to the wet chemical etching and the subsequent chemical reactions to air [42]. Figure 4.13 shows the response when a voltage was applied to the gate. This was done to eliminate the possibility of the probes or the test circuitry causing the slow response. For the 40nW pulse the rise/fall time was approximately $25\mu s$.

The time response is determined by the RC time constant of the GaAs substrate. In order for the drain-source current to change, the substrate potential must change in accordance to the amount of incident light. The capacitance is determined by the depletion width of the channel-substrate junction and the resistance is determined by the available photocurrent in the substrate. It is not possible to directly measure either the capacitance

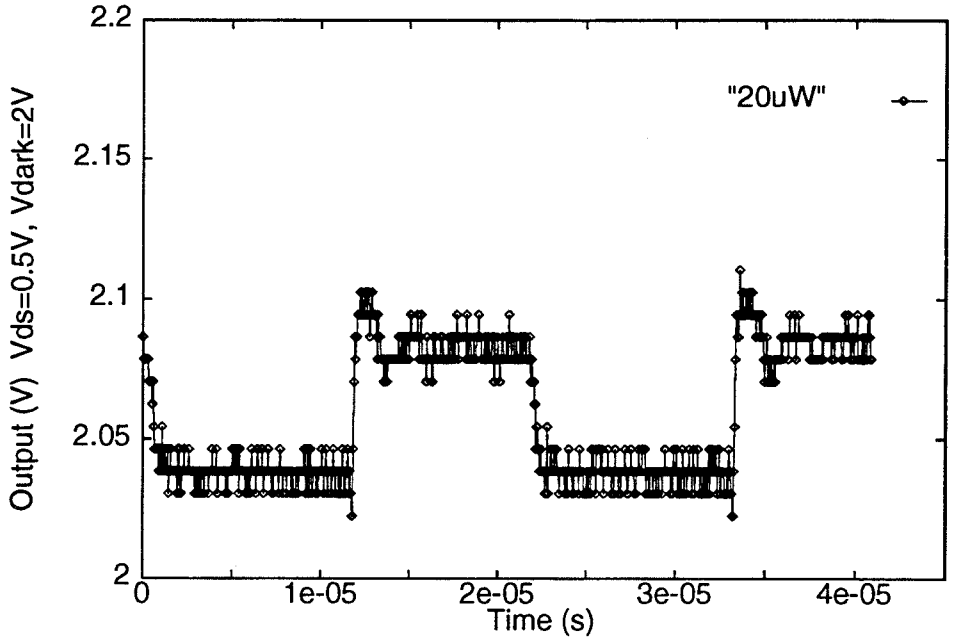


Figure 4.11: Response of an optical FET to a large optical pulse (20μW)

or the photocurrent, because there is no ohmic substrate contact available. If we assume that the responsivity in the substrate is 0.01A/W (from the measurements on the MSM detectors), then the available photocurrent for the an optical input of 40nW is only 0.4nA. The voltage change on the substrate is only a few millivolts (20mV from Figure 4.7) which corresponds to R=500MΩ. The measured switching time was 25μs so the substrate-channel capacitance is 50fF. One way to decrease the capacitance is to increase the background p doping. This will also increase the responsivity of the optical FET. One can also vary the device layout to reduce the total capacitance. The optical FET still responds to optical signals at higher frequencies where the gain mechanism is photoconductivity, but the response is much weaker [57].

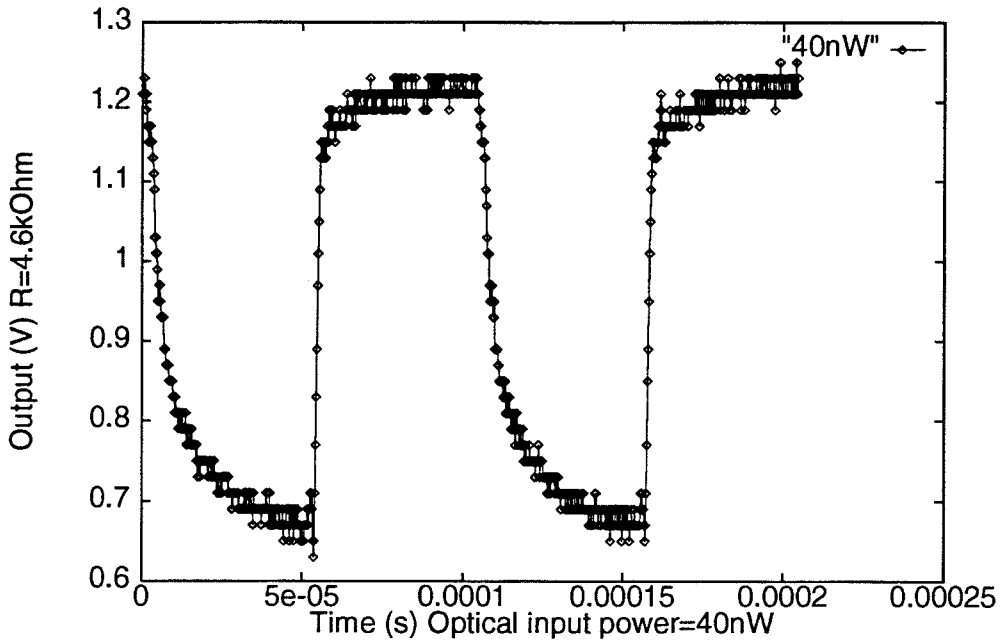


Figure 4.12: Response of an optical FET to a small optical pulse (40nW)

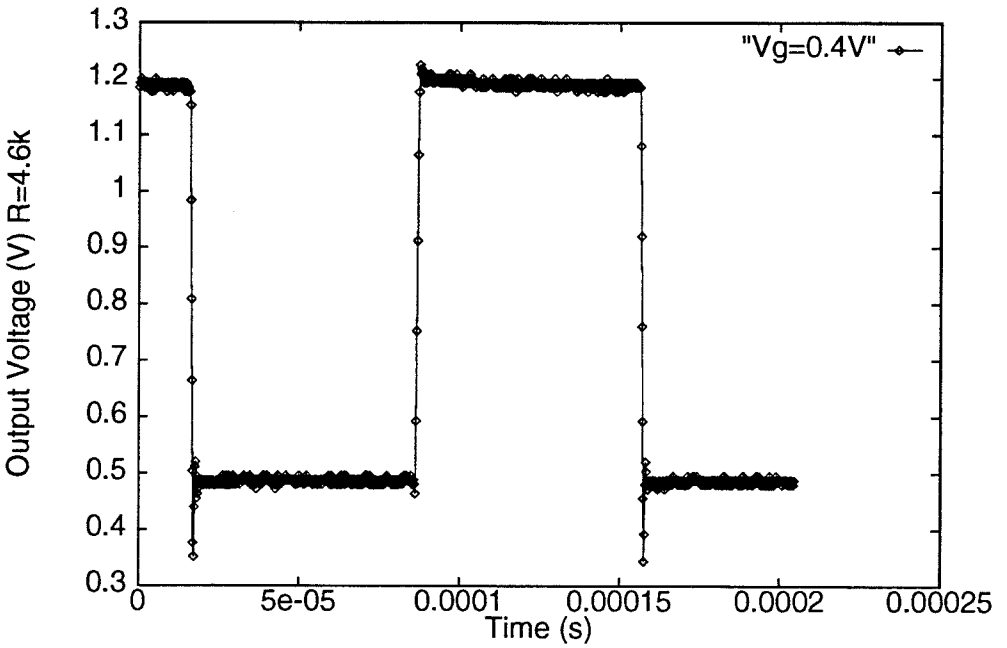


Figure 4.13: Response of an EFET to an applied electrical signal

4.4 Backgating

4.4.1 The Backgating Mechanism

Backgating is a term that refers to the reduction in the channel current of a MESFET due to a voltage applied to the substrate through an ohmic contact, such as a source or drain contact to another MESFET. The effect is only seen when the substrate voltage is less than the source voltage of the MESFET in question. Backgating due to Cr-doped emi-insulating GaAs substrates has been studied quite extensively [28, 5, 29]. The mechanism for backgating in the Vitesse process though is due to the p ion-implnat rather than deep traps and is identical to the mechanism for photoresponsivity in the optical FET. The basic idea is that there is a depletion region at the channel substrate interface. The band diagram for the Vitesse substrate was shown in Figure 4.5. When a negative voltage is applied to the substrate, the depletion region formed at the channel-substrate junction extends further into the n-channel thereby reducing the current through the MESFET. With an p ohmic contact to the substrate, it is difficult to electrically apply a positive voltage to the substrate.

For the MOSIS circuit, the substrate can be considered to be p-doped throughout since the doping is fairly deep. There are no p^+ contacts possible in the MOSIS HGAAS3 process. All substrate contacts are made with a n^+ source/drain contact. When a negative voltage is applied to an n^+ backgate contact, the n^+-p substrate junction is forward biased. Because there is no ohmic contact to the substrate, no current can flow and the substrate potential follows the negative backgate potential. This means that the

substrate-channel junction under the FET will now be reverse biased. This is the mechanism for the backgating in the MOSIS chips. If a positive voltage is applied to the substrate through an n^+ contact, neighboring FETs are not affected. In the SPICE simulations, backgating can be modeled by adjusting the threshold voltage of the MESFET as follows

$$V_t = V_{t0} - K_{bg}(V_s - V_{ss}) \tag{4.11}$$

where V_{ss} is the most negative potential. K_{bg} has been found experimentally to be 0.08 for the first MOSIS run [54]. Because the substrates currents are so small, backgating is not a serious problem at frequencies higher than 10kHz.

4.4.2 DC Effects

Figure 4.14 shows the IV characteristics of an EFET for a fixed gate voltage (V_g=0.34V) but different voltages applied to a backgate electrode. Notice that the current drops by 80% when the backgate voltage is -1V. Positive voltages on the backgate do not affect the EFET. The IV characteristics when a backgate is applied is identical to when a gate voltage is applied except the transconductance of the backgate is smaller. Figure 4.15 shows the normalized drain-source current for a DFET as a function of the backgate voltage for several different gate voltages. Notice that when the FET is operating well above threshold (V_g=0V) the FET is not very sensitive to the backgating voltage. This is because the channel is highly doped and is fairly wide at that gate voltage.

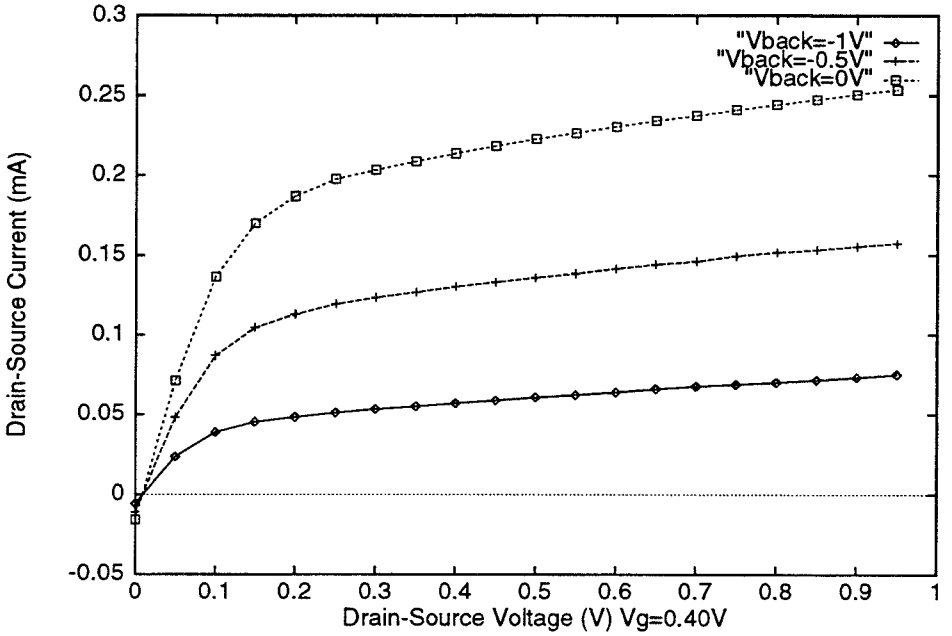


Figure 4.14: IV Characteristics of an EFET for a fixed gate voltage but different voltages applied to the backgate. V_g=0.4V

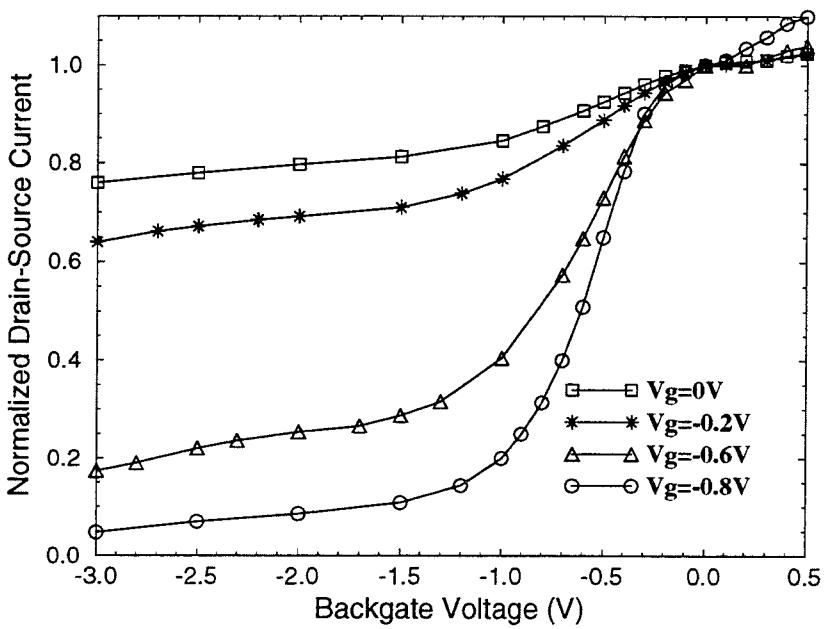


Figure 4.15: Normalized Drain-Source current for DFET for different gate voltages as a function of backgating voltage

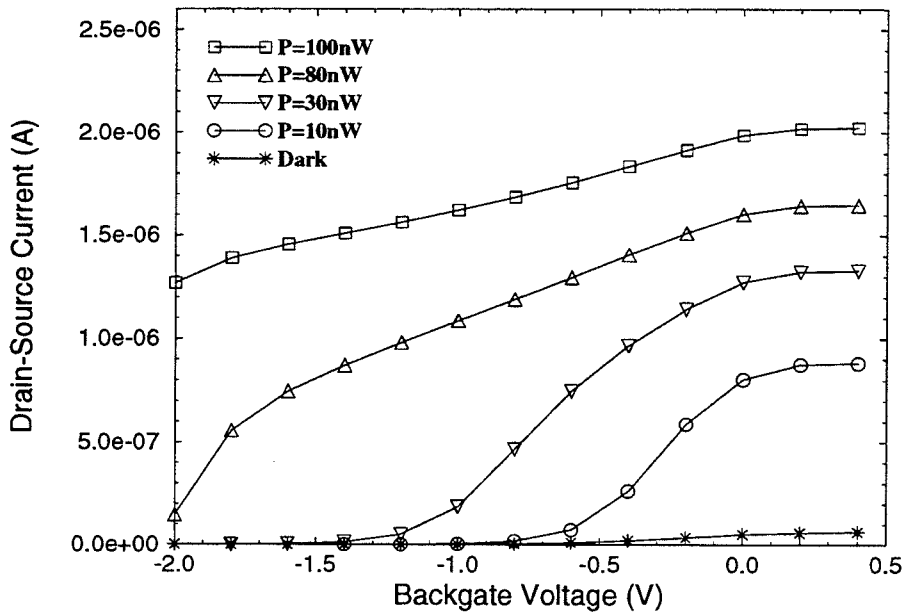


Figure 4.16: Drain-source current for EFET photodetector as a function of the backgating voltage for different optical input intensities

4.4.3 Backgating Effect in optical FETs

Optical FETs are also sensitive to backgating. Figure 4.16 shows the drain-source current as a function of the backgate voltage at different optical input intensities. For optical intensities greater than 100nW, backgating is no longer a problem. Notice that the curves for the optical FET are very similar to the curves for the DFET shown in Figure 4.15.

Unfortunately backgating and detector sensitivity are closely related [16]. Figure 4.17 shows the responsivity of two detectors on runs N2CM and N35U with and without backgating. The gate electrode was tied to the source so that the channel substrate interface would be isolated. While the N2CM detector shows little responsivity to light, it is also not sensitive to backgating. With -1V applied to a backgate, no noticeable change in the current was de-

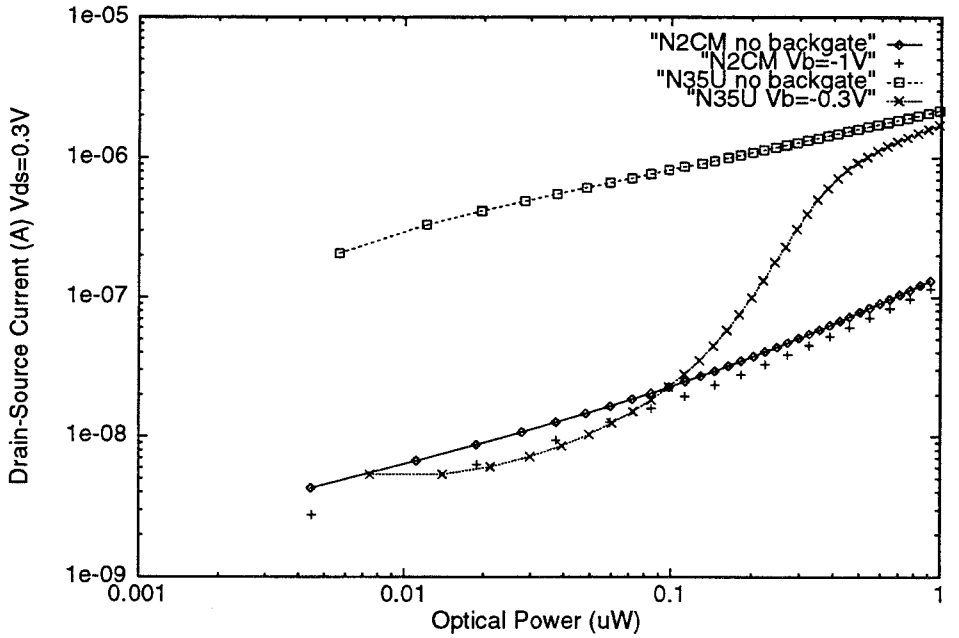


Figure 4.17: Detector responsivity of two different runs (N2CM and N35U) showing the correlation between optical responsivity and backgating responsivity

tected. On the other hand, the N35U detector has much higher responsivity and with only -0.3V on the backgate, the responsivity reduced to that of the other detector.

4.4.4 Solutions to reduce backgating

FETs on the N35U MOSIS chip are very sensitive to backgating. -2V on an n^+ contact can reduce the drain-source current the FET by over 50%. This seriously limits the ability to build threshold circuits. The responsivity of EFET photodetectors is also seriously affected by backgating.

One possible solution to backgating is to etch a moat around the transistor. The following experiment was performed to determine the effectiveness of an isolation etch.

The large n+ LED region on the N35U chip was used to make accessible n^+ contacts. The LED region was specified by an GOG (overglass etch) and G17 (Street clear etch) over n^+ implant. The first step in preparing the chip was to completely removed any oxide on the LED region with a CF_4 plasma etcher. The next step was to deposit AuGe/Ni/Au for the ohmic contacts in the LED region. The contacts were not alloyed because it is a high temperature process. H_3PO_4:H_2O_2:H_2O (1:1:5) etchant was used to etch around the AuGe/Ni/Au contacts. This isolated the contact from the FET being tested. The n^+ ohmic pad specified in the original layout remains an ohmic contact and not isolated during the etch. The pad is used as a reference to compare the effect of etching. The test FET was a Depletion mode FET with the gate tied to the source. Figure 4.18 shows the effect of backgating for different etch depths. There is no noticeable effect until the etch depth is greater than 0.7μm. After etching 1.4μm the backgating curve remains constant with further etches. While this is an effective method to reduce the backgating, it is not practical to etch a packaged chip. This approach is only realistic for chips when the etching is performed as part of the post-processing of the regrowth process.

Another method to isolate FET from bakgating is to try to isolate the p region underneath the FET channel. This can be done by surrounding the FET with a p+ contact or with an n+ ion implant and n+ ohmic contact. Currently in the MOSIS process, it is not possible to make an ohmic contact to the p region. Surrounding the FET with a large area of n+ ion implant and n+ contact eliminates some of the p region around the FET. By applying

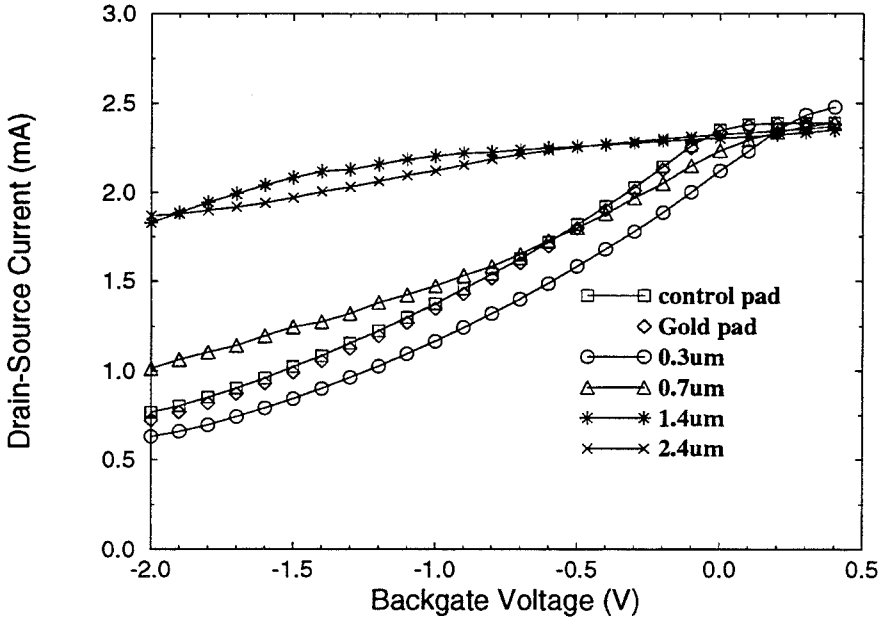


Figure 4.18: Backgating from n^+ pad after etching N35U

a positive voltage to the n+ guard ring, the entire region around the FET is depleted. Any negative voltage applied outside of this guard ring will not be able to penetrate to the FET channel. Figure 4.19 shows how an n+ guard ring can reduce the effect backgating. The test FET was an optical FET with an input optical intensity of 10nW. The optical FET was surrounded by an n+ ion-implant region with an ohmic contact. The backgate contact was located outside of the n+ guard ring. From the graph we see that with positive 3V applied to the guard ring, the optical FET becomes insensitive to the backgate. Unlike the trench etch method to reduce backgating, applying a positive voltage to the guard ring, increases the source-drain current. For circuits where it is impractical to etch around each FET, the n+ guard ring provides a good way to reduce backgating.

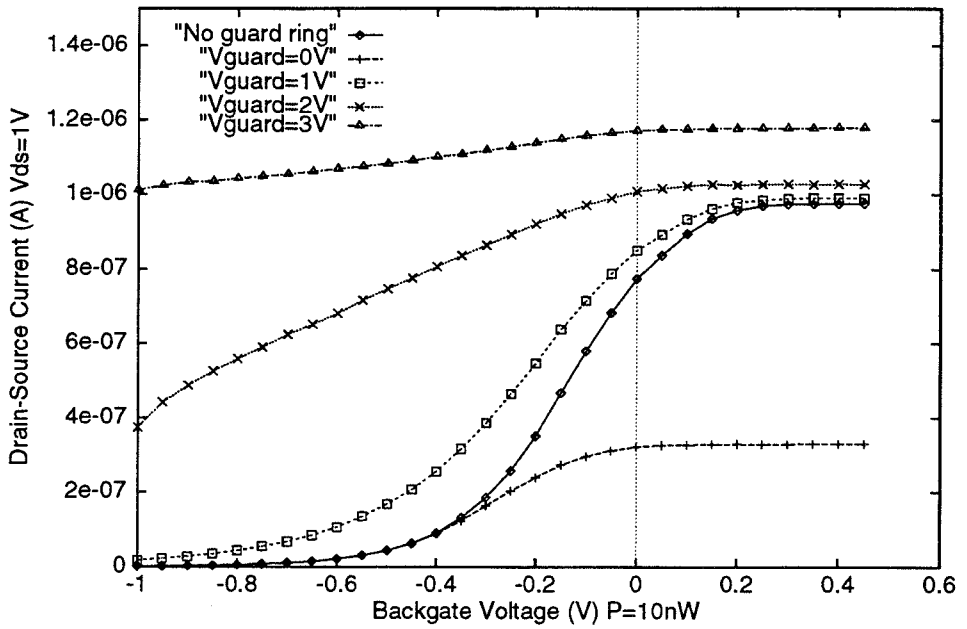


Figure 4.19: N+ Guard ring to reduce backgating on EFET 1/40 N38K P=10nW

4.5 Analog Circuits Design Using the HGAAS3 MOSIS Technology

In the last chapter, the circuits were based only on a single transistor and were relatively simple. With the MOSIS chips we are not limited to only single transistor circuits. More complex circuits such as the bump function and the winner-take-all function are now feasible.

The first step in any circuit design is simulation. The circuits discussed in this section were simulated using HSPICE available from Meta-software. The MESFETs are modeled as JFETs using the physical parameters available from MOSIS. The optical FETs can be modeled as JFETs as well where the optical power is represented as an electrical voltage applied between the gate and the source of the transistors.

The basic subcircuit of any more complex circuit is the inverter. Figure 4.20 shows the circuit diagram and response for a Direct Coupled FET Logic (DCFL) inverter. The input voltage is applied to the gate of the lower transistor which is in this case an EFET. The DFET has its gate tied to the source so that it acts as a current sink. The output is taken at the node voltage. The gate width divided by the gate length is referred to as β for a given transistor. In order to have a sharp swing in the output voltage, $\frac{\beta_e}{\beta_d} > 10$. Because the input signal to the inverter is positive with respect to the negative terminal, the output of one inverter circuit (which is also positive) can be directly coupled to the next circuit. If the input transistor had been a depletion mode FET, the input signal would have to be negative with respect to the negative terminal and therefore the output voltage would have to be buffered to be able to cascade circuits. Circuits designed using only depletion-mode FETs are referred to as Buffered FET Logic (BFL).

The threshold circuit is very similar to the inverter circuit except the depletion mode FET is replaced by an enhancement mode FET and the input signal is applied to the upper FET. In an optical threshold circuit, the EFET can be used as a detector and the gate can be left floating. This alleviates the problem of applying a differential voltage between the gate and source. Figure 4.21 shows the results from the circuit simulation for an optical input and an electrical threshold voltage. In the simulation the input signal is a voltage applied between the gate and source of the upper transistor. The equivalent optical input power was calculated using Eq 4.7 in section 4.3.

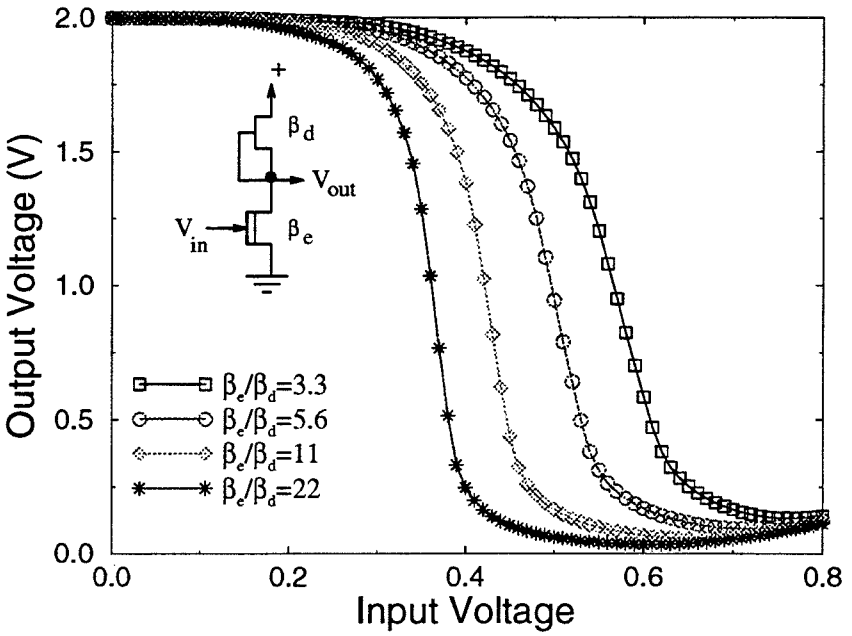


Figure 4.20: Simulation results from basic inverter circuit with different FET geometries

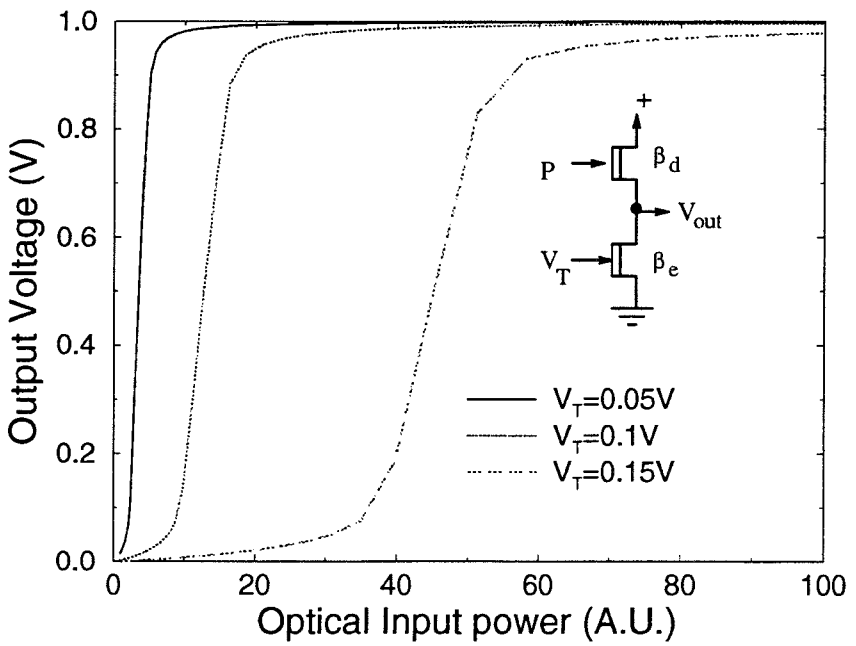


Figure 4.21: Simulation of an Optical Threshold Circuit without backgating.

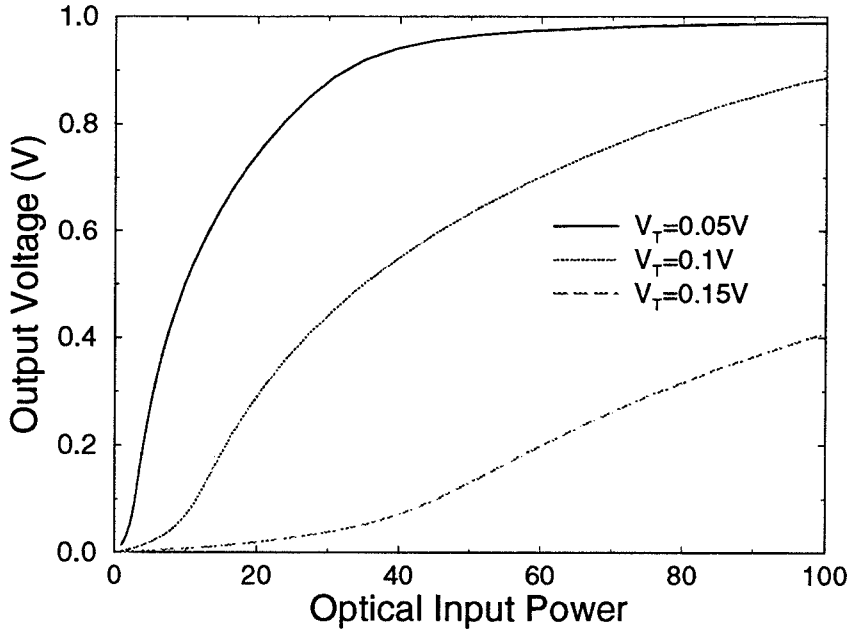


Figure 4.22: Simulation of an Optical Threshold Circuit with backgating

If one includes backgating into the model, the circuit response degrades significantly. Figure 4.22 shows the results of the simulation of the same circuit as above except this time backgating was included. Backgating is simulated as a voltage dependent voltage source that is in series with the applied gate input voltage. Notice that the required optical input power to make the node voltage go high is now much larger.

The similarity or bump function is a function closely related to the threshold function. Figure 4.23 shows the desired response of the bump function. The output is only high when the input is equal to some threshold. If the input is either greater than or less than the threshold, the output is low. The width of the bump function is designated as σ. This function is used in training neural networks with the back error propagation (BEP) algorithm. The BEP learning rule is to change the strength of a particular weight by an

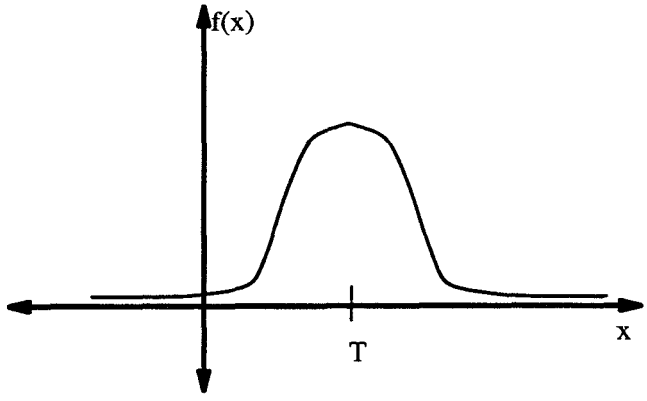


Figure 4.23: The bump function

amount proportional to the error between the actual output and the desired output. The bump function is also the basic function for radial basis function networks.

The exact shape of the curve is not so critical. What is important is that the maximum occurs when x=t and otherwise the output is close to zero. One way to implement this function is with two competing threshold circuits. Figure 4.24 shows the circuit diagram for the bump function. A and B are the two inputs for the bump function to compare. The output is taken at $V_{nodeout}$. If I(A)>I(B) then V_{node1} is close to V_{pl} and V_{node2} is close to V_{min}. This causes the output node to be shorted to ground when we have a constant current supplied by the DFET (V_{gs}=0V). The situation is the same when I(B)>I(A). Only when I(A)≈I(B) will both depletion FETs be off so that $V_{nodeout} \approx V_{DD}$.

To produce an optical output, we could put an LED across $V_{nodeout}$ and ground. This would mean that the LED is driven by the gate-source con-

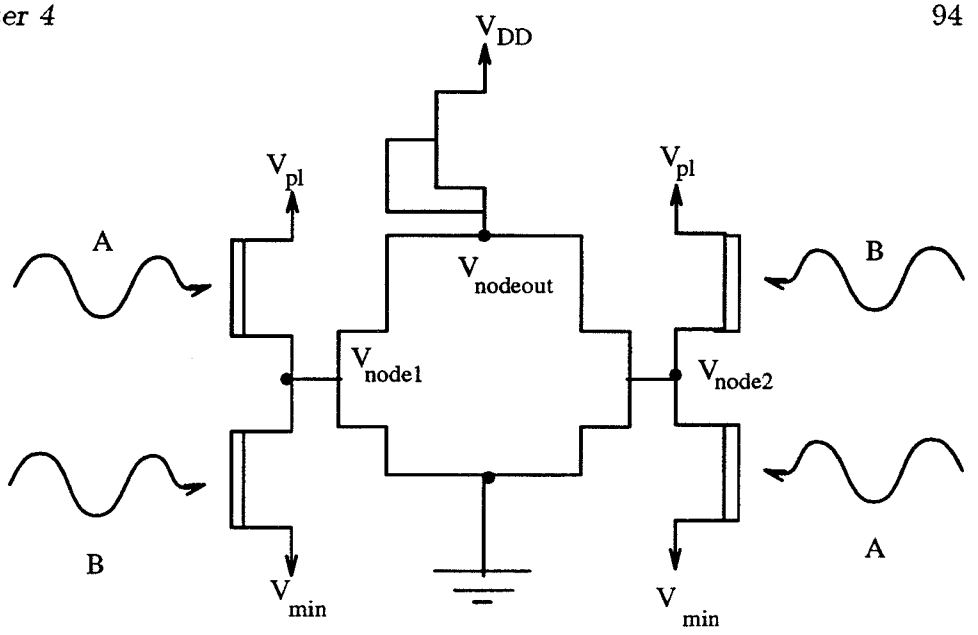


Figure 4.24: Circuit Diagram for an optical bump function.

nected DFET which is typically small to reduce the power dissipation. Instead, can add a large EFET to drive the LED.

We can eliminate the need for the dual optical input circuit by inverting the signal from one optical thresholding circuit. Since the two threshold circuits are simply th inverse of each other, it might be simpler to just pass the output of one of the threshold circuits through an inverter instead of trying to illuminate two detectors evenly with one input.

The results of SPICE simulations show that in order for the bump circuit to function properly, the inverter circuit should be symmetrical. Unfortunately the IV characteristics for an EFET at V_g=0.4V is significantly different than for V_g=0.6V. This explains the asymmetric bump shape. If we connect the output voltage to an EFET to drive an LED, we can suppress some of the asymmetry. Results of these simulations show that the

performance of the circuit is very much dependent of the parameters of the MESFETs (i.e., the threshold voltage and transconductance). Therefore it is probably not a good circuit to fabricate because of the nonuniformity.

Another common circuit in neural networks is the winner-take-all circuit. The circuit diagram for an N unit WTA circuit is shown in Figure 4.25. The basic idea of the Winner-Take-All circuit is that if I_1 is greater than any other input current then $I_{out1}=I_C$ and all other output currents are zero. The circuit relies heavily on the fact that the output conductances of the EFETs is small so that V_1 has to change a lot for small ΔI_1, which causes a huge change in I_{out1}. This means that the transistors should always be in saturation. All the transistors except the current sink should be EFETs. This is to ensure that V_i is never less than ground. Figure 4.26 shows the response of a winner-take-all with three inputs. The inputs EFETs and output EFETs are scaled so that the output current is much greater than the input current. The input current corresponds to the photocurrent and the output current corresponds to the LED output current. In order to have optical gain, the output current must be much larger than the input current. As the current gain increases, the switching between on and off becomes more and more gradual because of the increase in the output conductance. Thus there is a trade-off between the current gain and the sharpness of the curves. Adding more branches to the circuit does not change the circuit performance just the complexity of the simulation.

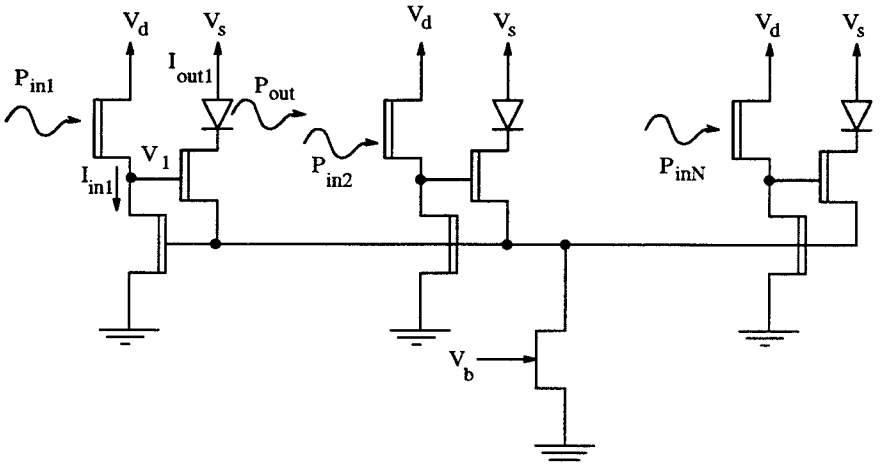


Figure 4.25: Circuit diagram for an N unit Winner Take All circuit

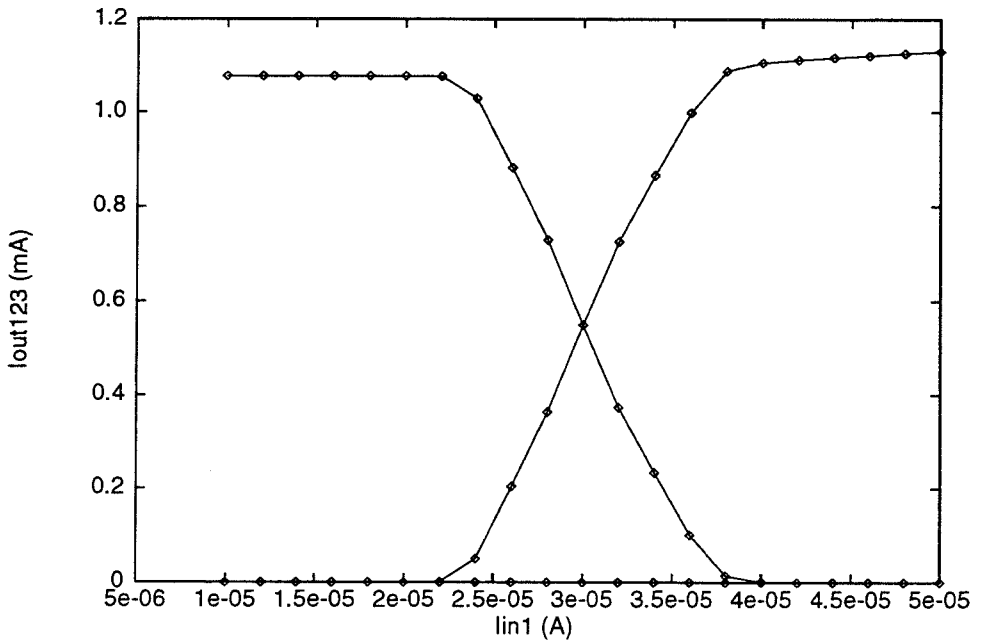


Figure 4.26: Response of a 3 unit Winner Take All circuit

4.6 Summary

Vitesse's E/D MESFET process allows one to design more complex circuit than would be practical with conventional recessed gate epi MESFETs. The optoelectronic circuits can be simulated with HSPICE using device parameters from MOSIS. Circuit layout including design rule checking (DRC) and circuit verification (Layout versus Schematic, LVS) is part of the CAD tool MAGIC. The MESFETs have good transconductance and uniformity. The enhancement-mode MESFET can be used as a high responsivity photodetector with responsivity on the order of 1000A/W for 10nW optical input power. The response time of the detector is governed by the channel-substrate capacitance and is on the order of 10's of microseconds for low input powers. For low frequency circuits, one has to be careful in the circuit design to reduce the effects of backgating. By using n^+ guard rings, or etched trenches, backgating can be reduced. It is important however to include backgating in the circuit design and simulations.

The device not included in the MOSIS GaAs process is the optical output device. Chapter 5 describes a technique to monolithically integrate GaAs/AlGaAs LEDs with the processed MOSIS chips using Molecular Beam Epitaxy (MBE) regrowth. The growth temperature is reduced to 530°C so that the MESFETs performance does not degrade significantly. Even at this temperature, the main reasons the chips can withstand the MBE regrowth process is that the Vitesse process does not include any gold metal. Gold, which is commonly used for contacts, diffuses easily into the substrate and creates deep trap states. The second half of Chapter 5 discusses results from specific circuits where LEDs where monolithically integrated with the Vitesse circuits.

Chapter 5

LED Regrowth on MOSIS chips

In the last chapter, we discussed how we can have GaAs MESFETs circuits fabricated with good uniformity through MOSIS. Unfortunately, active optical sources are not part of the MOSIS HGAAS3 process. It is, however, possible to integrate LEDs with GaAs MESFET circuits using Molecular Beam Epitaxy (MBE) regrowth. In this chapter, we will describe how LEDs are integrated with the MOSIS/Vitesse chips, the performance of the MESFETs after the regrowth, the LED characteristics and conclude with results from the circuit integration.

5.1 Initial LED Integration

As described in Chapter 4, the MESFETs in the Vitesse chips are ion-implantation based devices fabricated on the surface of the GaAs substrate. The Al interconnect metals are deposited on top of the substrate and are separated by layers of silicon dioxide. The first step in preparing the chip for MBE regrowth is to remove the dielectrics in areas where the LEDs are

to be grown. In the first set of experiments, half of the area on the chip was allocated for LED regrowth and the other half for the MESFET circuitry. Separating the two areas made it easy to remove the dielectric stack covering the substrate. Because the composition of the dielectric layers is different from layer to layer, the etch rate is not uniform. We found the best method to remove the dielectric stack completely and still protect the circuits was to cover the circuits with wax and remove the dielectrics with a solution of HF and H_2O (1:10). Although there was quite a bit of undercutting using the wet etchant, the circuits were far enough away that they were not affected. This method of defining areas for LED regrowth is not very good for high density integration. It merely served as a preliminary method for removing the dielectrics. In the initial design, two types of circuit layouts were used. One circuit contained only gate metal and ohmic metal, while the other also used the Al interconnect metals and opened Al probe pads. There was some initial concern that the Al interconnects and pads would not survive the high temperature MBE regrowth. This fortunately turned out not to be the case.

After the dielectric stack has been removed in the LED areas, the surface is thoroughly cleaned using a buffered oxide etchant to remove any oxides formed on the GaAs surface. Unlike normal epitaxial growth, the substrate of the chip is not etched immediately before growth. After cleaning, the chip is then loaded into the MBE chamber along with a 2 inch GaAs epi-ready control wafer. The control wafer serves two purposes. One is to be able to determine the layer thickness during the growth since the chip surface is much too uneven. The other purpose of the control wafer is to determine if

the chip substrate is limiting the performance of the LEDs. Optical sources grown by MBE usually start with a high quality GaAs substrate which has very few substrate defects. Defects in the substrate can propagate up into the epitaxial material and create deep level traps. The substrate requirements for electronic circuitry is not as critical. By comparing the characteristics of the LEDs fabricated on the Vitesse chip with those fabricated on the control wafers, we can determine what the effect of the substrate quality is.

The MBE regrowth was done at MIT in Professor Clifton Fonstad's group. Because the MESFETs begin to fail when exposed to temperatures above 530°C, the MBE growth temperature was reduced to 525°C. Normally optical devices are grown at approximately 800°C to reduce the number of defects in the material. By properly adjusting the arsenic over-pressure, high quality GaAs material can be grown at lower temperatures [60, 4, 38]. The epitaxial structure for the LED is shown in Figure 5.1. At the bottom of the LED stack, a GaAs/AlGaAs superlattice is grown to impede defects from the substrate from propagating upwards. Instead of propagating upwards, line defects propagate to the side in the superlattice thereby protecting the upper epi-layers. The LED structure was grown with the p side down so that the light generated at the undoped GaAs/n AlGaAs interface would not be reabsorbed in the undoped region before reaching the surface. The total thickness of the LED structure was designed to match the thickness of the dielectric stack. Thus the LED is planar with the dielectric stack surrounding it, making it is easier to metalize over to the MESFETs circuits.

Once the LED material was grown, the chip and control wafer were re-

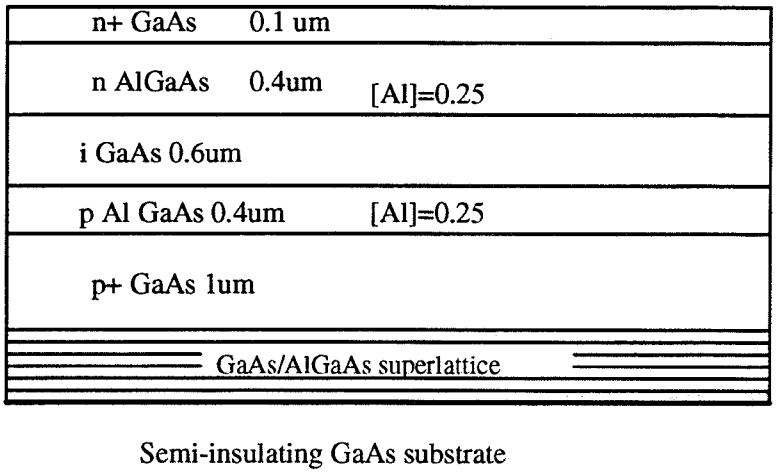


Figure 5.1: Epitaxial structure of the LED grown on the Vitesse chip by MBE regrowth.

moved from the MBE chamber. In the LED area of the chip, the regrown material was visually shiny indicating that the material was single crystalline. Over the electronic circuits, however, the surface appeared very rough. Here the regrown material was polycrystalline. The polycrystalline material covering the circuits has to be removed to gain access to the pads and the detectors. To strip the polycrystalline material, the single crystalline LED area was protected by photoresist and the poly GaAs was removed using a phosphoric etchant (H_3PO_4:H_2O_2:H_2O 1:1:5). The phosphoric etch is well suited for removing the poly GaAs because it does not attack the Al pads significantly. Figure 5.2 shows a photograph of the first Vitesse chip after LED regrowth. On the lower half of the chip, the dielectric stack was removed and the LED epitaxial material was grown. On the upper half of the chip are the MESFET circuits. Notice that the LED material contains only

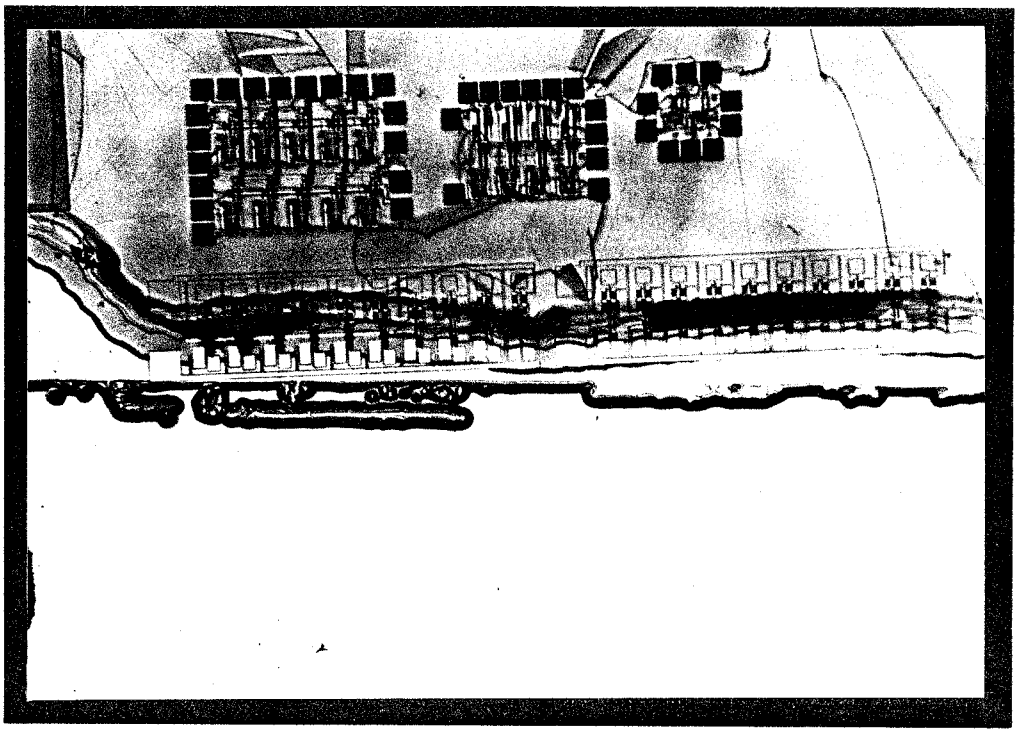


Figure 5.2: Photograph of the first Vitesse chip after the poly GaAs had been removed from the MBE regrowth.

a few defects. The total chip area was 3000μm $\times$ 3000μm. The LED area was 2000μm $\times$ 3000μm.

The next step in the LED processing is to define individual LED mesas by wet chemical etching. This step is similar to the first step in the optoelectronic circuit processing on epi-wafers described in Chapter 3. Because the chip is so small, it was difficult to spin a thin layer of photoresist across the entire chip. To prevent the photoresist from beading up at the edges of the chip, the chip was mounted on a larger substrate and surrounded by dummy wafers of the same thickness. Thus the edges of the chip were extended and

the photoresist would bead up on the dummy wafers rather than the test wafer. The LED mesas were etched down to the p+ contacting layer. This provided access to the p+ layer as well as isolating the LEDs from one another. After the mesa definition, a thin layer of silicon nitride (100nm) was deposited to passivate the surface. Openings in the silicon nitride for the n and p contacts were made using a CF_4 plasma etcher in the same manner as describe in Chapter 3. The ohmic contacts (AuZn/Au for the p contact and AuGe/Ni/Au for the n contact) were evaporated and pattern using standard lift-off techniques. Figure 5.3 shows a photograph of the fully processed Vitesse chip. The LED mesas are on the left-hand side of the chip while the electronic circuits are on the right. The electrical connection between the LEDs and the electronic circuits was made externally through contacting probes. The sketch below the photograph shows the surface profile across the chip. The deep etch in the center of the chip is due to the poly GaAs etch and the mesa etch overlapping.

Before the LED mesas were etched on the chip, the photoluminescence from the single crystalline material on the chip and the epimaterial on the control wafer were compared. Figure 5.4 shows the photoluminescence curves for the two wafers. The measurements were taken at room temperature with an Ar^+ ion laser illuminating the sample. The light emitted from the sample passed through a 0.25m grating spectrometer with the entrance and exit slits opened to 2mm. The Argon beam was incident at an angle so that it would not be detected in the spectrometer. Because the slit openings were large and the experiment was done at room temperature, the width of

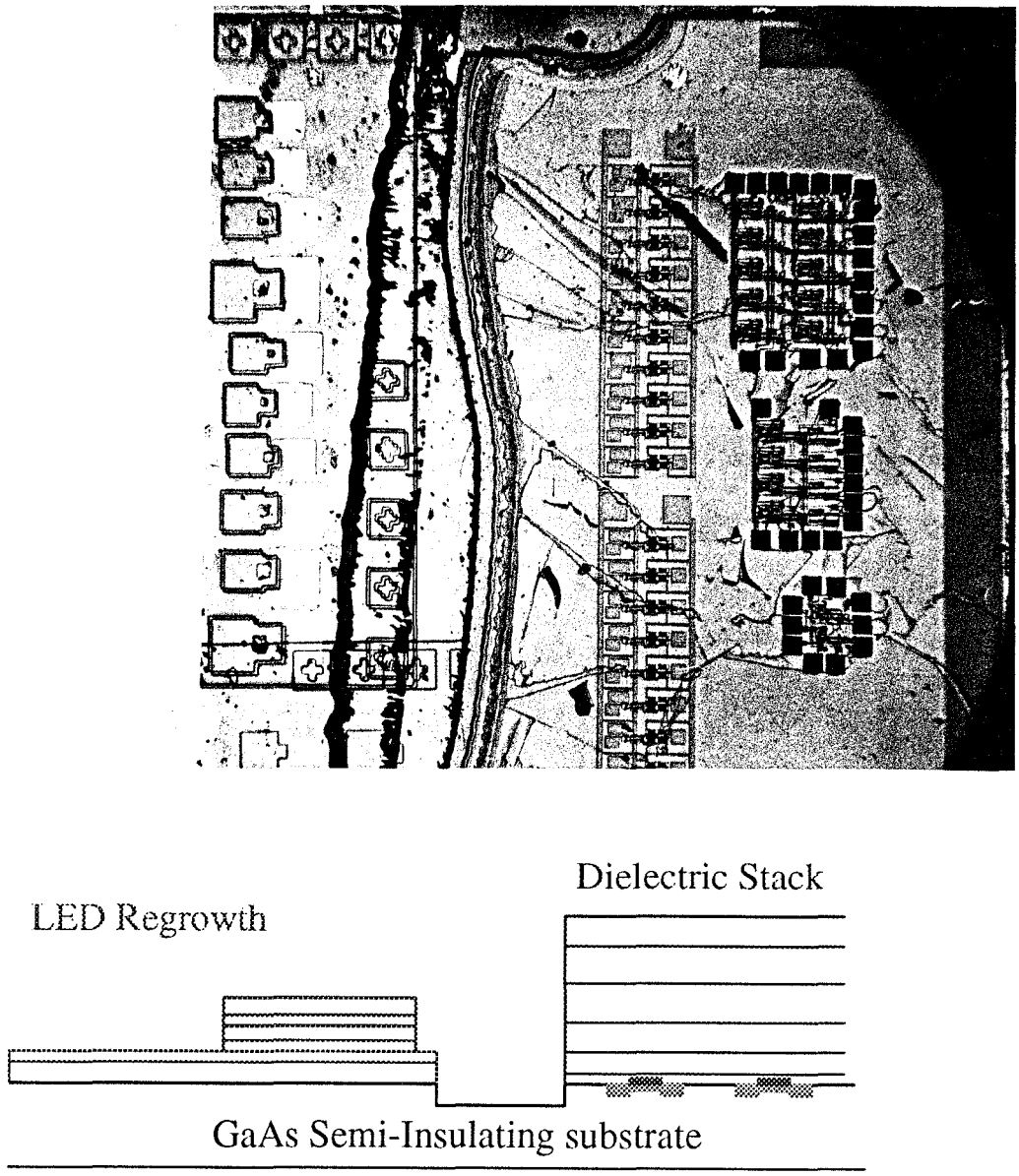


Figure 5.3: Photograph of the first Vitesse chip with LEDs monolithically integrate by MBE regrowth. The sketch below the photograph shows the surface profile across the chip

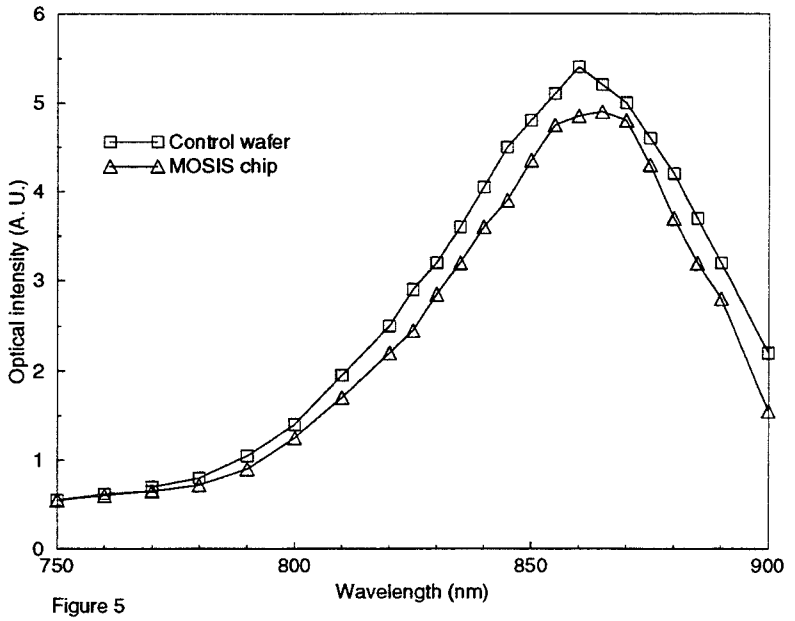


Figure 5.4: Photoluminescence from the epitaxial material on the MOSIS/Vitesse chip and on a control wafer for an double heterojunction LED structure grown at 525°C.

the photoluminescence curve does not convey much information about the material. It is encouraging though the relative amplitude and location of the maximum for the two samples are identical. If the material on the chip had a large number of defects, the electron-hole pairs excited by the Argon beam would recombine non-radiatively and the PL peak for the chip would be significantly smaller than the control wafer.

Figure 5.5 shows the LI curve and Figure 5.6 shows the IV characteristics of the LEDs fabricated on the MOSIS/Vitesse chip. In both cases the curves are nearly identical to the characteristics of LEDs fabricated on the control wafer indicating that there is no significant difference in the quality of material in the two cases. The efficiency of the LED was 0.0002W/A which is

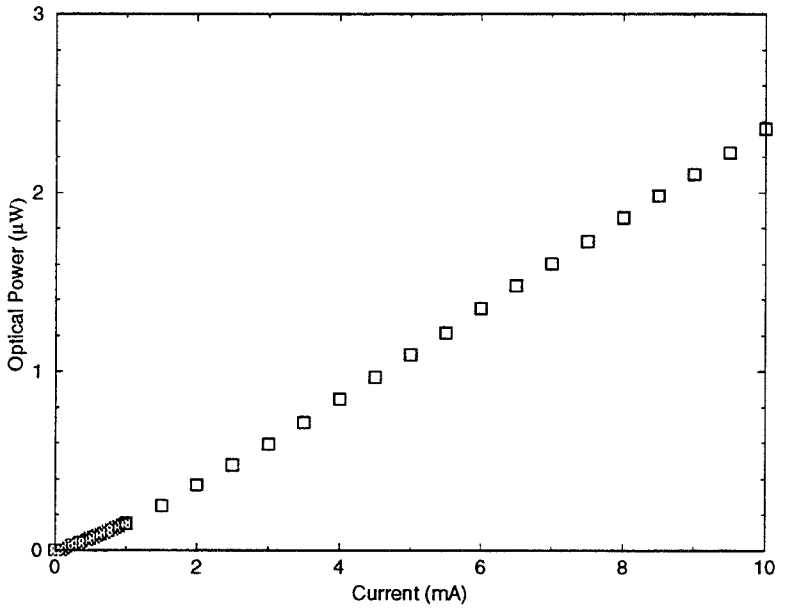


Figure 5.5: Light out vs current in for LED on the Vitesse chip

relatively low but comparable to LEDs made on standard epi wafers where no current confinement is used. Because the top AlGaAs layer is relatively thin, the current cannot spread out from the electrode. Thus, most of the current flows directly underneath the electrode and it is difficult to extract the light.

5.2 LEDs Grown in Dielectrics Vias

A more practical method to remove the dielectric stack in small areas for the LED regrowth is to define a mask layer in the original circuit layout. The final step in the Vitesse process is to etch the dielectrics in the scribe lines. This mask layer is called 'street clear' or G17 in CIF (Caltech Intermediate Form). We can use this mask layer to etch vias in the dielectrics in areas on

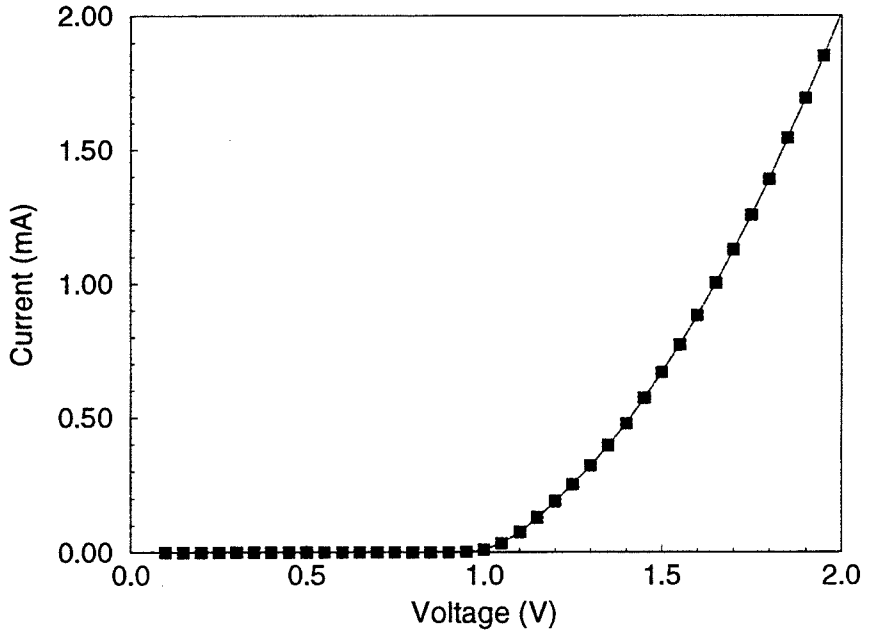


Figure 5.6: IV curve for LED on the MOSIS/Vitesse chip

the chip where we would like to grow LEDs. To ensure that the etch reaches the surface completely, we typically add an overglass (the top dielectric layer, GOG) etch to the layout as well. With this method we are able to define dielectric vias as small as $10\mu m \times 10\mu m$. The dielectric etch done at Vitesse uses powerful Reactive Ion Etching (RIE) to etch anisotropically down to the substrate.

Figure 5.7 shows a sketch of the chip cross-section with the LED grown in the dielectric via. Along with the G17 and GOG layers which specify the dielectric vias, an n^+ ion implant is also specified at the substrate surface. This allows the bottom contact of the LED to be made in the circuit layout. Thus the only contact required after the regrowth is the top p contact.

Figure 5.8 is a photograph of a MOSIS chip with regrowth in a vari-

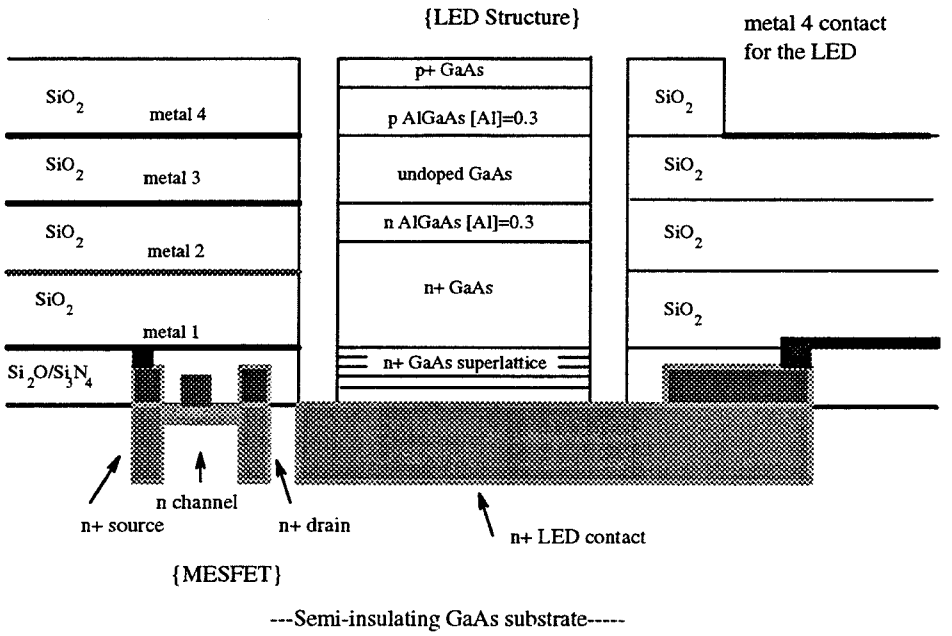


Figure 5.7: Cross-section of a MOSIS chip with the LED grown in the dielectric via

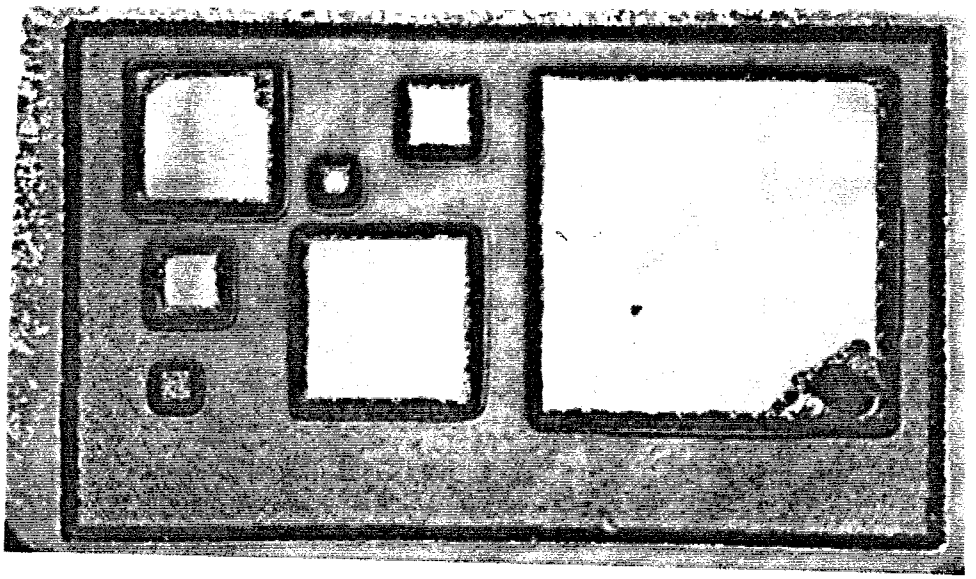


Figure 5.8: Photograph of LED regrowth in small dielectric vias on MOSIS N35U

ety of different sizes. The sizes of the regrowth area are 100μm x 100μm, 50μm x 50μm, 20μm x 20μm and 10μm x 10μm. Notice that the regrowth in one of the small 10x10 areas is not single crystalline. This is most likely due to the GaAs substrate surface was not completely cleaned and not because of the lowered temperature MBE regrowth. Because the dielectric stack is 4μm high, it is unlikely that the substrate surface can be sufficiently cleaned to produce single crystalline GaAs in areas less than 10μm x 10μm.

The post-processing required on the chip after the LED regrowth is relatively simple. The first step is to mask off the LED area with a 5μm overhang to protect from overetching (see Fig 5.9(a) and (b)). A phosphoric acid based

etchant can be used to remove the unprotected polycrystalline GaAs layers. The etch time should not be too long because of undercutting around the mask. The polycrystalline material left around the LED area is partially removed with a second etch (see Figure 5.9 (c)). The mask for the second mask should be slightly (5μm) smaller than the LED via. The etch depth for this step must be less than 4μm. The minimum etch depth is 2μm so the active LED area is isolated from the dielectric stack and the polycrystalline material.

The next step after the two wet etches is to deposit a thin layer of silicon nitride for surface passivation and electrical isolation. A small opening in the silicon nitride on the LED mesa is required to make electrical contact to the LED. The final mask defines the p ohmic contact area. AuZn/Au (500A/1000A) is evaporated and defined using standard lift-off procedures.

Figure 5.10 shows a photograph of three LEDs grown in 40μ x 40μm dielectric vias. The three LEDs correspond to the different outputs for a three unit winner take all circuit. The bottom contact is made through the n+ source/drain ion implant on the GaAs substrate and is electrically connected to the rest of the circuit using ohmic metal and metal1. Although the top contact for the LED has to cross a 4μm trench from the LED mesa to the pad area, there were no discontinuities in the metal. This is most likely due to the fact that the polycrystalline GaAs does not have a preferred etch direction. The IV curve of the LED shown in Figure 5.11 confirms that the bottom n contact provides a good ohmic contact to the LED.

Reliability of the LEDs is also extremely important if the optoelectronic

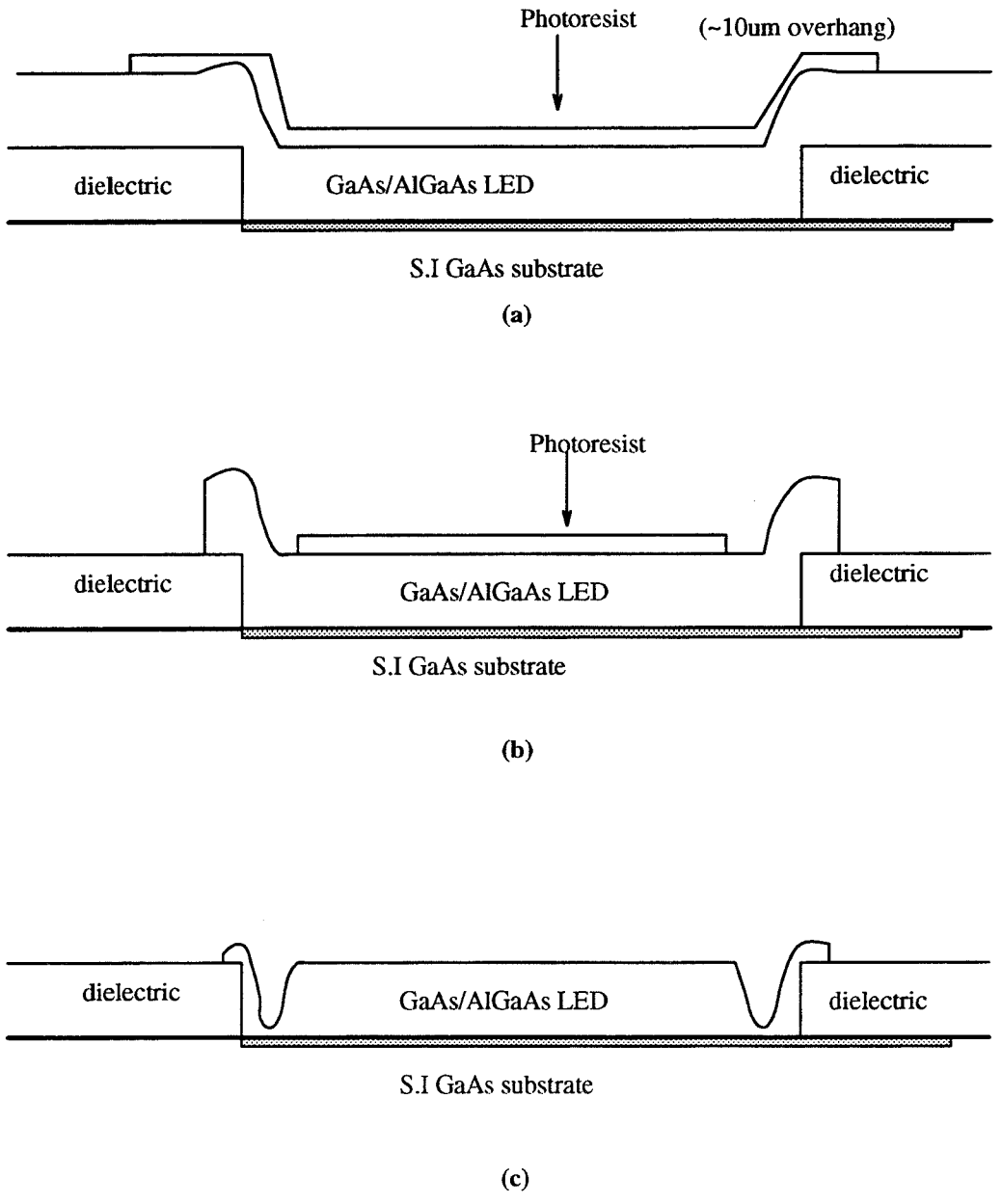


Figure 5.9: Post-processing steps for removing polycrystalline regrown GaAs material

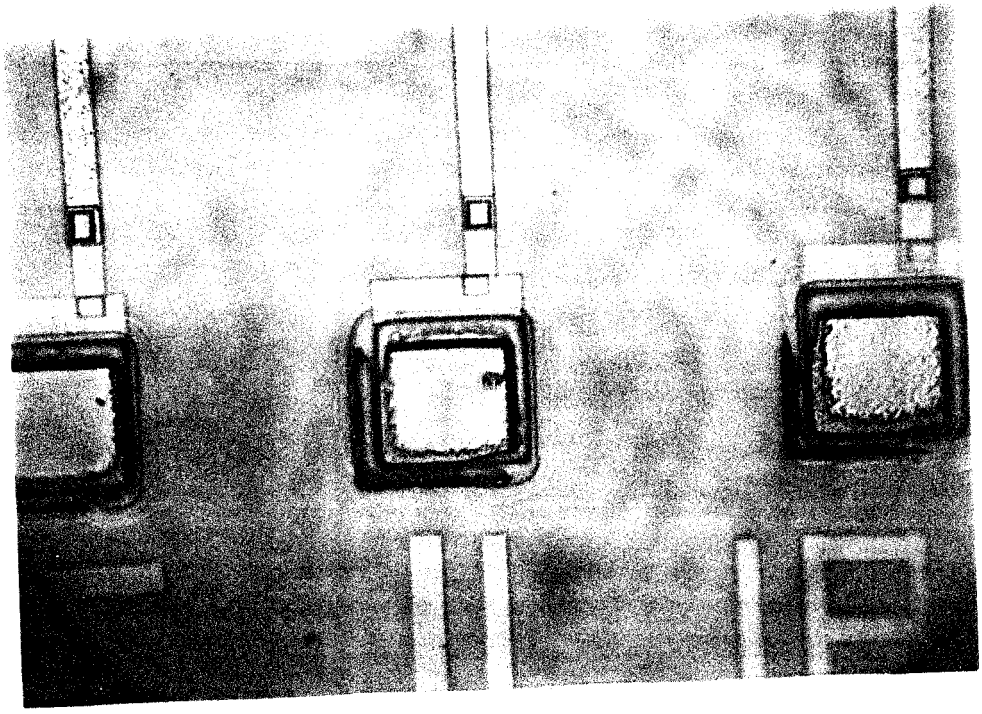


Figure 5.10: Photograph of three LEDs grown on a GaAs MOSIS chip in the dielectric vias

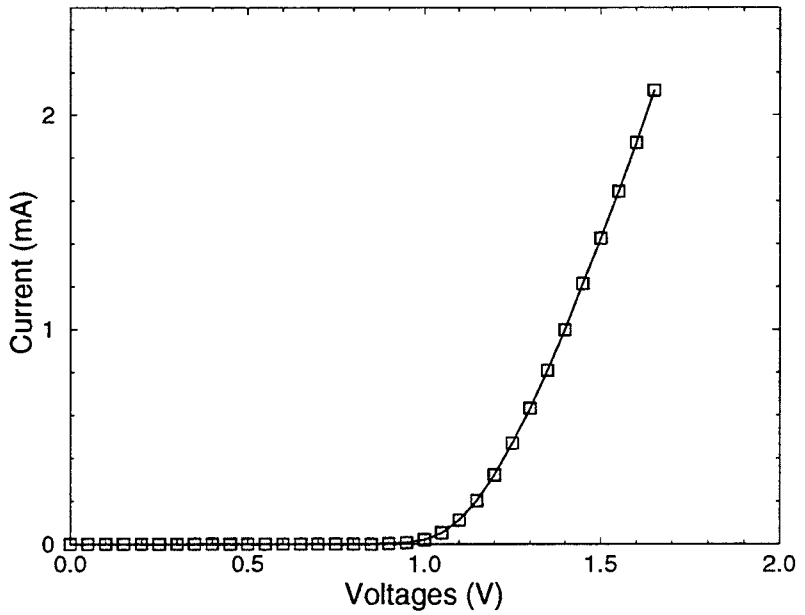


Figure 5.11: IV characteristics of LEDs grown on MOSIS N38K chip

circuits are to be useful. Reliability refers degradation of the LED efficiency as a function of operating time. During the first few hours of operation the efficiency of the LED can drop rapidly due to the growth of dislocations in the active region [31]. It is therefore very important that the surface of the GaAs substrate be extremely clean and that the substrate itself contain few defects. Figure 5.12 shows the decay in the LED efficiency over time. Notice that the drop in efficiency after 500 minutes has dropped almost 30% from the initial efficiency. After the first few hours, the efficiency degradation is not as severe. Commercially available LEDs quote the efficiency after the initial burn-in. The lifetime of commercially available LEDs is over 10,000 hours [50]. The low lifetime in the LEDs grown on the MOSIS chip reflects the poor surface quality of the chip.

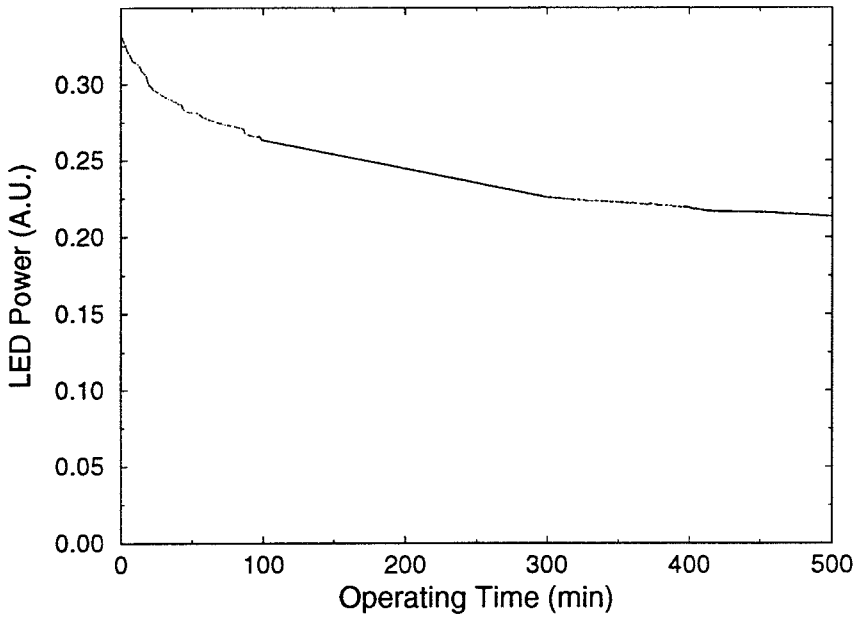


Figure 5.12: Lifetime of LED fabricated on N38K chip. LED current was set to 5mA.

5.3 MESFET Performance after Regrowth

The MESFETs and optical FET detectors are fabricated on the chip before the LED regrowth. This means that the devices must be able to withstand the high temperature MBE growth for several hours. Extensive measurements have been made on the effects of prolonged exposure to elevated temperature for the Vitesse process [51]. At high temperatures, the transconductance of the MESFETs degrades due to diffusion of the Si implants. There is a sharp drop in the transconductance as the temperature rises above 530°.

Table 5.1 shows the transconductance of depletion-mode FETs before and after regrowth on run N35U. Notice that the FETs with short gate lengths suffer more from the regrowth process than the longer gate FETs. This is

Transconductance of Depletion-mode FETs with W=58μm

Gate Length	g_m before	g_m after	Δg_m
L=1μm	172 (mS/mm)	103 (mS/mm)	(40%)
L=5μm	38 (mS/mm)	34 (mS/mm)	(10%)
L=20μm	10.4 (mS/mm)	9.8 (mS/mm)	(6%)

Table 5.1: Degradation in MESFET transconductance after MBE regrowth

because diffusion of the dopants has a larger effect on the fractional change in the gate length for the short gate FETs than in the long gate FETs. Despite the drop in the transconductance, the MESFETs still perform quite well. In the circuit design and simulation, the device parameters to be included should reflect the MBE regrowth process.

Not only does the transconductance of the MESFETs change during the regrowth, but backgating seems to be less of a problem. Figure 5.13 shows the normalized drain-source current of a depletion mode FET after regrowth. Notice that there is little backgating when the gate voltage on the FET is below threshold or well above threshold. This was not the case before regrowth. (see Figure 4.15) The data in Figure 5.13 indicate that the substrate is less p doped than before regrowth. This could be due to diffusion of Si ions into the substrate or diffusion from the ohmic metals into the substrate.

Because the MESFET is not sensitive to backgating below threshold, it is likely that the enhancement-mode FET photodetectors are not very sensitive to light for low optical intensities. Figure 5.14 shows the efficiency of an enhancement mode FET photodetector before and after regrowth. Although the responsivity is still very high for strong optical inputs, at low intensities

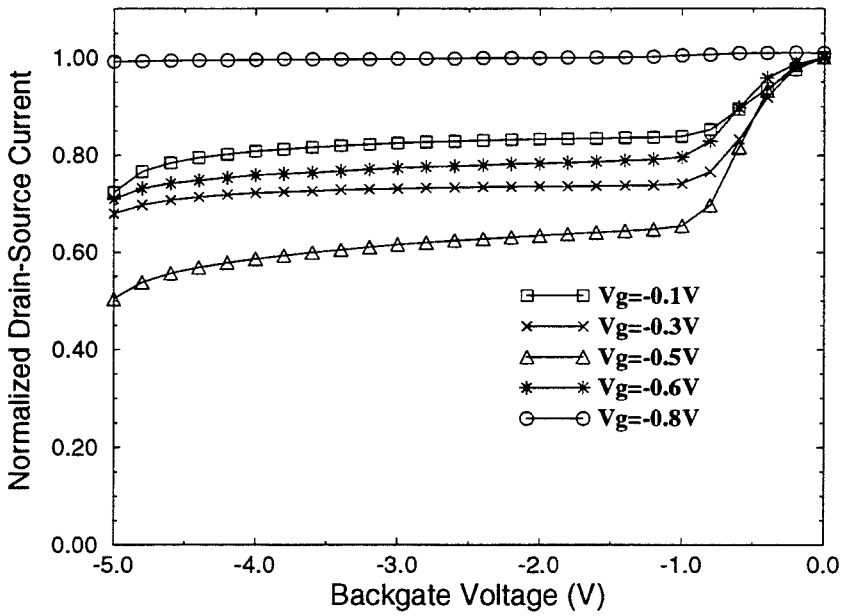


Figure 5.13: Normalized drain-source current of a depletion mode FET as a function of backgating voltage for different applied gate voltages

the responsivity is dramatically reduced. The responsivity curve of the detector after regrowth is very similar to the responsivity curves for the detectors before regrowth when a negative backgate voltage is applied. The responsivity of the optical FET is directly related to the hole concentration in the substrate as discussed in Chapter 4. If during the MBE regrowth process, the donor dopants from the n^+ source and drain implants diffuse into the substrate, the effective hole concentration will go down. The responsivity increases as the optical intensity increases for low input signals indicating that the change in hole concentration is most likely due to an increase in the number of deep level donor states. As the optical intensity increases, the empty donor states get filled by the excited photocarriers. The energy of the

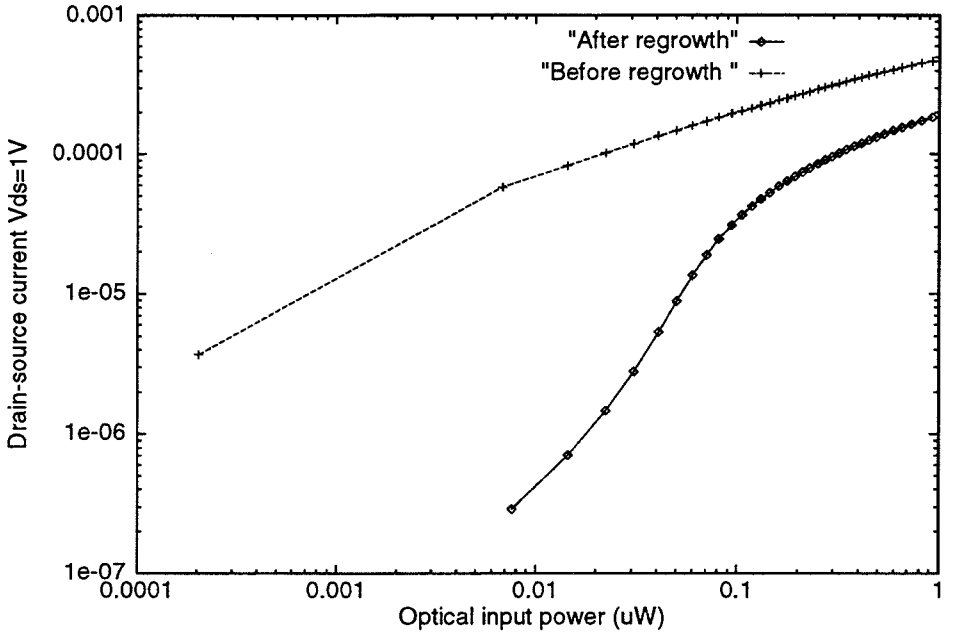


Figure 5.14: Efficiency of EFET photodetector before and after LED regrowth. V_{ds}=1V and the gate was left floating.

dopants can be determined by measuring the responsivity of the optical FET as a function of the wavelength of the optical signal [43].

5.4 Results from Optoelectronic Circuits on MOSIS chips

5.4.1 Optical Inverter circuit

The optical inverter circuit described in Section 4.5 was fabricated using MOSIS HGAAS3 technology. The dimensions of the DFET current load, the optical FET detector, and the LED-driver DFET are: L=8μm/W=6μm, L=1μm/W=40μm, and L=1μm/W=50μm. The saturation current of the DFET current load was 40μA. The dc response of the inverter is shown in

Figure 5.15. The power supply voltage for the input branch of the circuit was -0.8V and the voltage supply for the output branch was 2V. The two curves correspond to the direction in which the optical input power was changed. The squares correspond to increasing optical power and the circles to decreasing optical power. Notice that the transition from off to on is very sharp but that there is also some hysterisis.

In this case the gate was left floating, but it is possible to adjust the threshold by appling a gate voltage. As discussed in Chapter 4, the responsivity of the optical FET depends on the applied gate voltage. As long as the dark current of the optical FET is less than the saturation current of the DFET. As the dark current increases, the on-state current will decrease. This means that the current swing will be smaller for large currents/detector gate voltages.

Figure 5.16 shows the response of the inverter circuit with a 25nW pulsed optical signal. The frequency of the optical signal was 8kHz. Because the LED has not yet been grown on the chip, a 100 Ohm resistor was connected in series with the LED-driver MESFET. The node voltage was AC coupled into a digital storage oscilloscope. The output current through the 100 Ohm resistor is 0.8mA. The optical switching energy of this circuit is equal to the average optical input power (25nW) multiplied by the pulse period (125 μs) which is 3pJ. The switching time of the circuit is limited by the switching time of the optical FET detector.

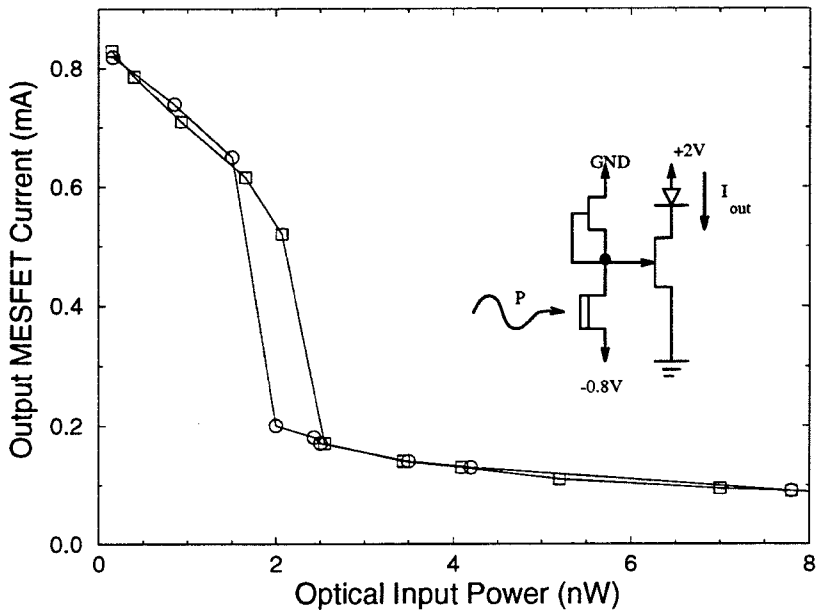


Figure 5.15: DC inverter output current versus optical input power

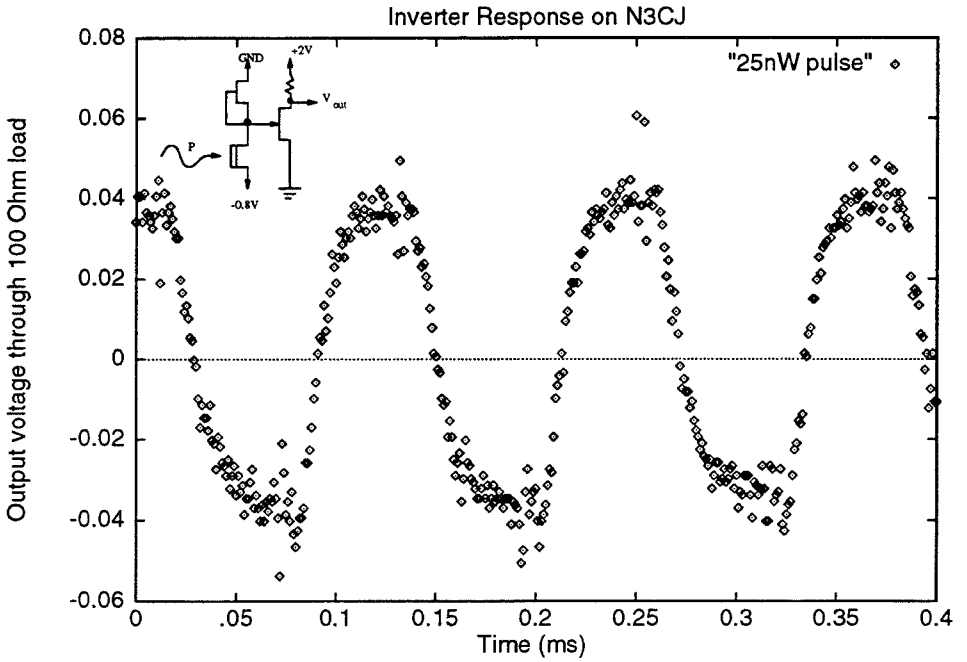


Figure 5.16: Time response of the optical inverter circuit

5.4.2 Winner Take All Circuit

A three unit winner-take-all circuit was fabricated with three LEDs directly connected to the electronic portion of the circuit. The circuit diagram is shown in Figure 4.25. The dimensions of the optical FET detectors are L=1μm and W=40μm. A photograph of the finished circuit is shown in Figure 5.17. The three LEDs are at the bottom of the photograph. The seven large dark squares are the Al bond pads after the regrowth. During regrowth the Al bond pad surface becomes rough, so that the reflection is not specular. The p^+ contacts are not connected to any Al bond pads. Instead, a gold pad is fabricated to the side of each LED and the electrical connection is made with individual probes. Figure 5.18 shows the DC response of the circuit. The optical input power was held fixed on two of the circuit branches at 10nW and 25nW. The output LED currents for branch 2 and 3 are plotted against the optical input power of branch 3. Since the input power on branch 2 is always greater than the input power on branch 1, the output current of branch 1 remains below 1μA. As the input power on branch 3 increases, the output current switches from branch 2 to branch 3. The two main reasons for the gradual transition between the two competing branches are: backgating and finite output conductance.

The ac response of the winner-take-all circuit is shown in Figure 5.19. The input signal on branch 3 was pulsed while the input power on branch 2 was held fixed at 200nW. The average input power of branch 3 was 300nW and the pulse frequency was 2.5kHz. The output voltage plotted on the y-axis in Figure 5.19 is measured at the node where the LED and output

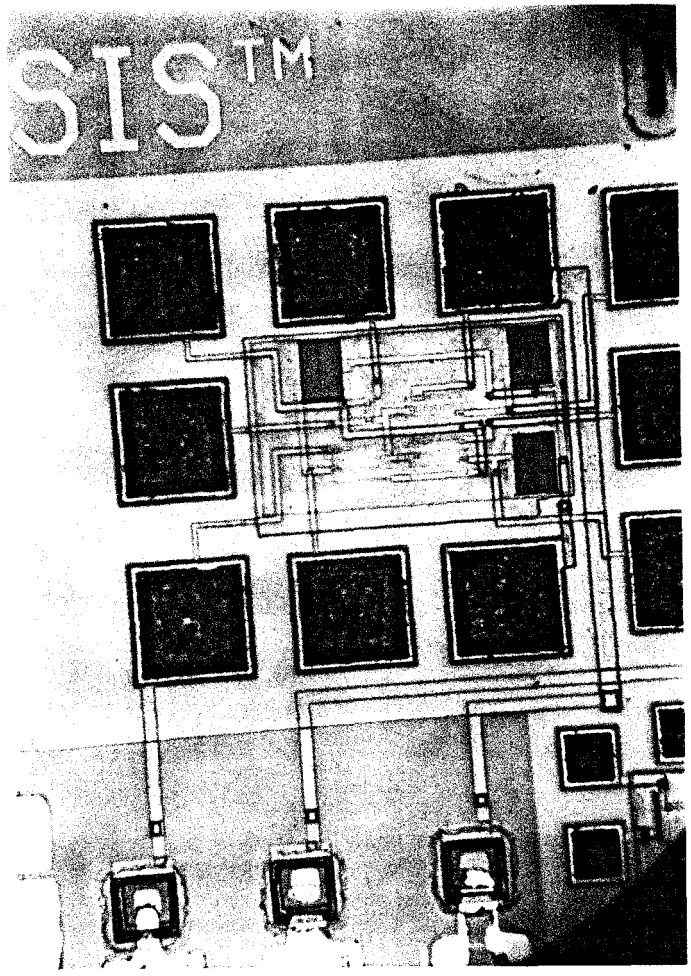


Figure 5.17: Photograph of a three unit winner-take-all circuit with three LEDs directly connected to the circuit through the bottom n^+ contact.

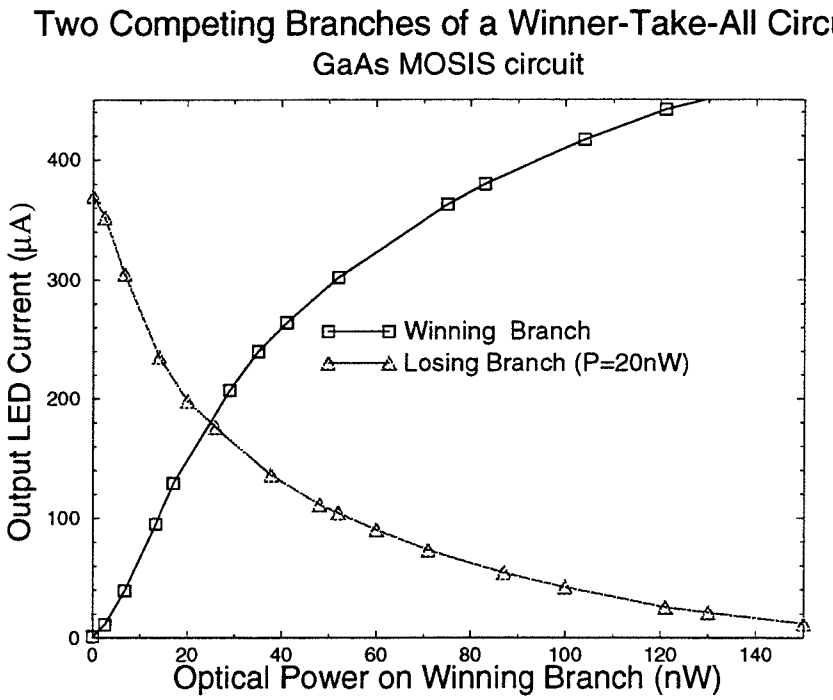


Figure 5.18: Response of two competing branches in a 3 unit winner take all circuit

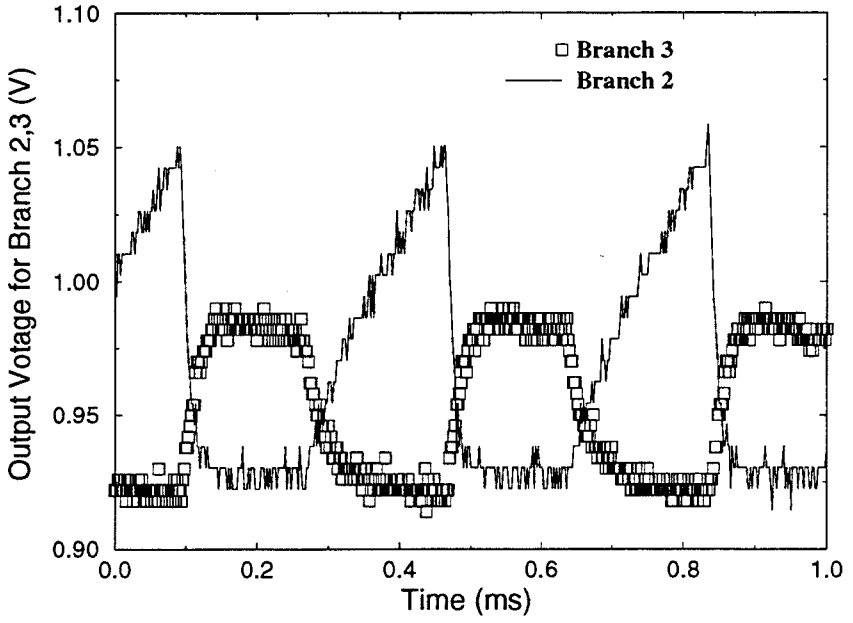


Figure 5.19: Time response to Winner Take All circuit

MESFET are connected. Notice that the response time of the circuit is limited by the time required for branch 2 to pull the current from branch 3. In other words the response time is governed by the input power of the winning branch. The optical switching energy required to transfer the output current is approximately 100pJ.

5.5 Summary

By lowering the temperature of the MBE growth, one can grow GaAs/AlGaAs epitaxial layers on fully processed MESFET circuits fabricated by Vitesse. The openings in the dielectric stack for the regrowth can be specified in the original circuit layout and the regrowth area can be as small as 10μm x 10μm. By specifying an n^+ source/drain ion implant in the growth areas, the n con-

tact of the epitaxial device can be made through the substrate and does not require any post-processing. The post-processing required to remove the polycrystalline GaAs and to deposit the top LED contact are relatively simple compared to fabricating the entire circuit. With this technology, it is now possible to design and fabricate complex arrays. There are, however, a few remaining technological issues which still need to be addressed. First, the reliability and performance of the MESFETs after the regrowth must be extensively studied to determine the exact cause for the failure. Also long-term reliability measurements on the LEDs need to be made to determine if the electronic grade substrate or the lower temperature regrowth seriously affect the lifetime. Studying these issues will only improve the performance of the circuits.

Some specific examples of large arrays currently in fabrication are: a 10×10 winner-take-all circuit and a 10×10 optical latch circuit. The 10×10 winner-take-all circuit is designed to detect the strongest pixel in a 10×10 image. A photograph of the 10×10 winner-take-all circuit is shown in Figure 5.20. The size of each pixel on the chip is 150μm×200μm. Instead of placing the LEDs to one side of the circuit, each LED is placed next to the detector in that pixel. Next to each LED is a metal4 pad with an overglass cut (50μmx50μm) for the top LED contact. The p contact metal will run from the LED to the metal4 pad. The metal4 pad is connected to a bonding pad on the perimeter of the circuit using metal4. This design will ease the lithography requirements in the post-processing.

The other circuit currently in fabrication is a 10×10 optical latch array.

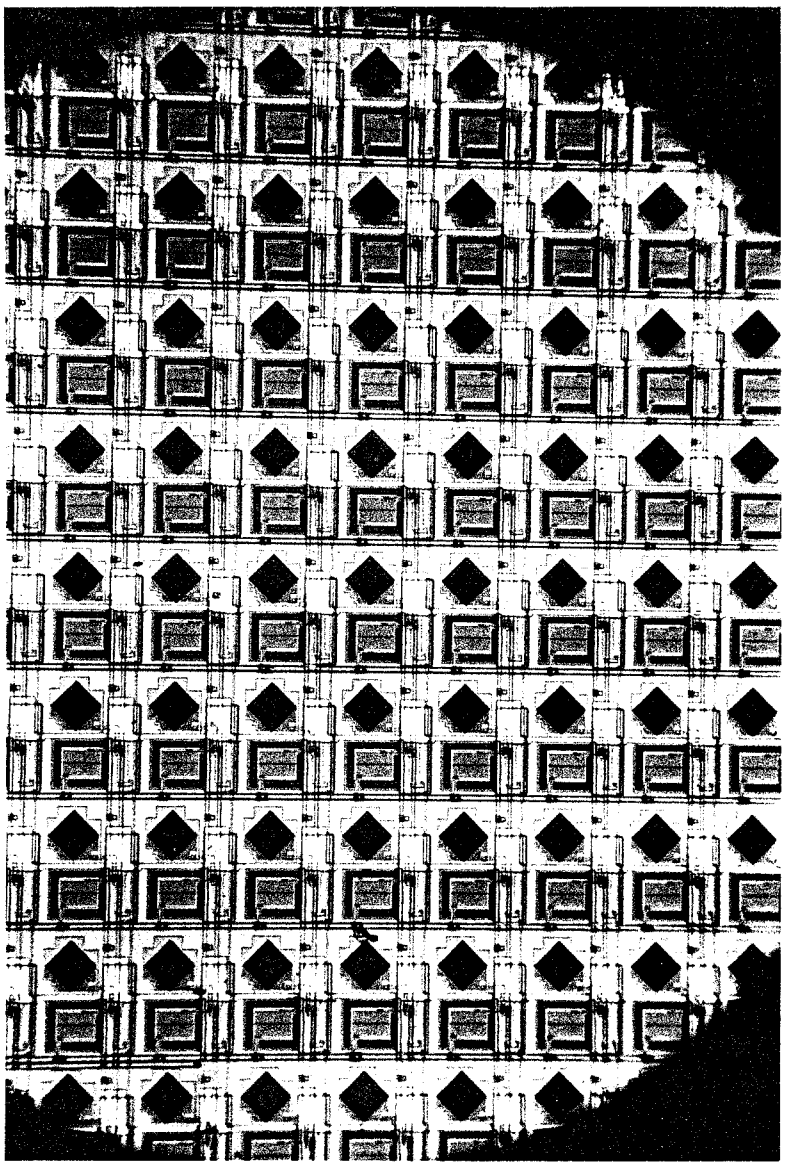


Figure 5.20: Photograph of a 10×10 winner-take-all circuit fabricated by MOSIS

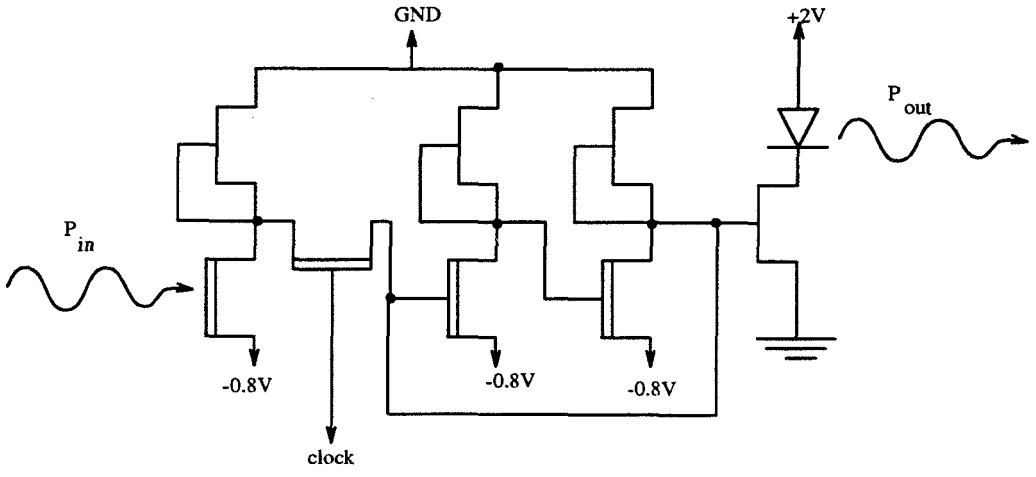


Figure 5.21: Circuit diagram for an optical latch pixel

Each pixel in this circuit operates independently. The optical latch circuit consists of an optical inverter circuit as described earlier, a latching circuit to hold the optical input signal, and the LED-driver MESFET and LED for the optical output. There is an electrical clock signal which is sent to each pixel to control when the voltage on the input circuit is read into the latch. The circuit diagram for the optical latch is shown in Figure 5.21. The area on the chip for one pixel is $90\mu m \times 80\mu m$. These two circuits will demonstrate the high density optoelectronic integration possible with this technology.

MBE regrowth is not limited to LED regrowth. It should be possible to grow Vertical Cavity Surface Emitting Laser (VCSEL) structures as well as multiple quantum well modulator and optical waveguide structures on the MOSIS chips. In the long run, the VCSEL threshold current will be below 1mA making it superior to LEDs even for large scale integration [23].

Almost all optical computing systems require optoelectronic components in some form. Although individual circuits or small scale arrays currently

exist, what is really required is a convenient method to design and fabricate optoelectronic arrays. For large scale arrays uniformity is a bigger problem than power dissipation or optical gain. For this reason, the electronic portion of the circuit should be fabricated by a commercial foundry. Monolithically integrating LED by MBE regrowth provides a practical and economical method to fabricate large scale optoelectronic arrays with good uniformity and fast turn-around-time.

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