FLEXIBLE NEURAL IMPLANTS

Thesis by

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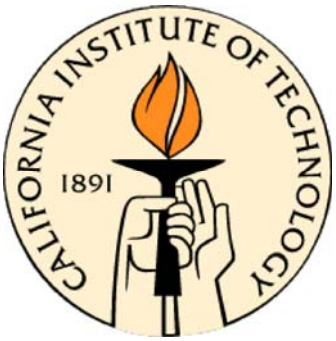
In Partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy



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To My Family and Friends

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This dissertation not only reflects the countless hours spinning photoresist, cleaning parylene machines, and mixing epoxy in Caltech Micromachining Laboratory, but it is also a conglomeration of years of wonderful experiences, opportunities, lessons, and valuable encounters during my PhD career. This endeavor would not be possible if it were not for my families, my friends, my mentors, my colleagues, and all those whom I have met over the past years.

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ABSTRACT

Despite recent development in integration technologies for biomedical implantable devices, current state-of-the-art prosthetic platforms still lack a reliable and convenient packaging scheme to integrate high-density signal-driving chips, wireless telemetry circuitries and noise-canceling amplifiers, mainly due to the limitations in fabrication technology, material compatibility and interconnect reliability. In this dissertation, new packaging technologies are developed and presented to enable a new generation of flexible neural implants. These technologies can also house integrated circuit chips and provide high-density electrical connection to it.

This packaging scheme utilizes the parylene-metal-parylene skin structure and can be totally integrated and be monolithically fabricated with existing functional devices. The size and the electrode patterns can be modified to suit different chips and applications. Integration with flexible cable integrated silicon probes for neural prosthesis, implantable muscle stimulators and implantable RFID tagging technology are all successfully demonstrated in this dissertation. Other discrete components can also be integrated to achieve high level functionality.

In order to ensure the long-term stability of such packaging scheme, accelerated hot saline soaking test is conducted on the overall structure and its components. Detailed adhesion enhancement techniques are also presented to improve its performances. A physical model of the flexible retinal implant is then tested *in vivo* during the course of the experiment. Finally, the high-density squeegee bonding technique is introduced, which allows the integration of a 256-channel chip. Functionality of the chip has been

demonstrated. As a result, this technology has the potential to achieve ultra high lead count connection and can facilitate future research in flexible implantable biodevices.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

ACIOL – anterior chamber intraocular lens

AMD – age-related macular degeneration

ASCII – American Standard Code for Information Interchange

ASIC – Application Specific Integrated Circuit

ASTM – American Society for Testing and Materials

BGA – ball grid array

CL-I^2 – Chip-level Integrated Interconnect

CMOS – complementary metal–oxide–semiconductor

CT – computed tomography

CVD – chemical vapor deposition

DIP – dual in-line package

DRIE – deep reactive ion etching

EDP – ethylene diamine pyrocatechol

FDA – Food and Drug Administration

HF – hydrofluoric acid

HNA – hydrofluoric acid, nitric acid and acetic acid

IC – integrated circuit

ID – identification

ISO – International Organization for Standardization

KOH – potassium hydroxide

LIGA – Lithographie, Galvanoformung, Abformung (Lithography, Electroplating, and Molding)

LOR – lift-off resist

MEMS – micro-electro-mechanical systems

MFI – MicroFlex interconnect

MRI – magnetic resonance imaging

MTTF – mean time to failure

PCB – printed circuit board

PDMS – polydimethylsiloxane

PR – photoresist

PSG – phosphosilicate glass

RF – radio frequency

RFID – radio frequency identification

RIE – reactive ion etching

RLC – resistor-inductor-capacitor

RP – retinitis pigmentosa

SEM – scanning electron microscope

SNR – signal-to-noise ratio

SOI – silicon on insulator

TMAH – tetramethylammonium hydroxide

TTL – transistor-transistor logic

USP – United States Pharmacopeia

WHO – World Health Organization

1 INTRODUCTION

1.1 Prosthetic Applications—The Need and Driving Force

1.1.1 Retinal Prosthesis

Two of the most common retinal degenerative defects in the world right now are age-related macular degeneration (AMD) and retinitis pigmentosa (RP). RP has already affected several hundreds of thousand people in the United States to date and AMD is estimated to cause more than several million people worldwide to have significant symptoms associated with it in the next ten years [1–3]. Even though gene therapies, drug and nutritional therapies and other types of remedies are developed [4–5] to decrease the rate of such occurrences, the defects still cause the loss of the rod and cone receptors in the eye [4, 6–8], and blindness in the long run becomes inevitable and cannot be treated.

It has been studied, however, that the ganglion cell layer, which consists of the optical nerves, remains functional even after the patient has gone completely blind and can be electrically stimulated to construct localized visual signals in patients [9–12]. Visual prosthesis, a technology that takes advantage of this fact to regains eyesight for AMD, RP and patients with other degenerative eye diseases, quickly becomes the focus for research and development around the world.

There are two main implantation and stimulation schemes in development right now to realize full visual prosthetic applications: subretinal and epiretinal, which differ by the location of the implanted devices and stimulation sites. However, regardless of the

location of the implant, the basic system components of this application remain the same. A camera is mounted on an external mount (such as a pair of glasses) and is powered to take videos and pictures to generate the raw signals that are to be sent into the eye. This signal is then passed into a circuitry box where it is analyzed and stimulation signals are generated. The stimulation signal will then be passed to the stimulation electrodes to excite the retinal ganglion cells [13–14].

1.1.2 Neural Prosthesis

Diseases, traumatic incidents and natural defects cause the interruption of information flow between the brain, nerves, spinal cords, muscles and sensors in human body. This disconnection have been one of the top priorities for research with goals to develop treatments and rehabilitation methods to either reverse, treat or to alleviate the symptoms and to improve the quality of life of the patients. As early as the 18th century, it was discovered that the use of external electrical stimulation has the potential to overcome paralysis [15]. Since then, a series of technical aids such as neural prosthesis have been developed to bridge the gap between the generation of the biological signals from the brain and the stimulation of the muscles.

Neural probe is one of the most common apparatus to conduct neural prosthetic for either recording or stimulation in the brain. This technology makes it possible to use cellular recording of the activities of individual or groups of neurons in specific areas of the brain to help scientists gain deeper understandings of the brain [16–23]. Regardless of the type of recording or stimulation electrodes that are inserted into the subject's body, the system requires at least (1) a series of electrodes to either sense and/or emit the signal; (2) implant package for all the microelectronics for control and (3) interconnects that

connects the different parts of the system. Silicon probe systems developed by University of Michigan [24–46], University of Utah [47–54] and SOI probe [55–58] and polymer probe systems [59–62] all have reported functionality and recording/stimulating capabilities in animal subjects and are expected to make great contributions in neural prosthesis research.

Finally, both neural and retinal prosthetic application are expected and required to be biostable and biocompatible. In-depth research is currently being conducted to realize a fully functional and reliable long-term implantation that is able to both record and stimulate neurons to achieve a total neural prosthetic system.

1.2 Integration Technology

One of the biggest obstacles that the prosthetic systems mentioned in the previous section has to overcome is the integration of circuitries with the biodevices to be implantable in human body. Cochlear implants, which have been commercially available since the 1980s, require only 5 to 6 stimulating electrodes to be able to regain hearing capability of an impaired patient [63]. The integration of circuitry is outside the subject and only the electrodes are implanted inside. Neural and retinal prosthetic applications, however, require hundreds or even thousands of electrodes to be connected and controlled at the same time to achieve minimal working functions [64]. In addition, in order to avoid possible infections and medical complications from percutaneous implantation schemes, the devices have to be completely inside the subject's body. This means the need for integration, connection and packaging of integrated circuit chips in this biodevice system is imminent and cannot be ignored.

Before more advanced techniques such as those discussed in this dissertation were invented, wire wrapping and point-to-point circuit construction was used to realize systems with more than several components [63]. As more complicated and intricate circuits are designed for more advance functionalities, and as more needs for smaller and faster components are demanded, traditional circuit integration methods become obsolete and are unable to be utilized for easy and mass production. The following sections introduce some of the techniques utilized today that were invented for integrating and assembling larger scale, general circuit components. Some specific technologies for bonding IC chips with devices that are used in biomedical fields and more specifically, prosthetic applications are also presented.

1.2.1 Traditional Chip Integration Technology

(a) Soldering

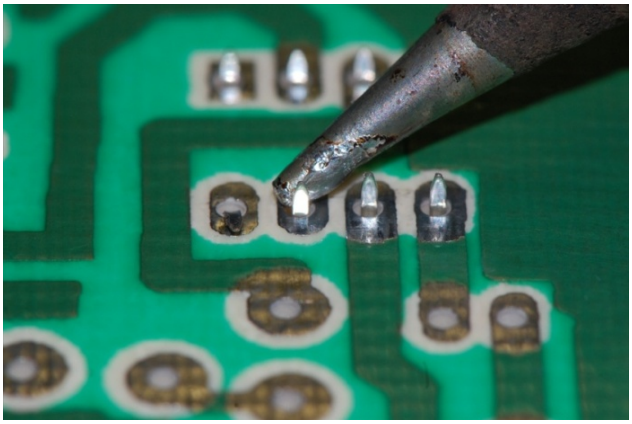


Figure 1.1. Soldering a component onto the back of a printed circuit board.
(Courtesy of Wynn Rostek)

Soldering is one of the most widely utilized interconnect technology for printed circuit boards and electronic components. The connection is formed by melting a filler material (solder) (figure 1.1) that would mechanically and electrically connect the target component onto a metal pad. Its biggest advantage is the ease of application for quick and

dirty bonding of discrete components, but the physical weakness of the solder bonding, toxicity of the materials, localized heat during assembly and its inability to connect small and dense array pads makes soldering a less attractive alternative than other more advanced technologies.

(b) Wire Bonding

Wire bonding is considered one of the most cost effective, flexible and efficient interconnect technology to be used in making connection between a printed circuit board and an integrated circuit chip after soldering technology. In wire bonding, a metal wire (usually gold, aluminum or copper) is fed through the wire bonding machine application tip and is pressed onto the target metal contact pads with electrically generated heat or ultrasonic vibration to form electrical and mechanical contact (figure 1.2). This step is repeated again at the second point of contact to complete a bond. This technology is most useful and most cost efficient in making small number of connection on big substrates and is most commonly used in bonding bare dies in DIP packages.

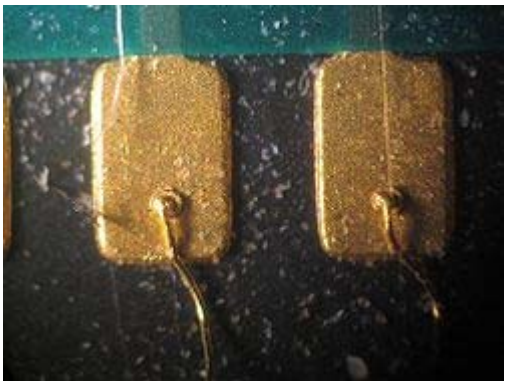


Figure 1.2. Gold wire bonded onto metal pads to make electrical connections.

(c) Ball Grid Array

In ball grid array technology, the pins that were traditionally used on printed circuit boards and the metals pads on bare IC chips are replaced by or appended with

balls of solder on the bottom of the package. This package is then placed on another printed circuit board or a substrate with metal pads patterns that matches the solder ball patterns (figure 1.3). In order to make mechanical and electrical connection, the entire structure is then heated to melt the solder ball. Surface tension would then align the package with the substrate, thus completing the interconnection. One of the biggest advantages of this approach is the density of leads it is able to achieve. Its need to heat up the substrate, however, posts limitation on the material and the process that is compatible with this technology.

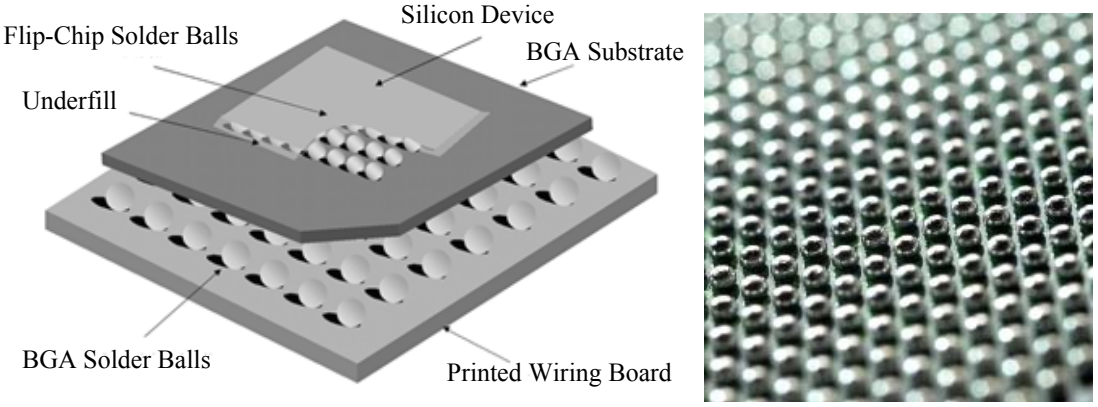


Figure 1.3. (left) Illustration of the ball grid array; (right) the BGA on an actual IC chip. (Image courtesy of ThomasNet and Dominic Plunkett from www.xjtag.com)

1.2.2 State-of-the-Art Chip Integration Technologies with Biodevices

(a) University of Michigan—The Michigan Probes

K. D. Wise at University of Michigan has developed a variety of penetrating electrode in different layouts for neural prosthetics. This endeavor started as early as 1969 in Stanford University [32] and has evolved into complete systems fully integrated with IC circuitries on the same silicon substrate (figure 1.4). The interconnections of these circuitries are made with a ~4–5 μm thick polysilicon cable. Weaknesses of this silicon-film cable are apparent since they are too brittle and are prone to breakage.

The silicon probes developed at the University of Michigan have recently adapted polymer cables [65]. These silicon probes are fully capable of simulating and recording from neural tissues and muscles. Much *in vivo* testing on animal subjects has been successfully conducted. However, the devices are still very difficult to make and require expensive process and equipment to realize; mainly due to the low yield in combining CMOS and MEMS process and the cost of materials.

On the other hand, University of Michigan has recently developed technologies to create electrical connection to a chip that is made separately from the cable and the probe itself [66], signifying a need for improvement for a higher density and easier bonding technique.

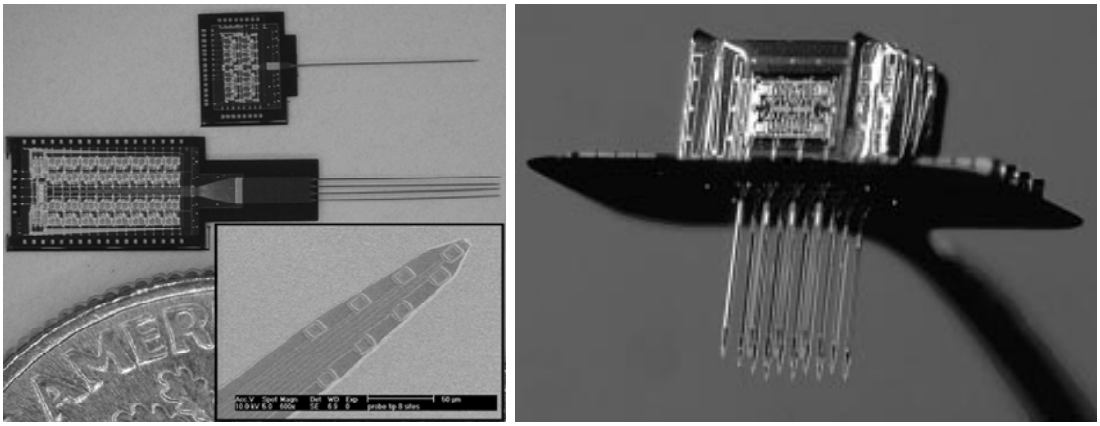


Figure 1.4. (left) The Michigan three-dimensional neural probe array [40]; (right) SEM picture of the tip of the Michigan probe [33].

(b) California Institute of Technology—CL-I^2

Li et al., with collaboration with the Doheny Eye Institute and University of Southern California Medical Center, has developed an embedded chip technology to integrate commercially available IC chips with polymer substrates and passive components [67]. A placement cavity is etched on the parylene-on-silicon substrate for chip placement. Once the chip is fixed inside the cavity, metal is deposited and a

photolithography step is done to make electrical connection between the pads on the chip and outside components. The traces run between two parylene layers and is well protected. The structure is released by back etching of the silicon substrate (figure 1.5).

The parylene substrate to be integrated with the chip is a parylene-metal-parylene sandwich layer that has been well characterized both *in vitro* and *in vivo* and is also approved by the FDA for long-term human implantations. Several chronic and acute devices tested with histology results have also been published to verify the overall biocompatibility and the feasibility of the sandwich layer technology.

However, the alignment problem that arises during the "chip-drop" could severely affect the feasibility of this technology. Not only would the surface flatness inside the cavity limit the metal connectivity over a step, but the low alignment efficiency of the bonding pads on the chip with the metal in the parylene sandwich layer renders the integration inefficient.

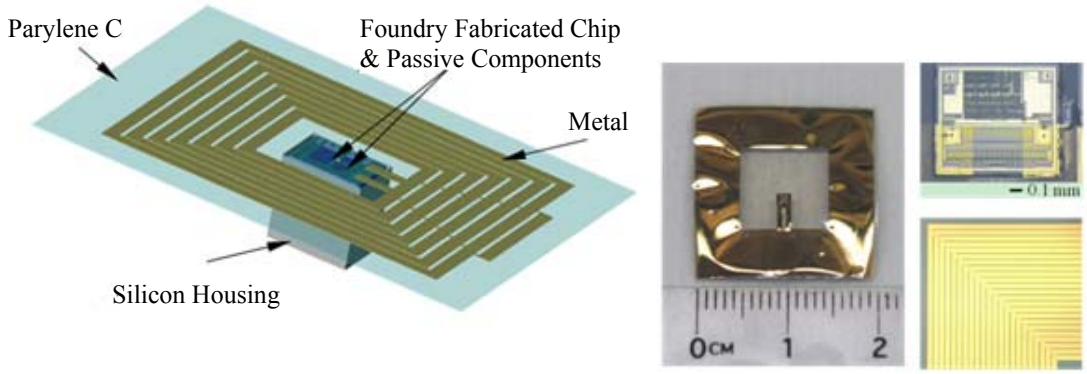


Figure 1.5. Concept of embedded chip integration; (left) overall view of the device; (middle) close-up view of the embedded chip; (right) close-up view of the coil wires.

(c) Microflex Interconnect

Microflex (MFI) is an interconnect technology developed by the Fraunhofer Institute for Biomedical Engineering; Meyer et al. [68] utilizes a polyimide substrate with

photolithography patterned metal embedded in it. The pitch and the shape of the metal pads correspond to the bonding pads on the chip. The via-hole on the substrate contact pads is then filled with metal balls or wedges applied by a commercial wire bonder to make the electrical and mechanical contact. This technology, though very similar to wire bonding, is specifically developed to integrate the passive and active electronic components to the electrodes (figure 1.6).

Since this technology is based on polyimide process, it is compatible for biomedical implants. This substrate has passed cytotoxicity testing according to ISO 10993, has been soaked more than 4 years in saline solution and has been implanted for more than 10 months in rats. The MicroFlex technology can also be applied to three-dimensional structures and the density is comparable to that of the flip chip technology. Several ultrasound array sensors, retinal stimulators (EPIRET) and multiplexer modules have been integrated successfully with this technology [68–71].

Their current device, called the EPIRET 3, has transmitting coils on external glasses and an internal receiver coil and chip secured in the eye in place of the lens (figure 1.7). As with all epiretinal prosthesis, the electrode array is tacked onto the back of the retina. In an exploratory human trial in 2009, the device was implanted for four weeks to observe the safety of the device and how well it would work. There was mild inflammatory response in some of the six subjects, but they decided there was no lasting damage from the prosthesis. Four of the six subjects gained light perception, one gained hand movement, and one had no light perception [72].

However, more clinical trials are still needed to demonstrate the long-term performances of implants. The mechanical properties of the bond on the substrate have

yet to be tested as well. There are also several other issues including alignment and overall packaging that needs to be considered before this technology can be reliably long-term implanted for chronic use.

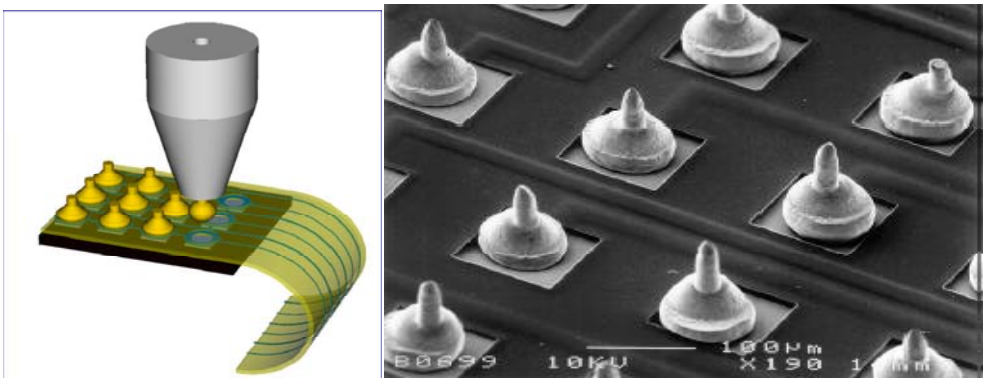


Figure 1.6. Close-up picture of the MicroFlex bonding technique, facilitated by a commercial wire bonding machine setup [70].

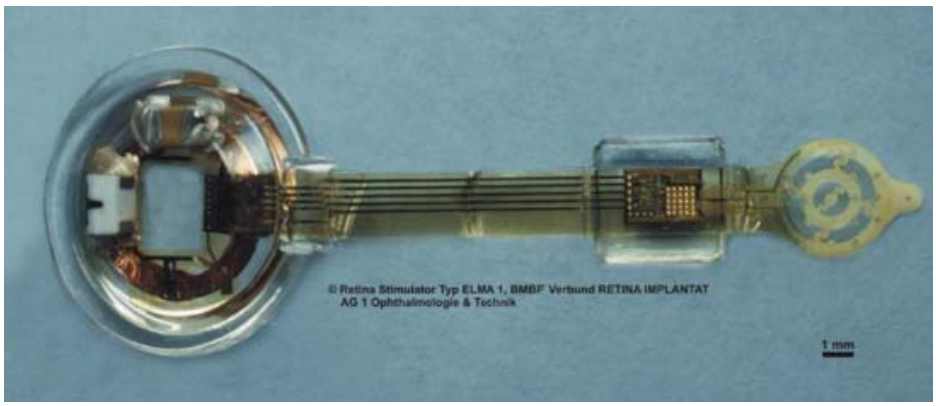


Figure 1.7. Final implant with parylene C and silicone rubber encapsulation [71].

(d) Boston Retinal Implant Project

Dr. Wyatt and Dr. Rizzo from Massachusetts Institute of Technology developed a subretinal implant device that aims to achieve visual prosthesis [73]. The polyimide device substrate hosts all the system components, which are connected via 50 μm wide Cu/Ni/Au metallization traces. As shown in figure 1.8, the ASICs on the left-hand side were mounted by stud bumping with 75 μm high Au bumps, followed by flip chip die attachment to the host substrate. Stud bumping was also used for the flex-to-flex

connections between the flex circuits and the electrode arrays. Nonconductive epoxy was used to encapsulate the entire device and then coated in PDMS (polydimethylsiloxane).

Although this device has been through several *in vivo* studies, the integration approach proved to be prone to reliability problems. Also, the lifetime of the encapsulation coating (PDMS) has subpar performance relative to other biocompatible coatings.

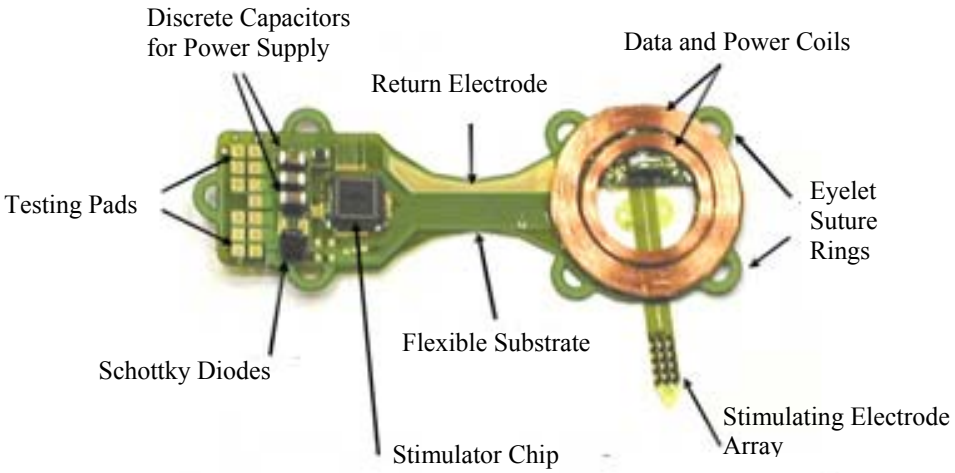


Figure 1.8. Schematic representation of the retinal implant by Theogarajan et al. [73].

(e) Other Technologies

Deguchi et al. from Tohuku University in Japan have developed a one-piece, stacked retinal prosthesis chip system to be implanted in human eye [74]. It consists of implantable IC chips responsible for photodetection, image processing, current generation and stimulating arrays (figure 1.9a). While implanting the entire chip into the eye eliminates the need for integration of flexible electrodes with circuitry, the hard substrate that comes along with this stacking technology makes it more damaging to the tissues and less surgically friendly.

A pressure monitoring system integrated in a small package has been developed by Schlierf et al. [75]. The package comprises a sensor ASIC, which includes a capacitive

absolute pressure sensor with an inductive telemetry unity and other passive components in different packaging (figure 1.9b). These components are soldered onto the underlying substrate, which is then subsequently encapsulated in a biocompatible silicone and parylene coated. While the system performed satisfactory *in vitro*, the packaging mechanism cannot be scaled to accommodate smaller components and IC chips with higher number of leads.

Other research groups worldwide have also developed different schemes for varieties of biomedical implants and prosthetic devices. The basic idea is to minimize the number of electronic components and the size of the packaging without compromising the functionality of the overall device. While many of these devices have good functionality and short-term stability, clinical trials still needs to be demonstrated for both animal and human models for long-term reliability and performance evaluations.

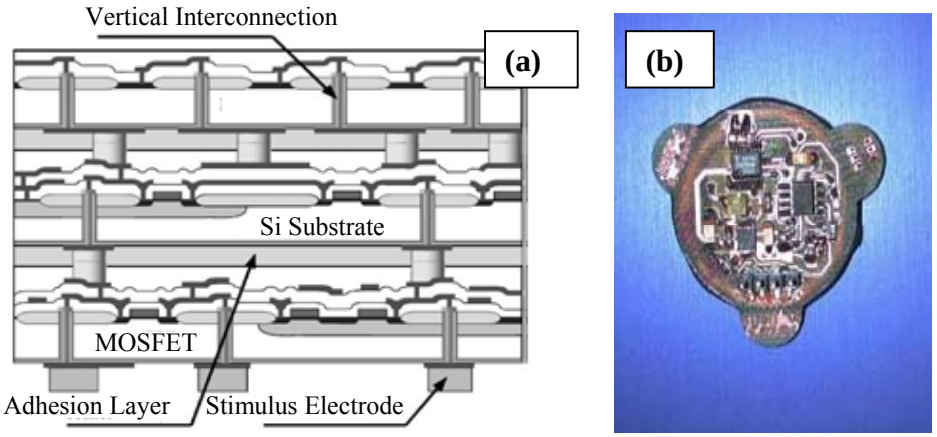


Figure 1.9. (a) Schematic of the three-dimensional stacked chip [74]; (b) implantable sensor system: A control unit and analogue part with RF coil [75].

1.3 Problems and Challenges

Next generation retinal prosthesis development will require totally implanted devices to minimize inflammations and surgical complexity as well as the physical damages incurred on the receiving subject during surgeries and procedures. This means the

telemetry circuit, along with signal processing and the stimulation circuit and a stimulation electrode all would have to eventually be fit inside a human eyeball (<1–2 cm^3). MEMS technology, which will be discussed in the next section, is not only a great candidate to miniaturize the system, but it has also been utilized to increase the precision and the ease of fabrication of such implantable devices. In fact, MEMS has become one of the most crucial technologies that would foster the success of the development of a reliable implantable system.

However, although numerous implantable devices have been developed with micro-electrical-mechanical system technology to integrate IC with bioimplantable microfabricated devices, there still lacks an enabling packaging technology that is able to meet all of the requirements that are demanded by current state-of-the-art retinal and neural implantable systems. First of all, the analog/digital driving electronics must be in a hermetic package/encapsulant, protected from the saline environment of the body since this package needs to address the long-term biocompatibility and reliability issue in the human body. It is necessary to develop a technique to protect these implanted components from the corrosive substances, like body fluid. As it is discussed later in the chapter, parylene C, a biocompatible polymer, is selected as the main structural and packaging material because of its many favorable properties. By doing so, the package will be mechanically stable within the tissue without causing damage either to the device or to the patient.

Secondly, this hermetic packaging must also have a large number of feed-through connections for the electrical signals and to enable connection to the inductively coupled coils and other passive devices such as chip capacitors. A conservative estimate of pixel density will be 32 × 32 to enable blind individuals to better carry out activities of daily

living [76]. This is a density and number that has yet been fully attempted. It must also connect with an electrode array, either a flexible substrate or a stiff device, and the material used to insulate and stabilize this connection must be biocompatible. Furthermore, current interconnect and packaging technologies are labor-intensive, inefficient, and costly, limiting the achievable device resolution.

In addition, a compatible process must be developed to build implantable devices that can integrate other discrete components (application specific integrated circuits (ASICs), capacitors, etc.) and can withstand adverse human implant environment reliably for many years. The insulating material must not corrode, dissolve, or leak; parylene C, a MEMS compatible material, provides just the right solution to solve this problem.

In conclusion, it is clear that for the state-of-the-art implantable systems on this scale, it has become not only a trend, but a necessity to utilize MEMS technology to fabricate microelectrodes and its packaging schemes. The next section will be devoted to the discussion of this technology with a focus on parylene.

1.4 MEMS Technology

MEMS (Micro-Electrical-Mechanical Systems) encompass miniaturized systems that consist of both electrical parts and mechanical parts. These parts may include elements such as sensors, actuators, fluidic channels and electronics that are fabricated or integrated on a substrate such as silicon by means of microfabrication technology, with typical dimensions ranging from 0.1 to 100 micrometers in size. The history of MEMS started shortly after the realization of transistors in 1947 and has fully taken off since then. Much attention of MEMS was also brought to light after the talk by Richard Feynman's "There's plenty of room at the bottom," which lays out the fundamentals of system

miniaturization. The design of MEMS is different from the design of systems of a larger scale. This is due to the fact that the surface area of a miniaturized structure is much greater than its volume and causes the reduction of mass and inertial volume effects but increases the electrostatic and wetting surface effects of the system.

There are countless advantages from using MEMS technology. Not only does it enable the communication between mechanical and electrical elements on the same substrate in a system, it also has lower cost, is smaller in size, mass and power consumption, and has higher functionality, reliability and precision. Because of these advantages, numerous devices such as micromotor [77], accelerometer [78], pressure sensors [79] and RF filters are realized.

Because of its root in the IC industry, many of MEMS basic processing techniques are borrowed or adapted from IC technology, such as photolithography, oxidation, diffusion, ion implantation, chemical vapor deposition (CVD), evaporation, sputtering, wet chemical etching, and dry plasma etching. There are, however, features that one may encounter in MEMS fabrication process that are uncommon in integrated circuit fabrication such as nonplanar substrate (i.e., relatively large three-dimensional features); the use of thick photoresist layers (for structure purposes or for long etching time); relatively high aspect ratio structures; relatively large feature sizes and unusual materials (particularly important in terms of adhesion). Traditional MEMS process, along with several special processes such as deep reactive ion etching (DRIE), LIGA, electroplating, and soft lithography have been developed to support these uncommon features.

Before any MEMS specific process can be brought to discussion, the most essential step in the process is the photolithography step. This step provides pattern resolutions high enough to achieve miniaturization, which is done with photodefinable compounds called photoresist. Photoresist is a light sensitive material that can be selectively removed by shining light at specific wavelengths on desired areas. Depending on if this material is "positive" or "negative," areas that are shined with light will be removed from or will remain on the substrate, respectively (figure 1.10).

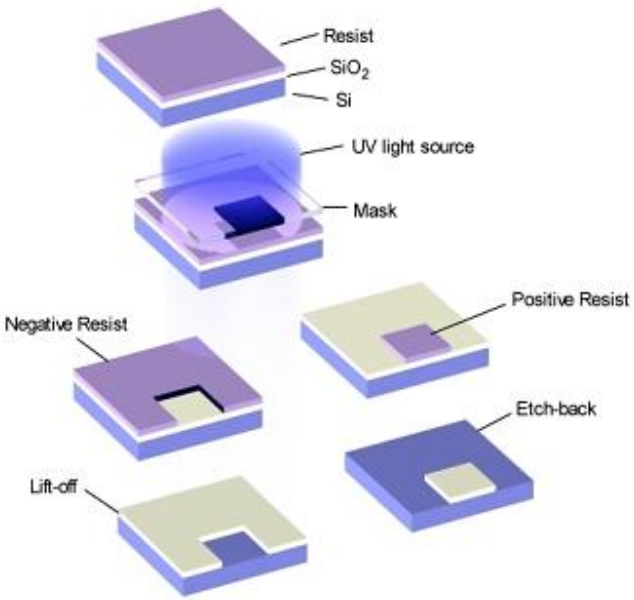


Figure 1.10. Comparison of positive and negative photoresist.
(Courtesy of NCSU Soft lithography Wiki)

The most noticeable difference of the fabrication process of MEMS from traditional integrated circuit fabrication is the ability to modify the substrate with the two basic techniques: surface micromachining and bulk micromachining (figure 1.11).

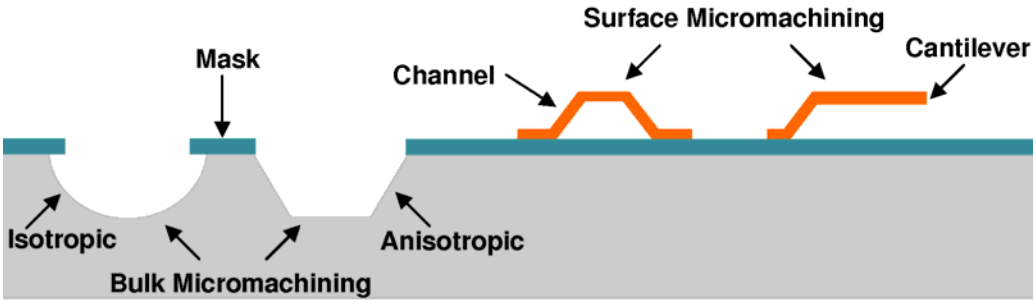


Figure 1.11. Comparison of surface micromachining and bulk micromachining.

1.4.1 Bulk Micromachining

Bulk micromachining takes advantage of all three dimensions of the bulk material and creates features inside the substrate (top-down machining) by etching. Single crystalline silicon is the most common material used in MEMS processing because of its ability to be easily etched. Etching can be separated into two categories: isotropic etching and anisotropic etching; both of these etchings can be achieved in a wet or dry environment (figure 1.12).

In isotropic wet etching, where the etching rates in all directions in the substrate are the same, etchants such as HNA (hydrofluoric acid + nitric acid + acetic acid) are used. In anisotropic etching, where the etching rate differs by the direction of the crystal plane, wet etchant such as solutions of KOH (potassium hydroxide), EDP (ethylene diamine pyrocatechol), TMAH (tetra-methyl-ammonium-hydroxide), and hydrazine-water are used. By combining anisotropic etching with etching stops such as boron implantation (P+ etch-stop) and other electro-chemical etch-stop technique, varied silicon microstructures can be bulk machined.

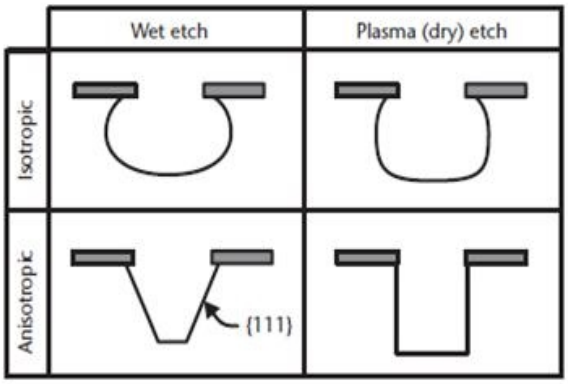


Figure 1.12. Comparison of isotropic and anisotropic wet etching and dry etching. (Courtesy of An Introduction to MEMs Engineering—Nadim Maluf and Kirt Williams)

Etching can also be achieved by dry etching, which can be separated into three classes called reactive ion etching, sputter etching and vapor phase etching depending on the different chemical and physical interactions between the ions of the gas and the atoms on the substrate. In reactive ion etching, external energy generated by RF (radio frequency) power induces chemical reaction in low-pressure reaction chambers between the gaseous ions and the atoms on the target substrate. Some physical bombardment of the gaseous ion onto the target substrate also occurs. In this process, gases such as chlorofluorocarbon gases, sulfur hexafluoride, bromine compounds and oxygen are commonly used as reactants. Sputter etching, on the other hand, is very similar to reactive ion etching, except that the process is made up entirely of the physical bombardment of the ions without any chemical interactions. In vapor phase etching, the substrate is placed inside the chamber where the gas is present, and is dissolved at the surface in a chemical reaction with the gas molecules. This process is made possible by using XeF_2 [80] (xenon difluoride) or a mixture of interhalogen gases (such as BrF_3), which provide very high selectivities for aluminum, silicon dioxide, photoresist and other masking materials used during etching. Examples of bulk micromachining can be seen in figure 1.13.

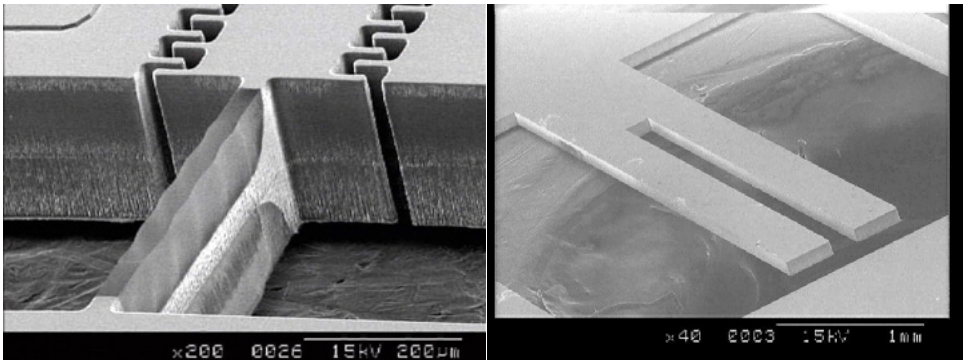


Figure 1.13. Examples of silicon bulk micromachining; the substrate material is etched away to create different features [81].

1.4.2 Surface Micromachining

Surface micromachining, unlike bulk micromachining where features are inside the substrate, is based on the deposition and etching of different structural layers on top of the substrate (bottom-up processing). Because the process does not depend on the etching characteristic of the substrate, different materials such as soda lime, silicon on insulator and metals are sometimes used in this process.

During surface micromachining process, the layers deposited may be metal, oxide, polymer or other process compatible materials. These layers are selectively etched by photolithography with a mask by either a wet etch involving an acid or a dry etch involving an ionized gas or plasma. When a suspended structure is necessary, sacrificial layers are used (figure 1.14). These sacrificial materials must have process-compatible properties such as good adhesion to substrate or low residual stress, to avoid failure during fabrications. Common sacrificial materials are photoresist, polyimide, metals, phosphosilicate glass (PSG) and polysilicon.

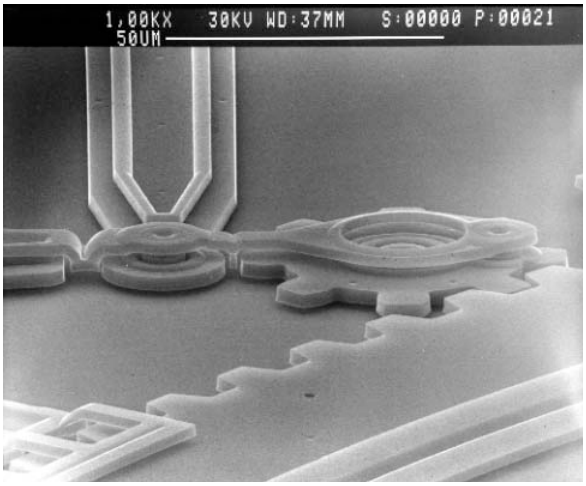


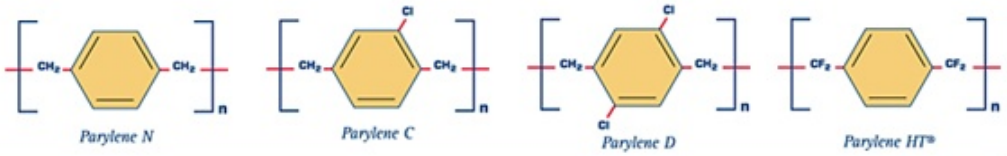
Figure 1.14. An example of surface micromachined gears [82].

Finally, by combining steps of material deposition, photolithography, material etching/removal, and necessary cleaning steps, two-dimensional masks can be used to extrude and fabricate complex devices in three dimensions.

1.4.3 Introduction to Parylene

Parylene was discovered by Dr. Michael Mojzesz Szwarc at the University of Manchester, England, in 1947 and commercialized by Union Carbide Corporation in 1965 [83] and is a generic name for a family of polyxylylene polymers. Its primary application is in the electronics industry for protection of PCB (printed circuit boards) against moisture and corrosive environments. There are more than seven types of commercially available parylene dimer to date; the most well-known ones include parylene C, parylene N, parylene D and parylene HT. As shown in figure 1.15, parylene N is poly-para-xylylene, a completely linear and highly crystalline polymer, where parylene C and parylene D are variants of parylene N with one and two chlorine atom in place of the aromatic hydrogen atoms, respectively. The benzene backbone of the parylene molecules makes them very chemically inert, while the polyethylene-like interconnect makes them flexible.

Parylene is deposited at room temperature with a chemical vapor deposition process called Gorham process [84]. In this vacuum process (~25–35 mT, to increase mean free path to the substrate) (diagrammed in figure 1.16), raw dimer material is placed in a vaporizer furnace, and evaporated to a dimeric gas at approximately 130 to 150ºC. This gas then passes through a high-temperature pyrolysis (~650 to 750ºC) furnace, where the molecule is split into monomers. The monomers enter a chamber that is held at room temperature, and polymerize on all exposed surfaces in the chamber conformally without pinholes. Residual monomer is collected on a cold trap before it enters the mechanical vacuum pump to prevent damage. Parylene coating thickness often ranges from several hundreds of nanometers to tens of micrometers and can be controlled by the amount of the dimer placed in the evaporation chamber. By changing the deposition chamber pressure, the deposition rate and the density of parylene can also be controlled. Different variants of parylene require varying process conditions, but the method remains essentially the same.



	Parylene N	Parylene C	Parylene D	Parylene HT®
Vaporizer	170°C	170°C	170°C	155°C
Pyrolysis	650°C	690°C	700°C	750°C

Figure 1.15. Chemical structures of parylene N, C, D, and HT, and some of the correlated process parameters used in parylene deposition system PDS 2010 and 2060.

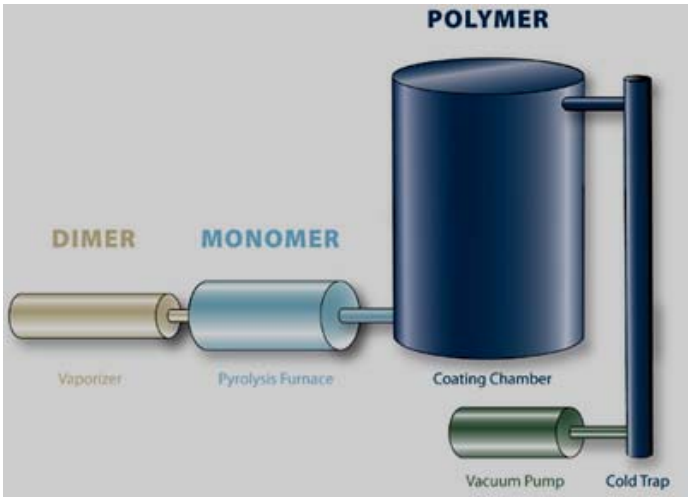


Figure 1.16. Parylene deposition system and its deposition process.

The properties of the different species of parylene are listed in table 1.1 to compare with PDMS (polydimethylsiloxane), a material that has been traditionally used in biomedical applications. Not only is parylene superior in many aspects than PDMS and polyimide [85] such as pinhole-free conformal deposition, low gas and water vapor permeability, and chemical inertness, it is also transparent in the visible light range. These desirable characteristics make it a perfect candidate for protecting implanted devices and electronics from corrosive agents and body fluids. With Young's modulus of 2–3 GPa and an elongation-to-break percentage of more than 200%, parylene C also acts as a perfect membrane material for large deflection applications.

To summarize, due to the different chemical structure of the different species of parylene, different applications and uses are realized. Parylene N has excellent crevice penetration ability, thus is primarily used as a dielectric and when lubricity is important, but has the slowest deposition rate among all species. Parylene D has superior mechanical strength and can withstand higher temperature than others, but has been largely replaced by parylene HT [86]. Parylene C, having a useful combination of electrical, mechanical and water barrier properties, is also an ISO 10993, United States Pharmacopeia (USP)

Class VI material (the highest biocompatibility rating for plastics in the United States). Parylene HT is the new favorite with its excellent thermal stability, water barrier property, high ultraviolet stability, better electrical and crevice penetration property, lower coefficients of static and kinetic friction, and is also ISO 10993 biocompatible [87–88].

Table 1.1. Properties of parylene N, C, D, HT, and PDMS.
(Table and data adopted from [89–91])

Property	Parylene N	Parylene C	Parylene D	Parylene HT	PDMS
Dielectric Strength (V/mil), 1 mil film	7,000	5,600	5,500	5,400	610 (1 mm film)
Dielectric Constant					
60 Hz	2.65	3.15	2.84	2.21	
1 kHz	2.65	3.10	2.82	2.20	2.3–2.8
1 MHz	2.65	2.95	2.80	2.17	
Young's Modulus (psi)	350,000	400,000	380,000	--	52–126
Index of Refraction	1.661	1.639	1.669	--	1.4
Yield Strength (psi)	6,100	8,000	9,000	--	325
Elongation to Break (%)	20–250	200	10	--	210–310
Coefficient of Friction					
Static	0.25	0.29	0.33	0.145	--
Dynamic	0.25	0.29	0.31	0.130	0.43–0.51
Density (g/cm^3)	1.10–1.12	1.289	1.418	--	9.7×10^{-4}
Melting Point (ºC)	420	290	380	>450	–49.9–40
Thermal Conductivity at 25ºC (10^{-4} cal/(cm × s × ºC))	3.0	2.0	--	--	3.6
Water Absorption (% after 24 hours)	< 0.1	< 0.06	< 0.1	< 0.01	-- (depends on cure conditions)
Specific Heat at 20ºC (cal/g × ºC)	0.20	0.17	--	--	0.35

1.4.4 Parylene for MEMS and Biomedical Applications

Innate immune response from human body tissue is one of the biggest issues when conducting a biomedical implantation endeavor because of the occurrence of inflammation and scar tissues, which may either impair the functionality of the device or even cause harm to the test subject. On the other hand, the implanted device and electronics also need to be protected from corrosive body fluids, electrolytes, proteins, enzymes, and lipids for as long as the device is inside human tissue. The devices may need electrical insulation and lubrication to reduce friction as well. Thus, the biocompatibility of the packaging material that is in contact with tissue is crucial and important to the overall stability of the system.

Numerous packaging materials have been investigated to serve this purpose in many implantable applications such as pacemakers, cochlear implants, etc. From the permeability study by Ko et al. and Kazemi et al. [92–93], metal has the best hermetic sealing of electronics to be implanted in human body while generic silicone and epoxies have relatively inferior performances (figure 1.17). However, the listed materials may not meet toxicity and/or biocompatibility requirements and cannot be applied with precise control.

As mentioned in the previous section, parylene C has been widely used for coating bioimplantable devices due to its biocompatibility [94–95]. It is currently the choice for wire insulation inside pacemakers. In addition, studies from Rodger et al. [96] during an *in vivo* chronic rabbit eye implantation indicated no adverse immune response caused by implanted parylene C structures. This result further strengthens the fact that parylene C is not only suitable for implantation in the human body, but specifically for neural prostheses

and implantable devices. In addition, parylene produces no cure forces (compared to silicone and epoxy), contains no additives (no catalyst, solvents, plasticizers), is inert (no metal oxidation), lubricious and is applicable to most materials that are stable in vacuum. Finally, parylene C is the longest (~3 years) proven protective biocompatible material [97].

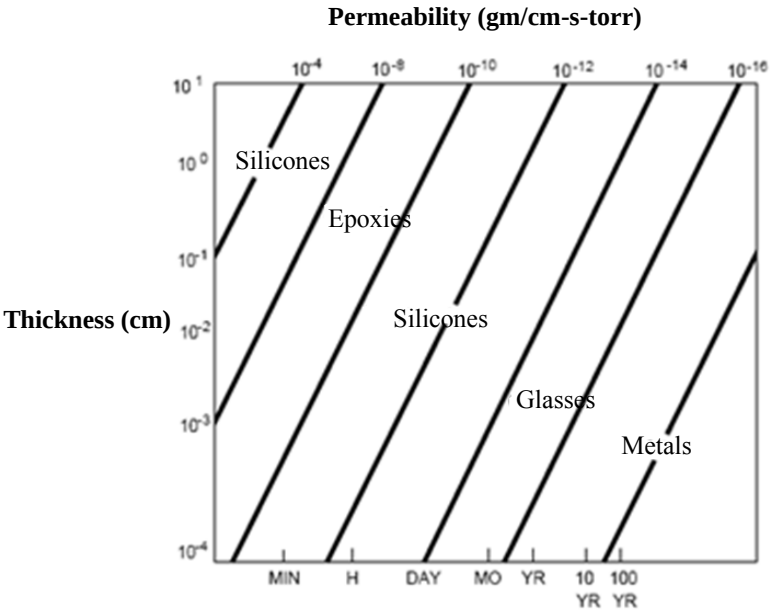


Figure 1.17. Permeability vs. time of different materials.

The possible uses of the main parylene variants for biological applications are summarized in table 1.2. It can be clearly seen that parylene C has become the choice of material to be used in biomedical and implantable device applications mainly for its biocompatibility and its good ability to block water. This further strengthens our case to use parylene C in the development of implantable device platform.

Table 1.2. Parylene coating functions for selected medical applications.
(adapted from [86])

Property	Parylene N	Parylene C	Parylene HT
Catheter mandrels	Lubricity	--	High temperature stability
Endoscopic devices	Dielectric, lubricity	--	--

Animal RFID	--	Water barrier	--
Pulse generators/ Electronic circuits	--	Water barrier, dielectric, biocompatibility	--
Pressure sensors	--	Water barrier, dielectric, biocompatibility	--
Stents	--	Biocompatibility, water barrier, primer	--
Cochlear implants	--	Water barrier, dielectric, biocompatibility	--
Blood-handling components	--	Chemical resistance, biostability	--
Needles/syringes	Lubricity	--	Lubricity, water barrier
Cannulae	Lubricity	--	--
Analytical lab components	--	Chemical resistance, biostability	--
Ocular implants	--	Biocompatibility, water barrier, dielectric, mechanical strength	Biocompatibility, water barrier, dielectric, UV stability, process temperature stability

1.5 Prosthetic Interface Technology Thrust

The overall goal of this dissertation is to develop the necessary subsystems fabrication and packaging technologies to support the implementation of neural interfaces for recording and stimulating in the retinal and cortical implantable test beds. In order to enable the long-term communication between the outside world and the neural tissue, three technologies are developed: *electrode technology*, *packaging technology,* and *radio-frequency (RF) communication technology*. In particular, these interface technologies need to be uniquely designed for both the retinal prosthesis and the cortical implantable test beds.

The system, shown in figure 1.18, consists of two MEMS radio-frequency coils for receiving wireless power and data signal, circuitry to convert control signals to stimulation

pulses and a high density MEMS electrode array for the actual stimulation of the retinal neural cells. While the electrode array has already been invented by Dr. Damien Rodger and the RF coil fabrication technology has been invented by Dr. Wen Li in the Caltech Micromachining laboratory, this work will focus on the flexible MEMS parylene-based implantable technology for pocket chip integration and its functionality demonstration, which aims to contribute to the overall initiative of realizing all prosthetic system applications including the intraocular epiretinal implantation system.

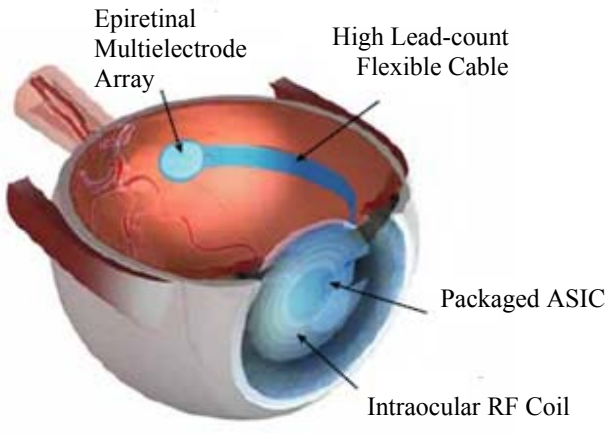


Figure 1.18. Proposed all-intraocular system for high density epiretinal implant.

1.6 Layout of the Dissertation

Chapter 2 describes the pocket fabrication technology and then discusses the variety and the versatility of the flexible pocket structure. A full integration demonstration with a flexible parylene-cabled silicon probe for a brain-machine interface is also presented. Chapter 3 demonstrates total system integration with a commercially available muscle stimulator chip and a radio frequency identification chip and discusses, in depth, their integration and packaging process. The result of their functionality testing is also presented. Chapter 4 then presents the long-term packaging reliability and the mechanical characteristic of the pocket structure and the result of the expected lifetime experiment.

Furthermore, an *in vivo* model of the intraocular epiretinal implantation system is presented. Finally, chapter 5 addresses the need for a high density packaging scheme and introduces the process to connect a 256-lead high density channel chip. Some of the technical fabrication challenges and issues are also discussed in the chapter.

1.7 Summary

Two prosthesis applications and their driving forces and needs are described in this chapter. It is shown that one of the biggest needs to push implantable prosthetic technologies to their fullest potential is a reliable, high density packaging scheme that allows stimulation and recording circuitries to be integrated with the device. Many research attempts to overcome this obstacle are discussed in this chapter. However, current state-of-the-art technology still cannot fulfill the ever-increasing need for a quick, simple and reliable high-density integration with commercially available IC chips. Parylene is believed to be the ideal candidate for enhancing the biocompatibility of these devices and is highly compatible with MEMS and micromachining technology. Therefore, a biocompatible flexible parylene pocket packaging technology based on MEMS micromachining techniques will be proposed to address these issues and challenges and to achieve total system integration in this dissertation. It is believed that this integration technology not only can fulfill the need of retinal and neural prosthetic application, but also other bioimplantable devices that require integration with external circuitries as well.

2 PARYLENE POCKET TECHNOLOGY

2.1 Introduction

Prosthetic applications require transmission of electrical signals in and out of the subject's body for the external circuitries to analyze the signal and to control the voltages and currents to stimulate muscle groups and targeted nerves via electrodes. Recent trends have indicated an increasing demand for a high number of electrodes per unit area and the migration from wired to wireless transmission, which put more emphasis on the packaging and the reliability of the integrated circuits that performs these functions. However, current state-of-the-art implantable prosthetic platforms still lack a reliable, simple and cheap packaging scheme to integrate high density signal driving chips, wireless telemetry circuitries and/or noise canceling amplifier chips to satisfy these demands. A few have a well-developed CMOS/MEMS integrated process that combines integrated circuits with MEMS fabrication technology but are very expensive and painstaking to make. On the other hand, some have no integrated circuits at all [31, 98–99]. For example, the MicroFlex interconnection (MFI) technology discussed in chapter 1 [68–69, 100], in which flexible polyimide substrates are fabricated as carriers, have individual devices mounted to the polymer substrates using bump-bonding method. While devices packaged with this technology are flexible enough, their long-term biocompatibility is not fully validated. Its tedious and low yield process also makes it difficult and costly to integrate high electrode density devices. To overcome these

challenges, we develop here a new packaging technique that utilizes a flexible parylene (chip) pocket on silicon and parylene substrate with metal pads. This pocket can both house an IC chip inside and provide electrical connections to it, and can be totally integrated and be monolithically made with existing functional structures. The pocket size and the configuration of the electrodes can be modified to suit different chips and applications and is not sensitive to dry etching flatness [67]. Another advantage of our approach over traditional methods is that the density of interconnections is limited only by photolithography resolution, which offers the potential to achieve high-lead-count (>1,000) integration. As a result, we are able to fabricate IC packaged devices that are highly customizable, fully biocompatible, and easy to mass fabricate. This will facilitate future research in developing more complex bioimplantable systems.

2.2 Pocket Design—Parylene vs. Silicon Substrate

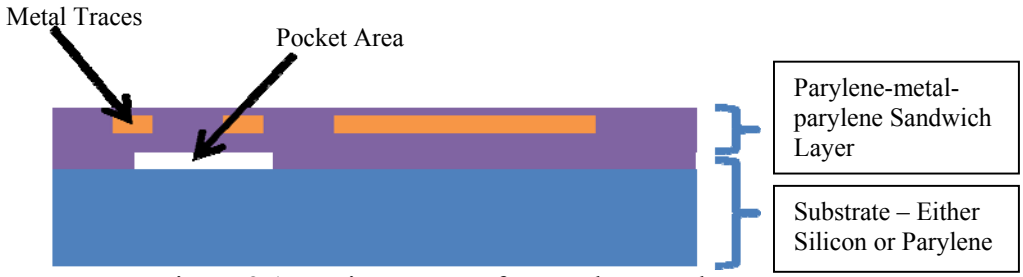


Figure 2.1. Basic structure for parylene pockets.

Figure 2.1 shows the basic structure of the parylene pocket. The basic principle behind parylene pocket fabrication is the same for both silicon and parylene substrate. In both processes, a parylene-metal-parylene sandwich skin [101] is deposited on the substrate with a sacrificial layer that resides in between. The sacrificial layer is removed by the end of the process to create the pocket cavity that accommodates external IC chips. Pockets with parylene substrate and silicon substrate can be made depending on application and physical size of the IC chip. From experience, chips that are very thin

(less than 250 μm) and have relatively small surface area (less than 2 mm × 2 mm) are easier to assemble and integrate with pockets with silicon substrate as it provides a good mechanical support to maneuver the chips inside the pocket for alignment and bonding. Pockets with parylene substrate are recommended for chips that are thicker and larger in size, since the real estate required for silicon substrate grows exponentially as the thickness and the size of the IC chip increases. For example, a pocket with parylene substrate of 1 cm × 1 cm is able to accommodate a 5 mm × 5 mm × 700 μm IC chip when a pocket with silicon substrate would need a 2.3 cm × 1.6 cm real estate to achieve the same goal. It should be noted that only pocket structure with parylene substrate is completely flexible, and is generally preferred in implantable applications.

The pocket presented first in this chapter was designed to fit a 500 μm thick, 0.5 mm × 0.5 mm sized 16-channel amplifier integrated circuit chip (figure 2.2) designed by Dr. Wentai Liu's group in University of California, Santa Cruz [102]. The signals from 16 channels are amplified by the low-noise amplifier of voltage gain 50. The fabrication process of the parylene pocket for both silicon and parylene substrate are demonstrated. An assembly process was also developed to integrate and assemble these components into a fully functional platform for neural signal recording. The combined thickness of the parylene C skin [103] and pocket is 25 μm with gold metal connection traces embedded.

Numerous skin technologies have also been developed by other research groups worldwide [104–106]. But we have found parylene to be the ideal candidate for our application because of its better mechanical properties and its superior soaking mean time to failure in accelerated soaking tests [107].

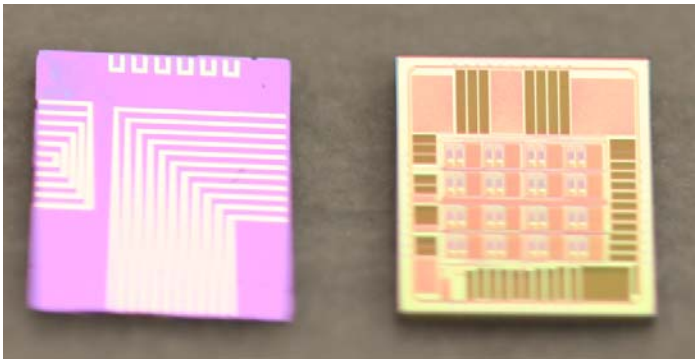


Figure 2.2. (left) Conduction chip and (right) the CMOS amplifier chip used in the testing of the devices. The conduction chip was made in-house with electron beam evapoator metal deposition on oxide wafer and DRIE process.

2.3 Fabrication

2.3.1 First Generation

The parylene pocket configuration is fabricated with DRIE and RIE technology. Figure 2.3 shows the fabrication process for parylene pocket with silicon substrate. First, a sacrificial photoresist layer is spin-coated on the silicon substrate for pocket releasing. A bottom layer of parylene C (5 μm) is then deposited, followed by Cr/Au (0.05/0.2 μm) lift-off process with electron beam evaporation to provide electrical connection. The top layer of parylene C (5 μm) is deposited to complete the parylene-metal-parylene sandwich skin structure. Electrode sites and the device definition are then opened by a two-step RIE with O_2 plasma process. The outline of the parylene pocket structure is subsequently etched by DRIE with Bosch Process (Unaxis Corporation, St. Petersburg, FL, USA) [108] from both sides of the wafer. In the final step, the devices are released in photoresist stripper and dried. An IC chip is then inserted by hand into the parylene pocket.

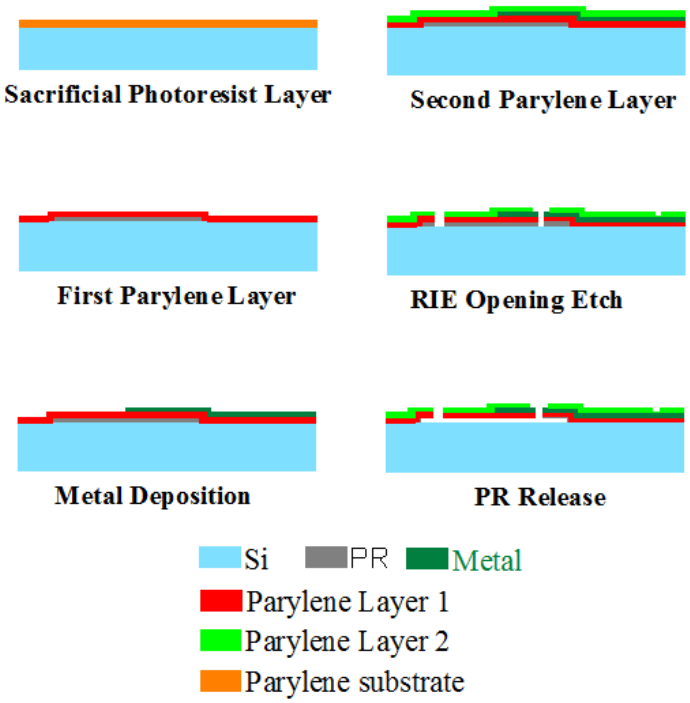


Figure 2.3. Process steps for parylene pocket with silicon substrate. The entire pocket structure can be released from the wafer by DRIE or wafer dicing.

The first-generation parylene pocket, however, has some design flaws that prevent it from functioning properly (the device is shown in figure 2.4). First of all, the pocket does not have enough stress relief to accommodate the thickness of the IC chip that is to be integrated inside the pocket. The insertion process causes damage on the side of the parylene pocket causing it to tear and break and would increase the chance of leakage and compromises the packaging. The conduction traces on the side are also broken as a consequence. In addition, the pocket area is not properly released due to the lack of openings for the solutions to dissolve the photoresist underneath. This causes the pocket to be physically stuck on the silicon substrate surface and prevents the chip from being inserted and aligned to the right position; the pocket may eventually be damaged (figure 2.5). Finally, the parylene near the edge of the device does not adhere well to the silicon substrate and causes delamination after releasing the device in the photoresist stripper.

All of these problems will be addressed in the second version of the device, where an additional stress relief opening will be added to the device.

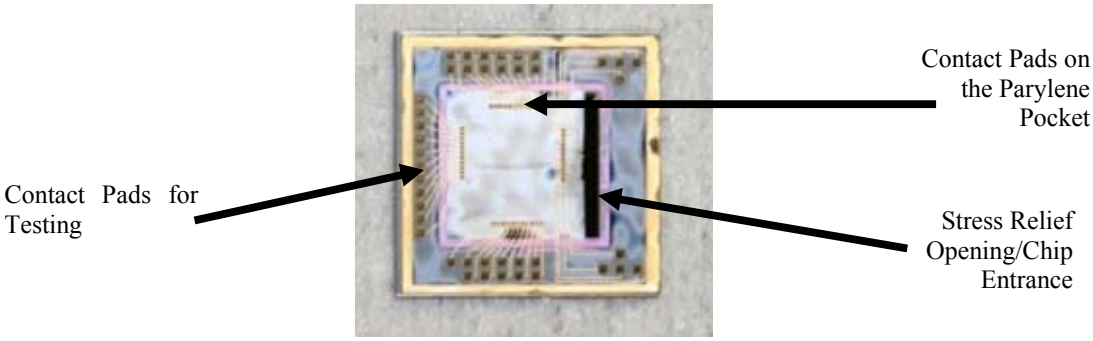


Figure 2.4. The first-generation parylene pocket with one opening on the side; all bonding pads are located on the chip.

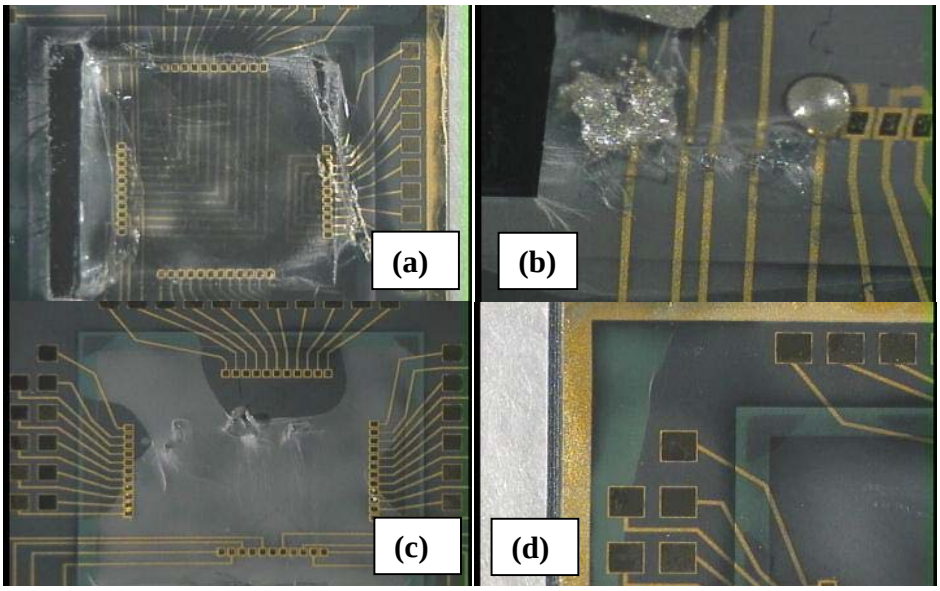


Figure 2.5. Issues during fabrication and chip insertion; (a) chip insertion tearing the side of the pocket, causing breakage of the parylene; (b) open circuits in trace lines; (c) the parylene substrate is stuck on the surface of the silicon substrate; (d) delamination of the parylene pocket from the silicon substrate.

Additional treatments such as melted parylene and parylene surface roughing are needed to ensure good adhesion between the sandwich skin layer and the substrate. After the devices are released and the IC chip integrated into the pocket, protective layers and biocompatible materials are deposited on the structure. Only after these protective

treatments can we fully utilize these packaged IC chips in long-term implantation for prosthetic applications.

2.3.2 Second Generation—Silicon Substrate

In the second generation, stress relief openings are placed on both sides of the pocket to facilitate the insertion of the chip (figure 2.6). After the chip is inserted by hand into the pocket, it is aligned (figure 2.7), bonded with conductive epoxy (figure 2.8) and totally coated with parylene C again for complete encapsulation and to ensure biocompatibility. The fabrication step is similar to that of the version one pocket structure with the exception of an additional melted parylene adhesion layer before the photoresist coating to enhance bonding strength of parylene on silicon. This enhancement process and its performance characterization will be discussed in length in chapter 4.

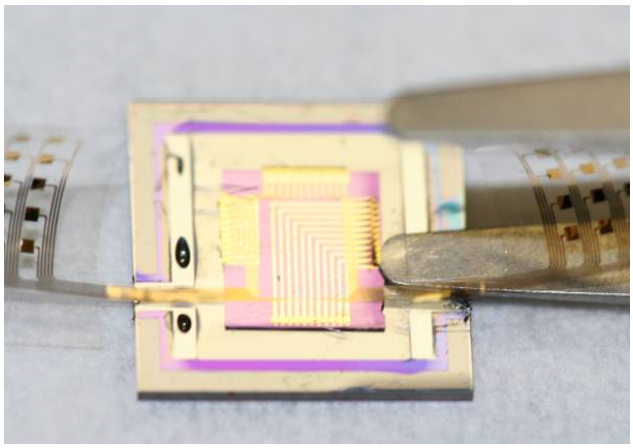


Figure 2.6. Insertion of the IC chip into the parylene pocket; tweezers are used to align the bonding pads to the metal pads on the chip under the microscope.

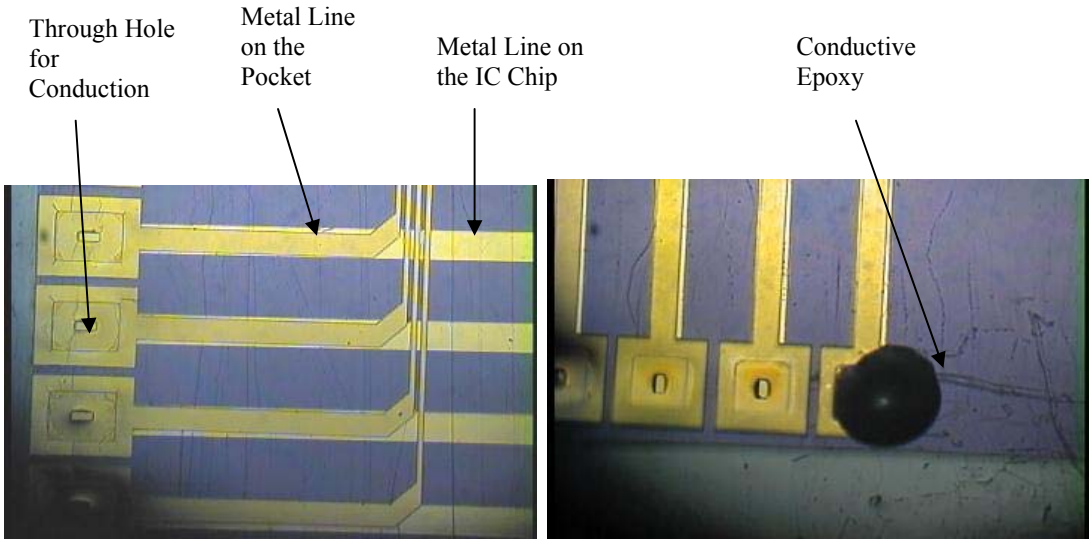


Figure 2.7. (left) Alignment of the pads on the parylene pocket and the metal lines on the inserted chip. The alignment offset was on the order of 10 to 20 μm; (right) a drop of biocompatible conductive epoxy is applied over the metal pads to provide electrical conduction. The size of the drop is on the order of 150 to 200 μm.

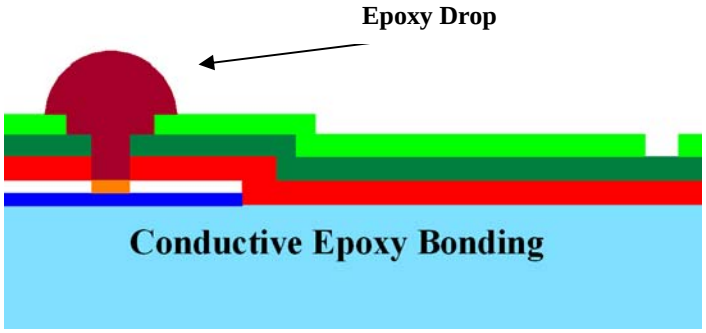


Figure 2.8. Bonding scheme for the parylene pocket. A drop of conductive epoxy is applied on the bonding hole that exposes the metal pads on the IC chip underneath.

2.3.3 Second Generation—Parylene Substrate

The parylene pocket configuration is fabricated with RIE technology. Figure 2.9 shows the fabrication process for parylene pocket with substrate. First, 5 μm of bottom layer parylene C is deposited by room temperature CVD on a prime, untreated silicon wafer. Sacrificial photoresist of 1 μm is then coated to create the parylene pocket structure. Another layer of parylene C (5 μm) is deposited, followed by Cr/Au (0.05/0.2 μm) lift-off process by electron beam evaporation to provide electrical

connection. The top layer of parylene C (5 μm) is deposited to complete the structure. Electrode sites and the device definition are then opened by a two-step RIE with O_2 plasma process. The devices are released in photoresist stripper.

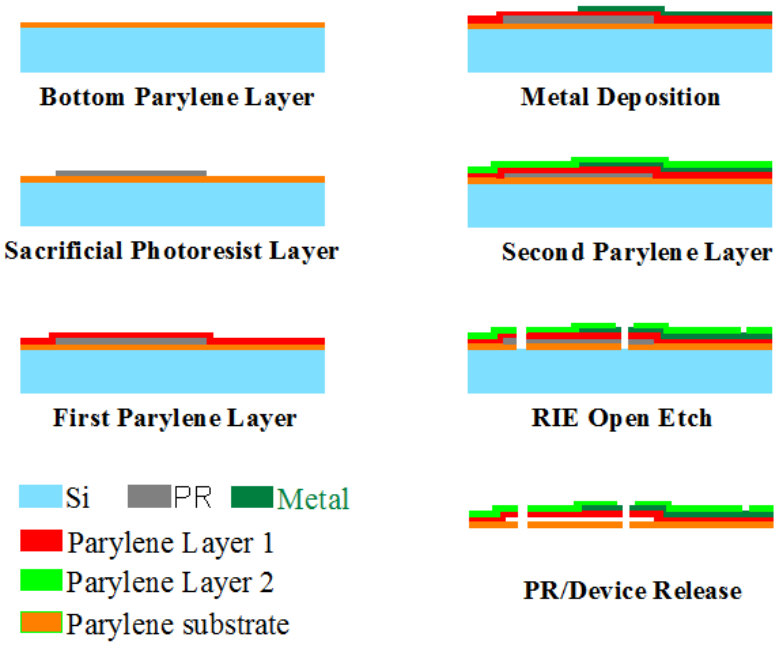


Figure 2.9. Fabrication process for the pocket structure with parylene C substrate. The device can be made on any type of wafer.

It should be noted that the chip insertion and bonding process for parylene pocket on parylene substrate requires more steps than the bonding process for parylene pocket on silicon substrate due to the mechanical nature of the two structures. The parylene substrate lacks the mechanical backbone that the silicon substrate provides to support and fix the IC chip in place after insertion and leaves the IC chip too much freedom to move around in the pocket. An extra fixation process is thus developed to fix the parylene pocket on parylene substrate in place to facilitate the insertion and the alignment of the chip.

In the chip-fixation process, the released parylene pocket structure is placed on the tape that is used for wafer dicing operations. The structure is first carefully placed on

the tape to prevent any trapped air bubbles. Tweezers are then used to separate the top layer of the pocket from the bottom layer of the pocket. Aluminum foil is then inserted in the pocket to keep the two layers separated. The structure is then soaked in acetone with the tape to be released because the tape loses adhesion in acetone. Finally, the chip is inserted into the pocket and the aluminum foil is pulled out to complete the package. Detailed examples will be discussed in chapter 3.

2.3.4 Variety of Pockets

On some occasions such as wireless telemetry and nerve stimulation, circuit components including capacitors and inductors are needed for the functionality of the overall system [109]. One of the biggest advantages of the parylene pocket over traditional packaging techniques is its ability to accommodate not only integrated circuit chips, but also different types of components such as printed circuit boards and surface mount components.

2.3.4.1 For IC Chips

The embedded CMOS amplifier chip [102] is a scalable 16-channel preamplifier and buffer chip with an in-band gain of 35.5 dB. This chip was tested using a function generator on a pocket-only structure. Pockets with both silicon (figure 2.10) and parylene (figure 2.11) substrate are demonstrated here.

Both sine waves and square waves with frequency of 0.5, 1, 2 and 5 kHz and amplitude of 5 mV were passed into the chip by connecting the function generator to the bonding pads on the device. The amplified output (figure 2.12) from the oscilloscope concludes a successful functionality testing of our packaging technology for integrated circuit chips.

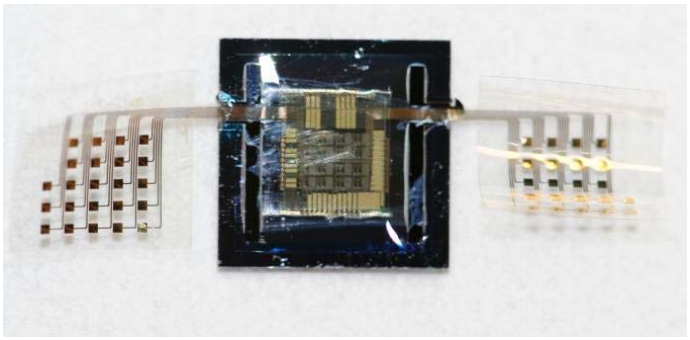


Figure 2.10. Parylene pocket-only structure. This device is used to test the amplifier chip after bonding. Signal is driven in from the bonding pads on the right-hand side of the figure and is measured from the bonding pads on the left-hand side of the figure.

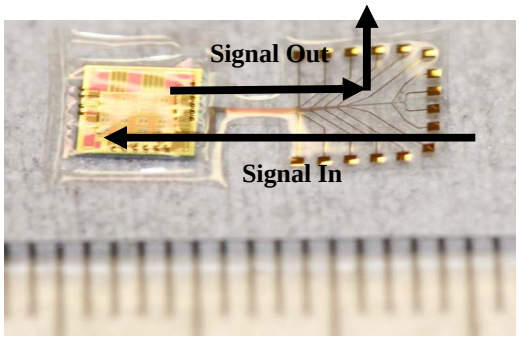


Figure 2.11. Parylene pocket-only structure. It is used to test the amplifier chip after bonding. Signal is driven in from the bonding pads of the parylene structure on the right-hand side of the figure.

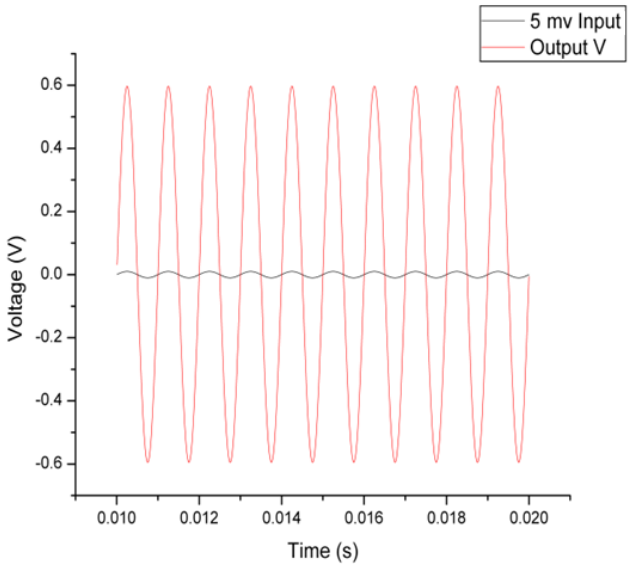


Figure 2.12. Input of 5 mV (10 mV peak to peak) sine wave of 1 kHz is passed into the amplifier (gain = 60) and its oscilloscope output is recorded. Signals of 0.5, 2, and 5 kHz were also tested with the chip.

2.3.4.2 For Discrete Components

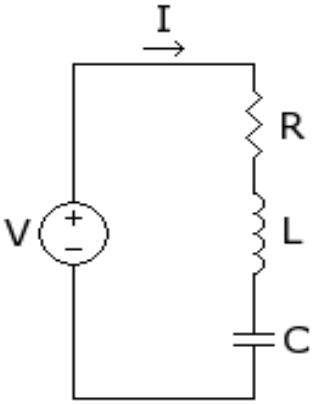


Figure 2.13. Circuit diagram of the RLC circuit packaged with the parylene pocket.

An RLC series circuit (figure 2.13) consisting of three 0.4 mm × 0.2 mm × 0.5 mm surface mount components (0402 package, Digikey Corporation, Thief River Falls, MN, USA) is packaged in parylene pockets with parylene substrate. The insertion and bonding process of the discrete components is exactly the same as that of the IC chips where conductive epoxy is used to make the connection from the bonding pads of the pocket and the contact pads of the surface mount components. The platform in figure 2.14 shows a 1 cm × 1 cm × 20 μm parylene substrate with three open pockets for the three surface mount components. The wafer bonding tape was used to assist the packaging and bonding of the structure.

The result for the impedance measurement of the circuit is shown in figure 2.15 with the following parameters: resistance = 1 kΩ, capacitance = 1 μF, inductance = 2.2 μH. The resonance frequency is calculated by the following equation,

$$\omega = \frac{1}{\sqrt{LC}}$$

Measurement result with HP 4192A LF impedance analyzer shows a resonance frequency at around 106 kHz while the theoretical resonance frequency is at 107 kHz.

This verifies the successful bonding of the circuit with the pocket and the overall functionality of the parylene pocket technology for discrete components.

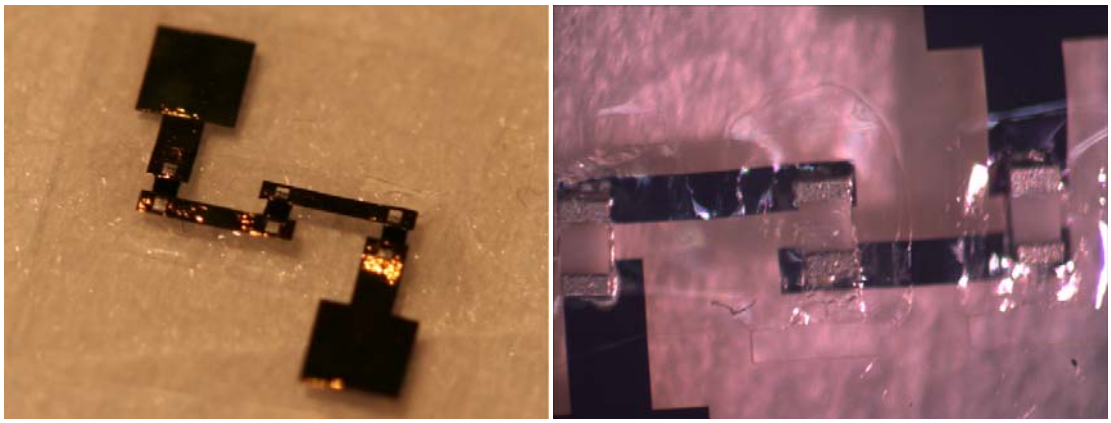


Figure 2.14. (left) Parylene pocket on parylene substrate for discrete components. An RLC circuit with 0402 sized surface mount components is shown in the figure; (right) backside of the parylene pocket on parylene substrate. The surface mount components are clearly shown inserted in the pocket.

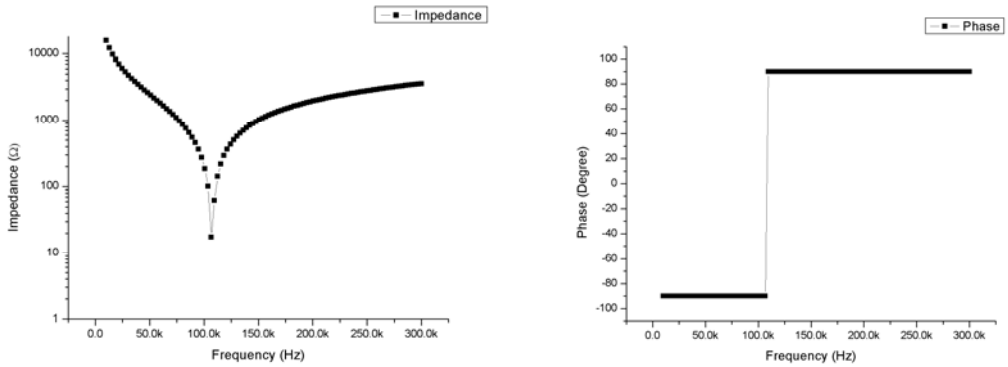


Figure 2.15. (left) Measured frequency response of the RLC circuit, the resonance frequency can be clearly determined from the plot; (right) measured phase response of the RLC circuit.

2.3.4.3 For Double Side and Multiple Layer Components

In addition to the two-dimensional pad layout shown in previous sections, the parylene pocket technology can be extended to house multilayer components such as double-sided printed circuit boards and/or be applicable for chip stacking. This section presents the multilayer technology developed for this purpose.

A dual-layer pocket is fabricated to accommodate a double-sided printed circuit board. It is fabricated with RIE technology and the process steps are shown in figure 2.16. First, 5 μm of bottom layer parylene C is deposited by room temperature CVD on a prime, untreated silicon wafer, followed by Cr/Au (0.05/0.2 μm) lift-off process by electron beam evaporation to provide electrical connection for the first layer. The 2nd layer of parylene is then deposited to complete the bottom sandwich layer. Bottom sandwich layer electrode sites are opened by RIE with O_2 plasma. Sacrificial photoresist of 1 μm is then coated to create the parylene pocket structure. Another layer (3rd layer) of parylene C (5 μm) is deposited, followed by another Cr/Au (0.05/0.2 μm) lift-off process with electron beam evaporation. The top (4th) layer of parylene C (5 μm) is then deposited to complete the top sandwich structure. Electrode sites and the device definition are then opened by a two-step RIE with O_2 plasma process. The devices are released in photoresist stripper and warm water bath.

The fabricated device has dimension 2.6 cm × 2.6 cm with pocket size of 8.5 mm × 9.6 mm (figure 2.17a). The device thickness is around 25 μm with trace width of 200 μm and pad size 900 μm × 900 μm. These dimensions can be modified depending on the device. The insertion process of the PCB into the dual layer pocket is similar to the process described in previous sections. The integrated structure is shown in figure 2.17b.

The contact pads on the bottom layer sandwich would connect to one side of the PCB and the contact pads on the top sandwich layer would connect to the opposite side. This configuration is clearly shown in figure 2.18, where one layer of metal runs underneath the PCB and another layer of metal runs above. The two sides of the parylene pocket can also be seen.

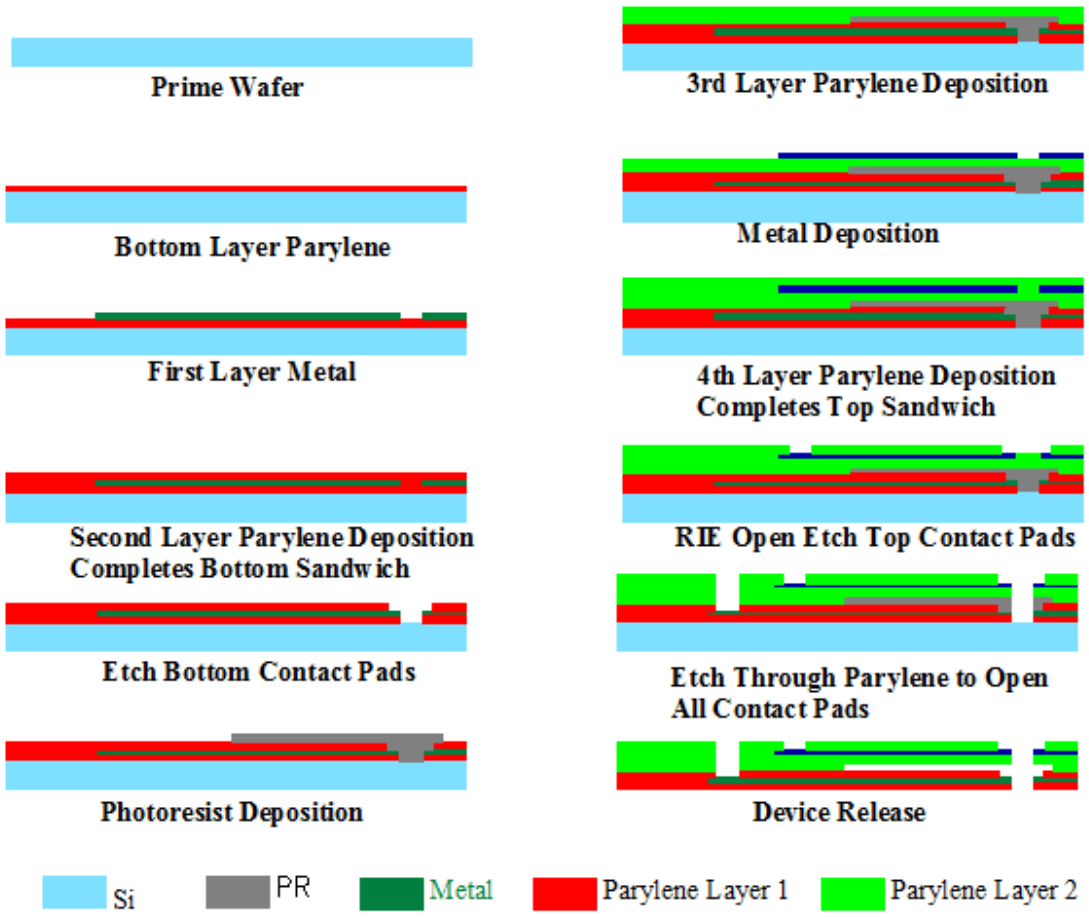


Figure 2.16. Fabrication process for dual layer pocket.

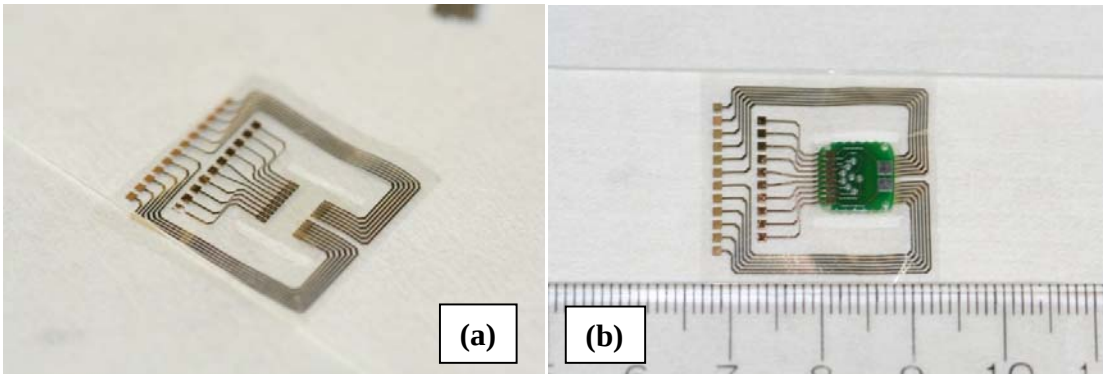


Figure 2.17. (a) Fabricated dual layer parylene pocket device for PCB integration; (b) PCB inserted into the pocket. The insertion process is similar to the process described in previous sections.

It should be noted that the metal on the bottom layer sandwich opens away from the surface (figure 2.19) and makes it more difficult to make connection. The conductive

epoxy may have to be slightly more diluted for it to seep into the gap between the metal that is pointing upwards and the bonding pad on the chip in order for the connection to take place. Further improvement of this process is underway, including new metal deposition methods to make both metal openings toward the surface (figure 2.20), which requires the metal to be deposited before the parylene substrate is coated.

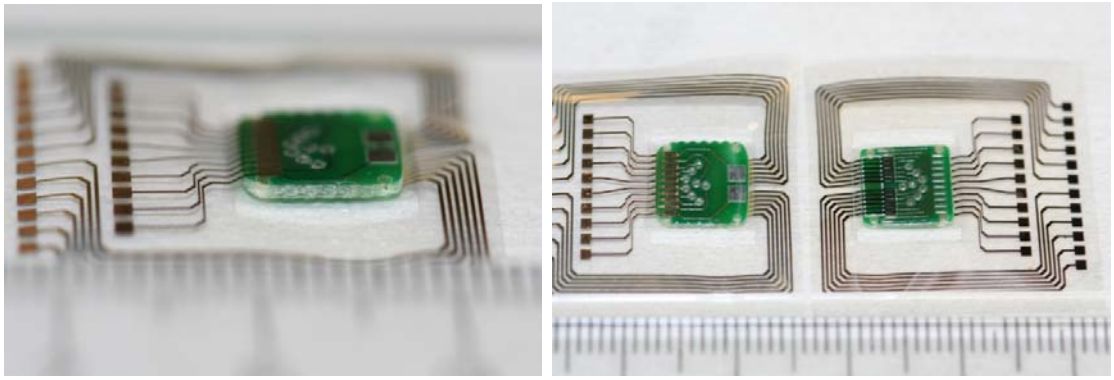


Figure 2.18. (left) Close-up view of the PCB inserted into the pocket. One can clearly see the traces on the right-hand side run underneath the PCB whereas the traces on the left hand side run above the PCB; (right) a side-to-side comparison of the front and back of the device.

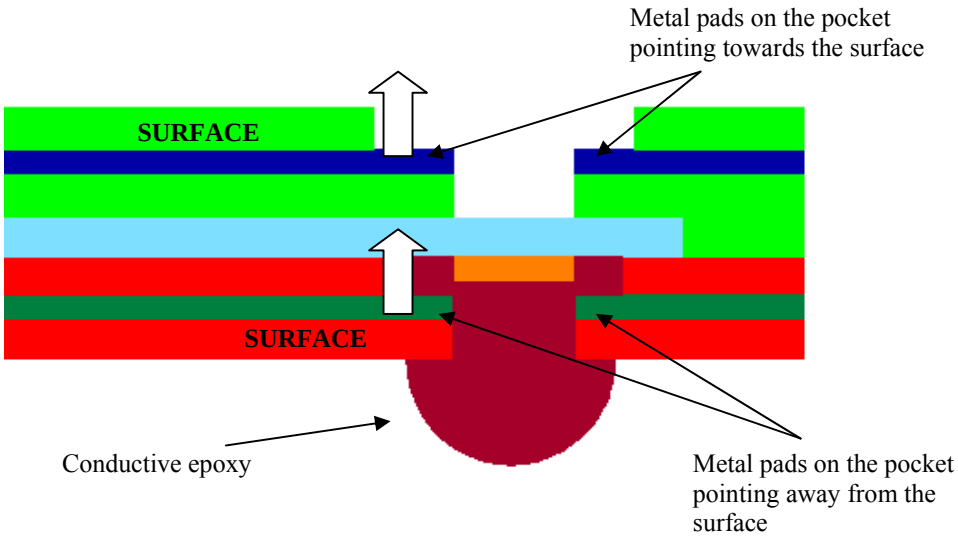


Figure 2.19. Current metal bonding pad orientation; the metal pads on the bottom layer point away from the bottom surface.

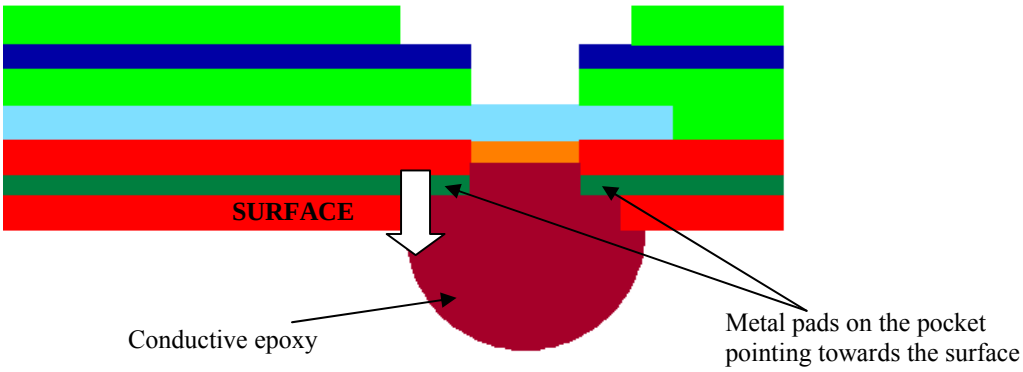


Figure 2.20. Ideal metal bonding pad orientation; the metal pads on the bottom layer point toward the bottom surface.

A quick conduction test of this structure verifies the functionality and the packaging ability of this technology. This dual layer structure not only can accommodate a double-sided PCB, it can also be extended to triple, quadruple or even more layers to incorporate ultrahigh density traces or multiple chip stacking applications. It would be possible to separate the control signal from the stimulation signal in a retinal prosthetic application, for example, to gain better control of the design of the system and to modularize the connections.

2.4 Integration with Silicon Probes

This section demonstrates a parylene pocket integrated silicon probe that is monolithically fabricated using MEMS technology. A schematic of the proposed implantation scheme is shown in figure 2.21.

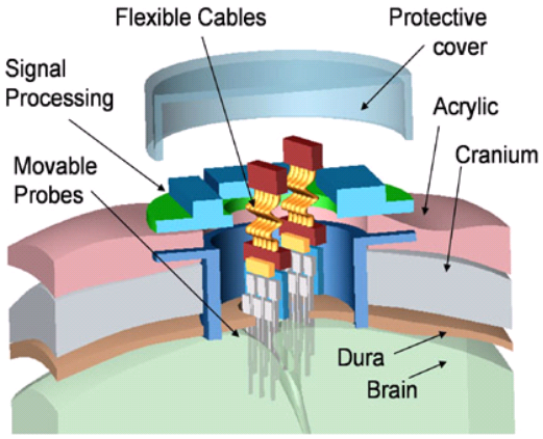


Figure 2.21. Schematic of cortical implantation using neural probes with parylene cables.

An important goal in neural prosthesis is to be able to decode the movement intention in the parietal cortex from neurons by implanting neuroprobes [110–111]. While three-dimensional integrated silicon probes have been successfully manufactured [112], the degradation of the signal-to-noise ratio (SNR) is still a major challenge because electronics are too far away from the recording site. Additionally, recent developments in bioimplantable devices such as retinal, cochlear and cortical prosthesis implants also increase the demand for totally implanted technologies. Therefore, the biocompatible parylene pocket technology becomes the perfect candidate for this application, as it is a suitable packaging/integration solution to embed amplifiers near the recording sites. A process to integrate parylene pocket onto a parylene-cabled silicon probe is presented in this section.

The parylene pocket technology offers several advantages such as (1) it causes no infections and inflammatory responses, (2) is be able to withstand the harsh physiological environment of human body, and (3) is inexpensive and easy to make. This technology meets numerous demands and overcoming the challenges that current state-of-the-art technologies cannot fulfill.

2.4.1 Design

A flexible parylene lift-off technology [113] allows us to fabricate two-dimensional 32-channel flexible cabled electrode array devices (figure 2.22). These devices can be expanded to three-dimensional 32N-channel structures by probe stacking of N number of two-dimensional probes (figure 2.22). Platinum electrodes on each of the eight silicon shanks can be spaced at configurable intervals, and two reference electrodes are located on two of the longer shanks. These electrodes are individually wired and are fabricated so that they are electrically isolated from one another to avoid interferences of signals. Unlike the traditional probes (figure 2.23) for signal recording where the entire microelectrode pin can only accommodate one electrode, the silicon probe configuration presented in this section can achieve a higher density recording landscape and is more area and space efficient.

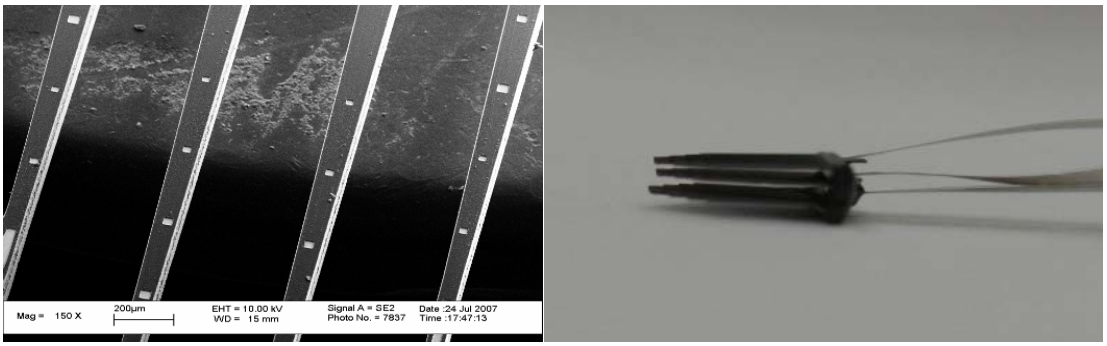


Figure 2.22. (left) SEM picture of the electrodes on the silicon shanks; (right) probe stacking capability of the silicon probe structure. Figure shows three 32-channel probes stacked together to form a 96-channel three-dimensional structure. The spacing between the probes can be modified.

The shank lengths range from 3 to 12 mm and are 150 µm thick and 60 µm wide toward the tip of the shank. The tip of the shank forms a 10° angle to facilitate the insertion into the brain.

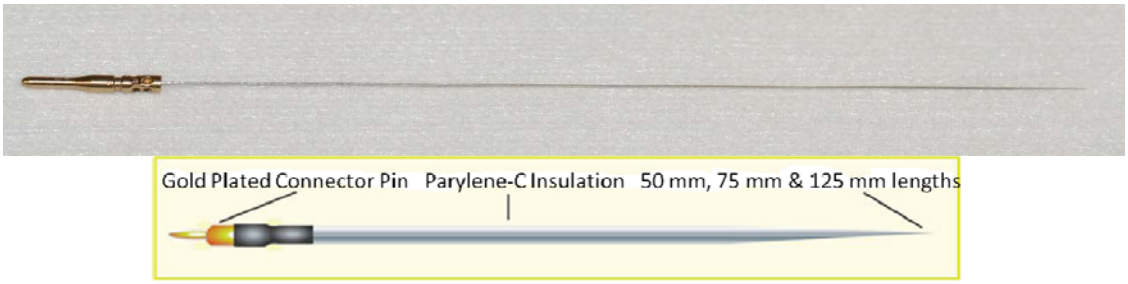


Figure 2.23. Single microelectrode pin with parylene coating. The only electrode is opened at the tip of the probe.

Figure 2.24, figure 2.25 and figure 2.26 show the unpackaged cabled silicon probes without the pocket structure and their bonding interface. The circular platinum rings arranged in a 60° Y shape pattern on the end of device are used to electrically bond to commercial available connectors with conductive epoxy on a circular PC board [114]. The parylene cables (7 cm long) are 15 μm thick and have 34 traces lines that are 10 μm wide and spaced 10 μm apart to connect the distal electrodes directly to external connectors [115] (figure 2.27). This original design does not have IC chip integration capability.

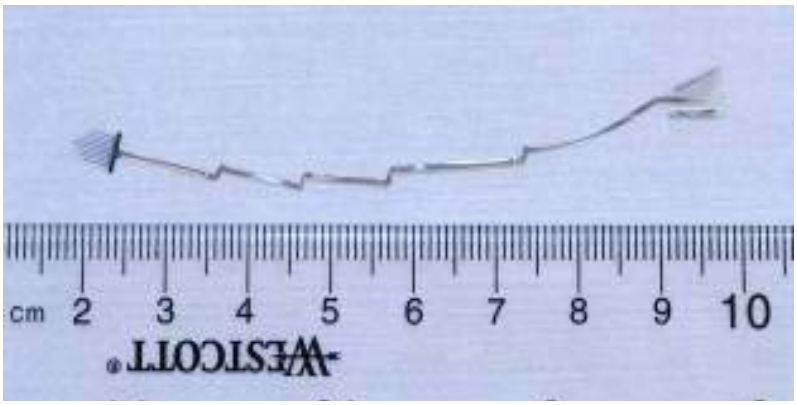


Figure 2.24. Released silicon probe with parylene flexible cable.

Figure 2.25. Proximal bonding of commercial connector with parylene cable connector pads; (left) before bonding; (right) after bonding with conduction epoxy.

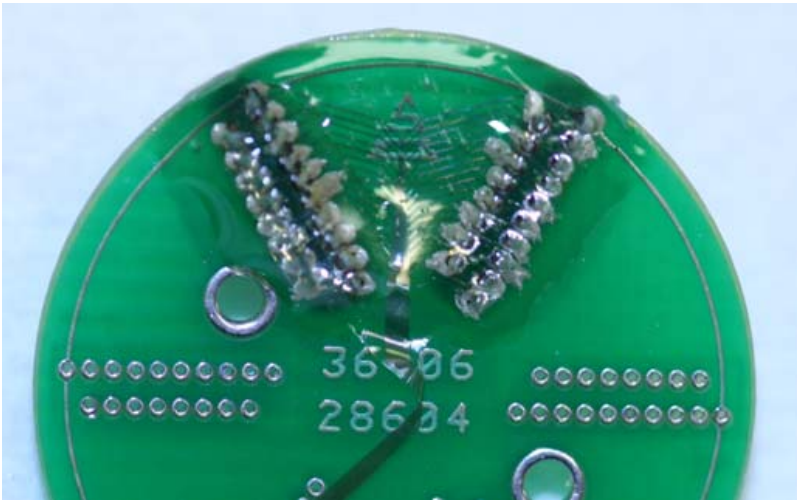


Figure 2.26. Bonding interface of the connector pads on the silicon probe device and the commercial connector through a custom PC board.

Figure 2.27. Schematic of the packaged silicon probes. The design shows a 96-channel device consisting of three 32-channel devices. The legs of the titanium pedestal are secured to the skull with bone screws.

2.4.2 Fabrication

In order to integrate amplifier chips close to the signal recording sites, parylene pocket structures with the parylene-cabled silicon probe are fabricated on double side polished wafers with DRIE technology. Figure 2.28 shows the fabrication process.

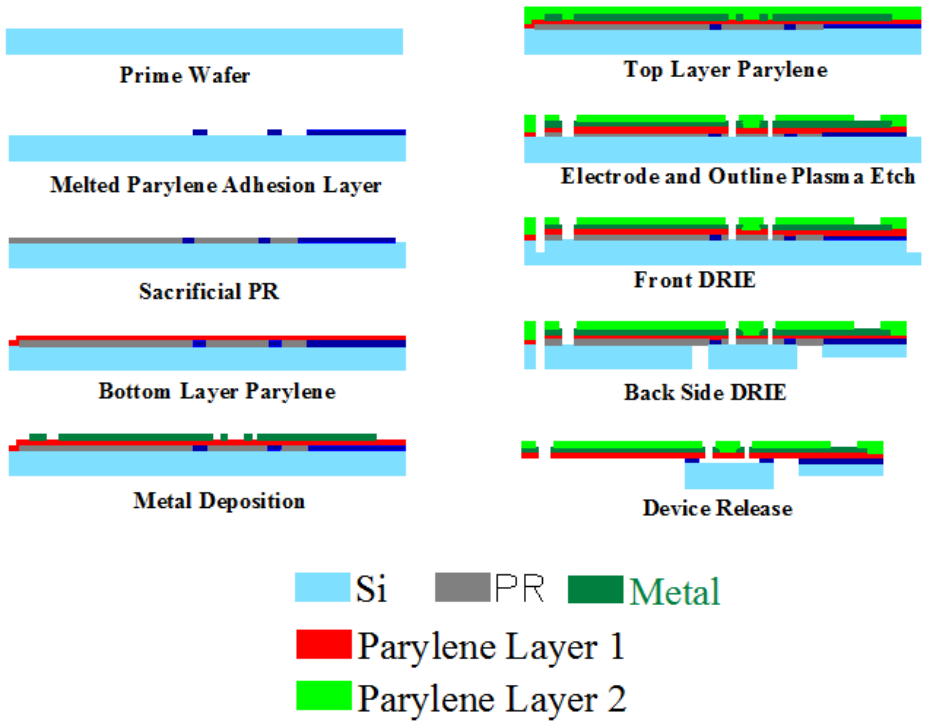


Figure 2.28. Fabrication process of the parylene-cabled silicon probe with parylene pocket.

First, 0.5 μm of parylene C is deposited on one side of the wafer by room temperature CVD and is melted in an oven with N_2 backflow at 350ºC. This film is then patterned by O_2 plasma to leave areas for adhesion enhancement between the parylene/silicon interfaces for the silicon probe and the pocket structure. A sacrificial photoresist layer of 1 μm is then spin-coated on the wafer for pocket and cable releasing. A bottom layer of parylene C (6 μm) is then deposited, followed by Cr/Au (0.05/0.2 μm) lift-off process with electron beam evaporation to provide electrical connection. The top layer of parylene C (6 μm) is deposited to complete the parylene-metal-parylene

sandwich structure. Electrode sites and the device definition are then opened by a two-step RIE with O_2 plasma process. The outline of the parylene pocket structure is subsequently etched by DRIE from both sides of the wafer after back-side wafer lithography steps. In the final step, the devices are released in photoresist stripper and dried on a hotplate at 100°C. A chip is then inserted into the parylene pocket, aligned, bonded with conductive epoxy and totally coated with parylene C again for complete encapsulation and to ensure biocompatibility in a similar fashion as described earlier in the chapter.

Figure 2.29 shows the packaged parylene-cabled silicon probe integrated with the parylene pocket with silicon substrate. After the entire structure is coated with a protective layer of parylene, the entire pockets structure is coated with 1 mm thick of biocompatible silicone and oven cured for 2 days.

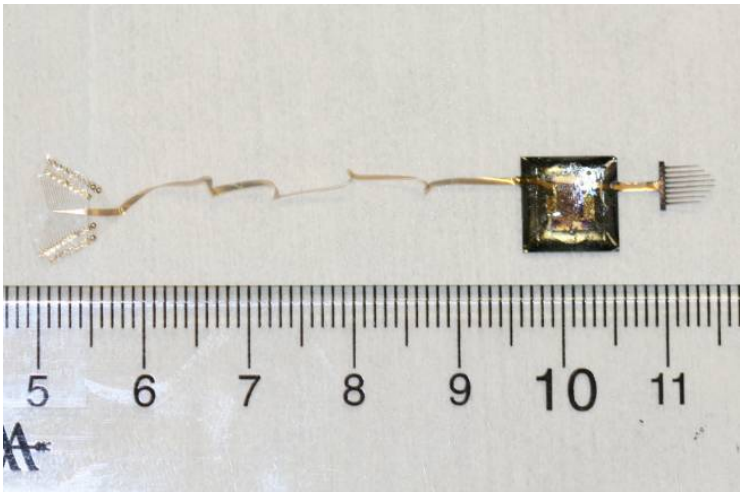


Figure 2.29. Silicon probe integrated with parylene pocket. A conduction chip has been inserted to demonstrate the functionality of the integrated pocket structure. This device has been totally coated with parylene and sealed with epoxy.

2.4.3 Testing and Verification

Device testing was performed in three phases: *in vitro* measurements in saline solution, *in vivo* probe penetration testing and accelerated life testing. In this testing phase, a conduction chip with metal traces is bonded with the structure.

In the first phase, we used the setup shown in figure 2.30 to conduct *in vitro* impedance tests with channel electrodes having mean dimensions 22 μm × 22 μm. The measured distribution of areas of these electrodes was determined to lie within 9.1 μm^2 of the nominal value under SEM measurements. Impedance measurements of channel electrodes resulted in values of 670 kΩ ± 33 kΩ at 1 kHz whereas the reference electrodes with areas approximately 25,000 μm^2 resulted in impedances in the range of 20 kΩ. To test the electrode's ability to pick up signal different signal types, sine waves and prerecorded action potentials were applied across a saline solution and were successfully recorded with the fabricated electrodes (figure 2.31).

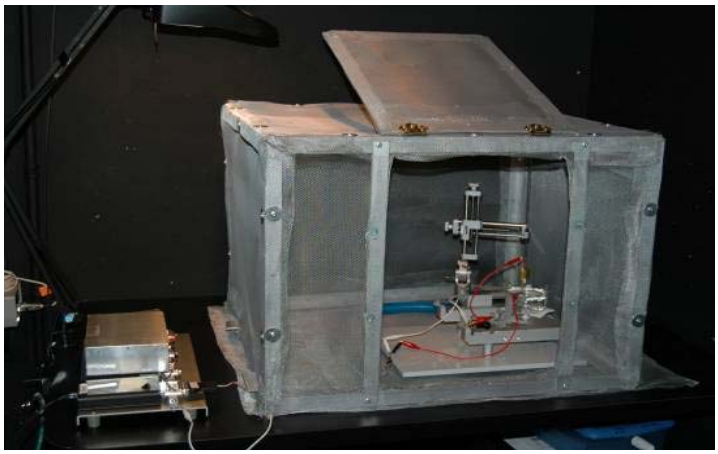


Figure 2.30. *In vitro* testing setup. The metal box on the left-hand side is a preamplifier. The x-y stage in the Faraday cage maneuvers the probe into the saline solution.

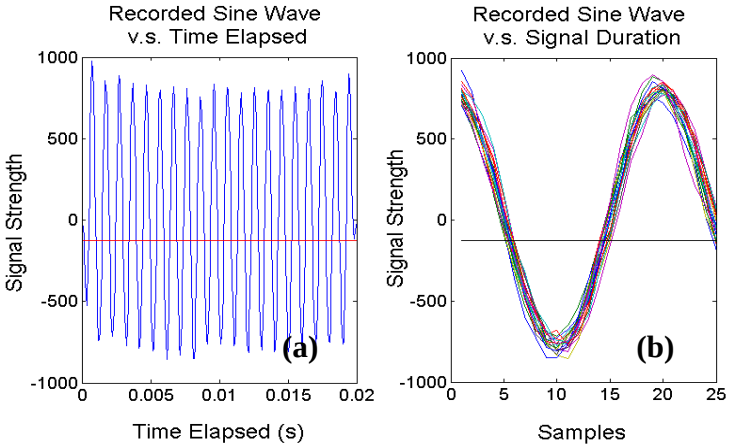


Figure 2.31. (a) Sine wave applied across a saline solution recorded with the silicon probe. (b) Threshold aligned waveforms. The horizontal axis is the number of samples taken at the rate of 20,000 samples per second for a duration of 1.2 ms. The vertical axis represents the signal strength corresponding to a sinusoid with amplitude (above baseline) of 400 μV.

Second, the devices were inserted through the pia and into the cortex of live rats to test penetration ability. Results show a full insertion (figure 2.32) of the probe was successful without any bending, buckling or breakage by observing the shanks under a surgical microscope during insertion.

Figure 2.32. Successful chronic implantation in rat cortex by penetrating pia using a complete device with metal electrodes and flexible parylene cables. The picture shows the silicon probe being inserted halfway into the brain.

Finally, the devices underwent accelerated life testing in saline to determine the mean time to failure. Failure modes include the failure of the silicon to parylene adhesion as well as the delamination between the parylene layers. Soaking test results show that the parylene-silicon adhesion is able to withstand more than five weeks in 90°C saline before delamination occurs.

In addition to the totally integrated silicon probe array, a second design was developed. It consists of a probe-only device with 36 electrodes and 2 reference electrodes separated from the parylene pocket-only structure (figure 2.33a). The probe-only device has identical geometry to that of the totally integrated device mentioned above. The user would be able to test the pocket structure with the integrated IC chip before connecting it to the electrodes on the silicon probe, resulting in a big advantage in terms of fabrication yield and testing convenience. It also demonstrates the ability of the parylene pocket technology to be bonded and integrated with any type of recoding and stimulating devices. The assembled device is shown in figure 2.33b. We use conductive epoxy as the medium for bonding.

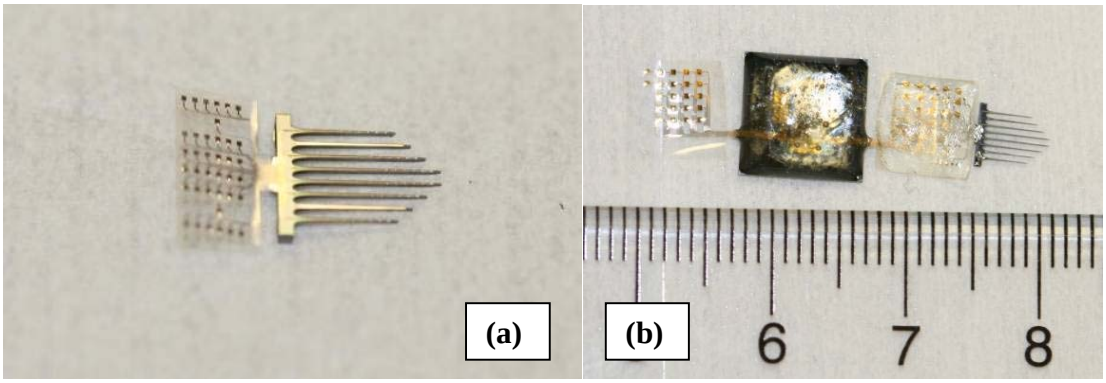


Figure 2.33. (a) Silicon probe-only structure for testing purpose. The parylene sheet extension provides metal pads for electrical connection to the parylene pocket-only structure; (b) bonded and packaged structure. In this device, the conduction chip was used. The impedance of the electrode was measured to be 600 kΩ.

2.5 Summary

An ideal well-packaged device for implantation would (1) cause no infections and inflammatory responses and (2) be reliable and able to withstand the harsh physiological environment of human body, (3) flexible and biocompatible and (4) be inexpensive and easy to make. Current state-of-the-art technologies, which includes wire bonding, bump bonding, flip chip and tape automated bonding have yet to balance the trade-offs between these criteria. The parylene pocket technology is thus developed to overcome this challenge.

This chapter summarizes the fabrication process and technique of the parylene pocket technology with both silicon and parylene substrate. Not only have this MEMS-technique-enabled packaging technology facilitated the integration of both IC chip and discrete components; it has also achieved high-level functionality for a neural prosthetic platform to overcome numerous challenges.

Finally, it is shown that these systems have been successfully bonded and packaged with the technology. Experiment and measurements are also done to validate the functionality of the structure and to demonstrate the versatility of the technology.

3 IMPLANTABLE CHIP INTEGRATION TECHNOLOGY

3.1 Introduction

Recent developments in prosthetic applications and implantation technologies have proven an increase in demand for reliable biocompatible packaging techniques with integrated circuits. Furthermore, high lead-count IC interconnect technologies have also become vital to realize numerous prosthetic application requiring high resolution stimulation electrodes and recording channels. Traditional integration methods to achieve this goal include but are not limited to

1. CMOS/MEMS process (shown in figure 3.1) to eliminate postprocess steps for bonding [116–120]
2. Wire bonding technique to bond pads to pads individually [121]
3. Flip chip/Ball Grid Array technique for high density connections [122–123]

These bonding methods, unfortunately, either have low reliability, nonbiocompatibility, high thermal budget, and high fabrication costs or lack the ability to integrate a high number of leads. Thus, to overcome these challenges, Rodger et al. developed a chip-level integrated interconnect (CL-I^2) packaging technology [124], in which the IC chip is integrated on wafer level during the process and is connected to the system with a combination of traditional MEMS lithography and metal etching steps.

However, this method is very sensitive to dry etching flatness and the vertical distance between the wafer and the chip since metal lines will be broken as they cross the step.

Parylene pocket technology, a cheap, biocompatible, flexible and reliable process has been developed to alleviate this problem. It provides an excellent alternative for applications requiring IC integration from fast prototyping to full system integration. Its two applications and integration processes are demonstrated in this chapter. A high density bonding model will be presented in later chapters.

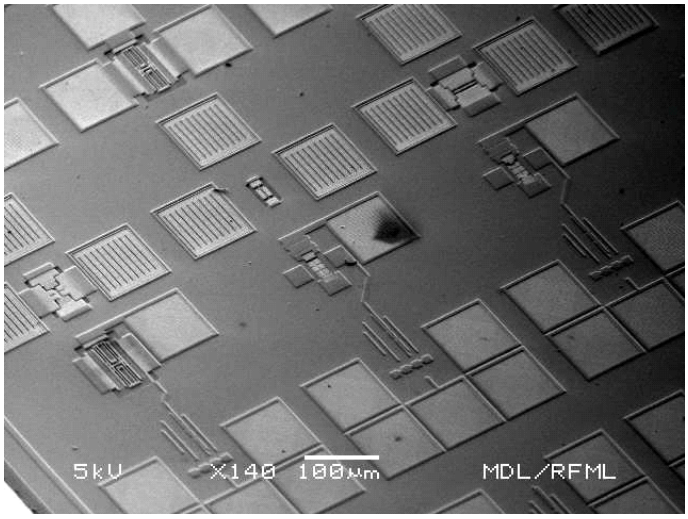


Figure 3.1. CMOS MEMS integrated process [119].

3.2 RFID Chip Integration

Radio frequency identification (RFID) is an ubiquitous technology that has affected our daily lives; not only can RFID be applied to product tagging and traffic controls, it can also be applied to animal and human tracking and tagging [125]. Although there has not been any direct evidence of RFID causing these issues and problems, there have been reports of foreign body in human body inducing sarcoma after decades of implantation [126]. As a result, the biocompatibility of the packaging and integration of these RFID IC

chips during animal and human implantations becomes increasingly important to minimize the risk of these occurrences.

In this section, a passive RFID chip integration with parylene pocket technology is demonstrated, functional and reliability tested. The chip we use is EM4100 read-only RFID chip (EM Microelectronic, Switzerland), a CMOS IC for use in read-only transponders [127]. The chip (shown in figure 3.2) is powered and clocked by an external coil and sends out a 64 bit signal contained in the memory operating at around 125 kHz. Only an external coil is needed to obtain the chip function. The chip will be integrated in a parylene pocket specifically designed for it and will be protected with silicone and parylene for a complete biocompatible sealing.

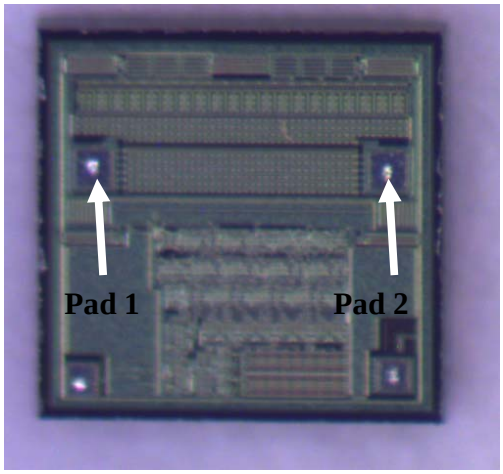


Figure 3.2. EM4100 RFID chip used to demonstrate the pocket integration technology.

3.2.1 Design and Fabrication

A parylene pocket with parylene substrate is fabricated for the integration of this device. The chip is around 180 μm thick and is 1 mm × 1 mm in dimension. The masks that were used to fabricate the parylene pocket structure are shown in figure 3.3.

The parylene pocket configuration is fabricated with RIE technology. First, 5 μm of parylene C is deposited on the wafer to act as the substrate of the pocket. Sacrificial

photoresist of 1 μm is then coated on the wafer and then exposed under a stepper lithography system to create a sacrificial area to accommodate the chip. The wafer is then cleaned with buffer hydrofluoric acid before being coated with another 5 μm layer of parylene C to encapsulate the sacrificial layer and to serve as the base layer for metal deposition. The wafer then undergoes a lift-off lithography step to create patterns for a Cr/Au (0.05/0.2 μm) metal layer that is deposited by electron beam evaporation to provide electrical connection. The metal parts near the top of the mask (seen in figure 3.3) consist of metal-pad areas with through-holes in the middle to enable the connection from the pad to the chip, which will be inserted underneath this layer during the packaging process. The metal trace toward the bottom of the mask also consists of two larger metal pads for connection to a coil for external functional testing. After the metal lift-off process by soaking the wafer in a photoresist stripper, the top layer of parylene C (5 μm) is then deposited to complete the sandwich structure. A two step lithography and RIE with O_2 plasma process is then used to open the parylene to expose the metal; the plasma etches the top parylene layer until the metal pads are exposed in the first step; then the through holes and the device structure are etched in the second step. The wafer is then again soaked in a photoresist stripper and cleaned. The devices are finally released from the wafer in a warm water bath.

In this design iteration, the dimension of the parylene pocket area (the area of the sacrificial photoresist) is designed to be 1.8 mm × 2.1 mm to leave room for chip maneuvering. The optimal area for the pocket could have been reduced to 1.5 mm × 1.5 mm since the chip is around 1 mm × 1 mm and the thickness of the chip is less than 0.2 mm. The area for the bonding pads designed to be 300 μm × 300 μm. This area could

have been reduced to 100 μm × 100 μm or less, but since there are only two pads on the chip that are placed very far apart, larger bonding pads are designed for ease of connection. The through holes usually have similar dimensions as the bonding pads on the chip.

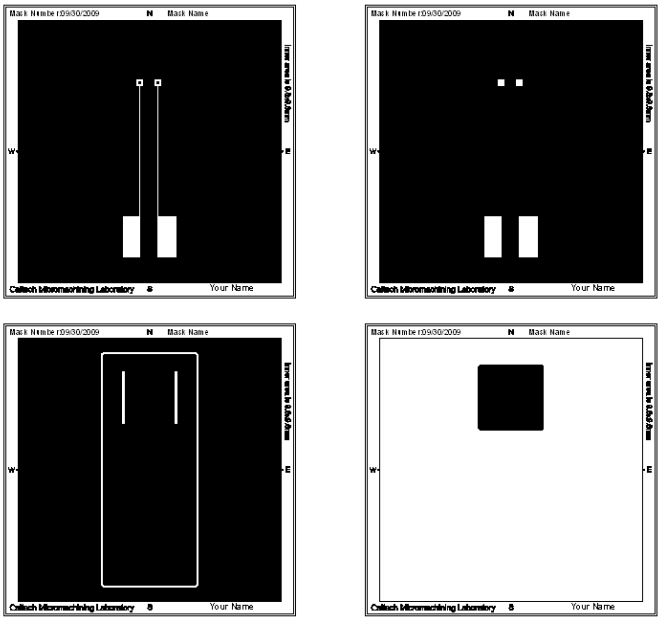


Figure 3.3. Photolithography masks used for the RFID parylene pocket structure; (top left) lift-off lithography mask for the metal; (top right) metal exposure mask; (bottom left) through hole and device definition mask; (bottom right) sacrificial layer mask. Positive photoresist is used is this process.

3.2.2 Integration Demonstration

After the devices are released from the wafer, the photoresist is dissolved away, and there is no barrier to prevent the parylene layers in the pocket area to stick to each other, thus making the layers very hard to separate while the device is free standing. An additional step needs to be taken to detach these two layers from each other so chips can be inserted between them. The devices are first placed on a wafer dicing tape (figure 3.4a). Since now the parylene substrate is fixed on the tape, the top sandwich layer becomes easier to detach from the substrate layer (figure 3.4b) with a spatula. A piece of aluminum foil is first inserted in the pocket to provide an anchor for the thicker chip to be

inserted (figure 3.4c). The pocket structure is then placed in acetone to be released from the wafer dicing tape and placed on a sticky surface for temporary fixture (figure 3.4d, figure 3.4e and figure 3.4f).

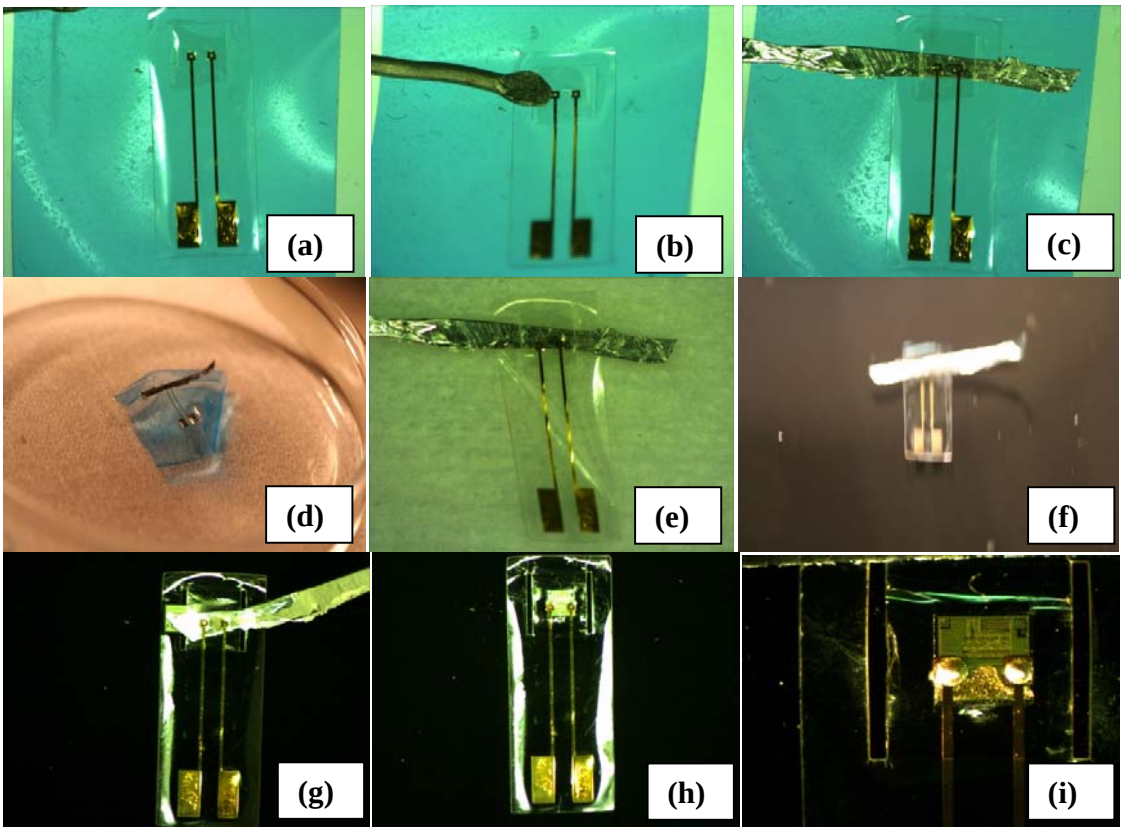


Figure 3.4. Step-by-step integration process of the RFID chip with the parylene pocket.

After the chip is inserted into the pocket (figure 3.4g), the metal pads on the chip are then aligned with the metal bonding pads on the pocket structure under the microscope (figure 3.4h). Alignment accuracy is on the order of 10–20 μm. Conductive epoxy adhesive is then mixed and applied on top of the pads individually to make the electrical connection (figure 3.4i). The bonded structure is then cured in the oven at 80ºC for 90 minutes, followed by a 30 μm parylene C deposition to encapsulate the device. Finally, a two-part biocompatible silicon is mixed and painted onto the chip area for further protection. The total thickness of the final device, including the thickness of the

silicone applied and the thickness of the chip, is around 2 mm. The bonding pads toward the bottom of the figure were not covered with biocompatible epoxy for testing purposes (figure 3.5).

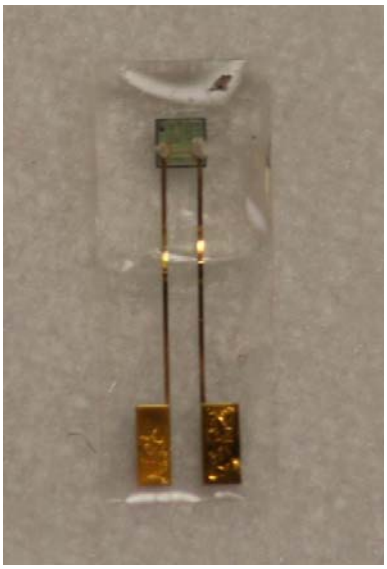


Figure 3.5. Parylene pocket packaged RFID chip. The structure is coated with 30 μm parylene C and around 1.5–2.0 mm of biocompatible silicone after bonding.

It should be noted that during the entire integration and fabrication process, the profile of the surface of the chip and how flat the chip rests in the pocket after bonding were not measured. In fact, the success of the integration does not depend on these two factors at all. This not only shows the insensitivity of the profile of the chip, but also illustrates how simple and easy this integration process can be utilized by any research endeavors who wish to embed a commercially available integrated circuit with their implantable biosystems.

3.2.3 Functional System Testing

The RFID chip is successfully integrated with the parylene pocket structure and a full functional testing is conducted to validate this bonding technology and the robustness of the packaging. The structure is connected to a hand-wound coil for the wireless

transmission, the self-inductance of the receiver coil is around 5.25 mH and the DC resistance is around 10.7 Ω. This coil will also be used in the next section.

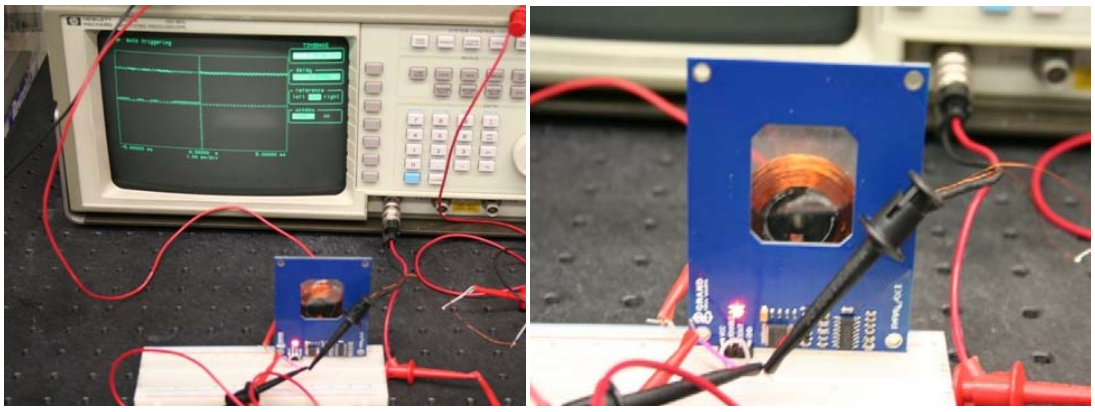


Figure 3.6. RFID test setup with the oscilloscope.

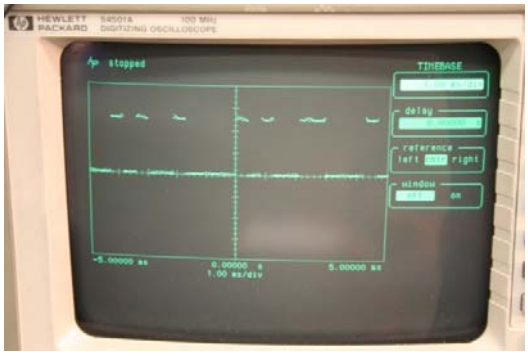


Figure 3.7. Signal readout from the oscilloscope.

The integrated RFID chip with the hand-wound coil is then tested with the Parallax RFID Reader Module #28140 (Parallax Corporation, Rocklin, CA), which is designed to work specifically with the EM4100-family chips of passive, read-only transponder tags. The setup is shown in figure 3.6. The RFID reader is powered up and the antenna is switched on by connecting 5 volt DC voltage and ground to the appropriate pins. The face of the hand-wound coil is held parallel to the front face of the antenna. The reading distance is about 3 inches. When a valid RFID transponder tag is placed within range of the activated reader, the unique ID will be transmitted as a 12-byte ASCII string via the TTL-

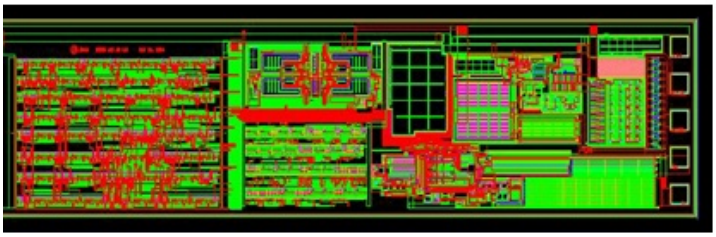
level SOUT (Serial Output) pin, which is monitored by an Agilent-HP 54503A digital oscilloscope, as shown in figure 3.7.

It should be noted that this parylene pocket structure is compatible with the fabrication process for the parylene-based RF coil [128]. A parylene pocket-coil structure can thus be monolithically made to further enhance the biocompatibility and the implantability of the system into human subject. It is known, however, that MEMS coils suffer from low inductance and noticeable parasitic effect due to the characteristics of planar MEMS fabrication techniques, and research is underway to optimize and alleviate these problems.

3.3 BION Chip Integration

A single channel muscle stimulator chip, BION, is developed by Dr. Gerald E. Loeb in University of Southern California to simulate the function of the muscle spindle to facilitate paralyzed patients. This device, after carefully positioned by X-ray, computed tomography (CT), ultrasound and magnetic resonance imaging (MRI) inside the body, is controlled by inductive coupling over a 480 kHz power and signal carrier generated by an external trainer unit. The chip will emit a precisely timed and regulated current pulse that spreads through the surrounding tissue to stimulate the muscle [129].

Because of its current emission and wireless transmission capabilities, BION acts as a great precursor for our retinal implant system. The schematic and the controls for the chip are shown in figure 3.8 and the overall system circuit is shown in figure 3.9.



Name	*Functionality*
V++	Rectifier output
A Coil	Coil terminal
B Coil	Coil terminal
Ta	Stimulation output
Ir	Common ground

Figure 3.8. BION chip layout and the pad connection.

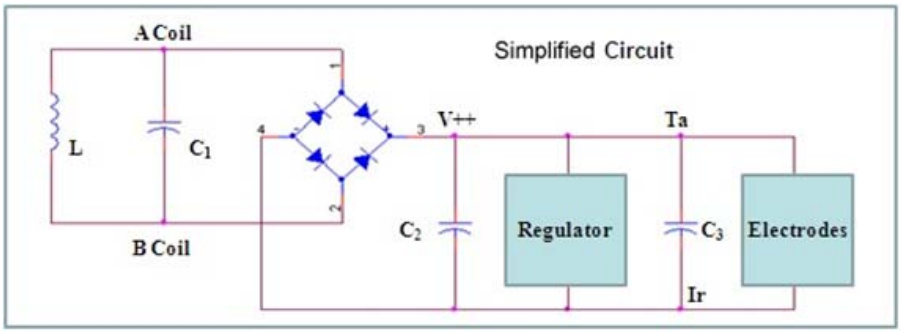


Figure 3.9. Schematic overview of a BION chip integration system.

3.3.1 Design and Fabrication

The fabrication step for the parylene pocket that houses the BION chip is exactly the same as that of the RFID chip and is introduced in the previous section and chapter 2. Extra metal pads are made to house surface mount capacitors. The mask layout that is used to fabricate the structure is shown in figure 3.10. The outermost outlines are used to release the structure from the wafer, the traces are the conductive metal lines and the big rectangle pads are the exposed metals for bonding and electrodes. The chip is located in the middle of the structure, which is surrounded by the pocket etch holes.

The structure is 20 μm thick, 28 mm long and 4.8 mm wide. The size of the pocket is 1.3 mm wide and 2.9 mm long and is able to house the BION chip, which is 250 μm thick, 0.98 mm wide and 2.1 mm long.

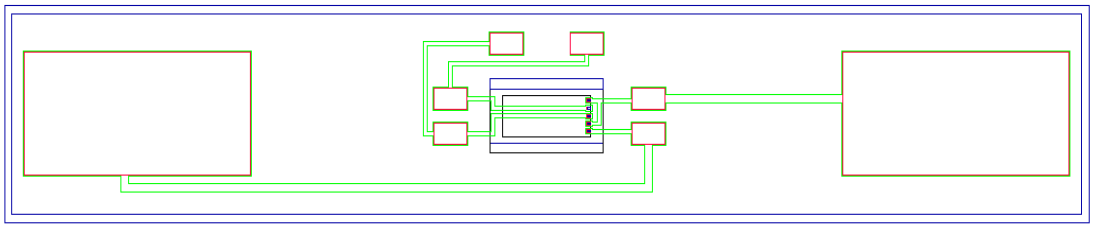


Figure 3.10. Mask layout for the parylene pocket structure for the BION chip.

3.3.2 System Integration Demonstration

Due to the number of pads that needs to be bonded in this process, it may become relatively more difficult for the chip to be completely aligned to the bonding pads on the parylene pocket structure. This is especially true for a system that has bonding pads in a two-dimensional arrangement (figure 3.11); if the movement of the chip is not constrained, it would be extremely difficult to set the chip in place during the bonding process. Thus, a sticky substrate on a commercially available substrate carrier (Gel-Pak Package, Gel-Pak, Hayward, CA, USA) is used to facilitate the fixture of the substrate during the alignment process.

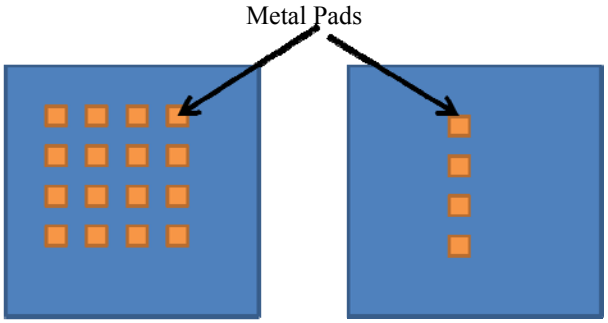


Figure 3.11. Chip pad arrangement; (left) two-dimensional arrangements; (right) one-dimensional arrangement.

The parylene pocket that will be bonded to the BION chip undergoes similar integration process as that of the RFID chip. This process is shown in figure 3.12, and it also involves the use of sticky surfaces to separate the two layers of parylene to enable the insertion of the chip. This step is followed by the application of the conductive epoxy,

which is very sensitive to hand movements when the pitch between the neighboring pads becomes smaller than 100 μm. A paintbrush or needle tip is often used to facilitate this process. Extreme care needs to be taken not to short neighboring devices and traces. A detailed process to fix short circuits and to handle high density connections will be covered in chapter 5.

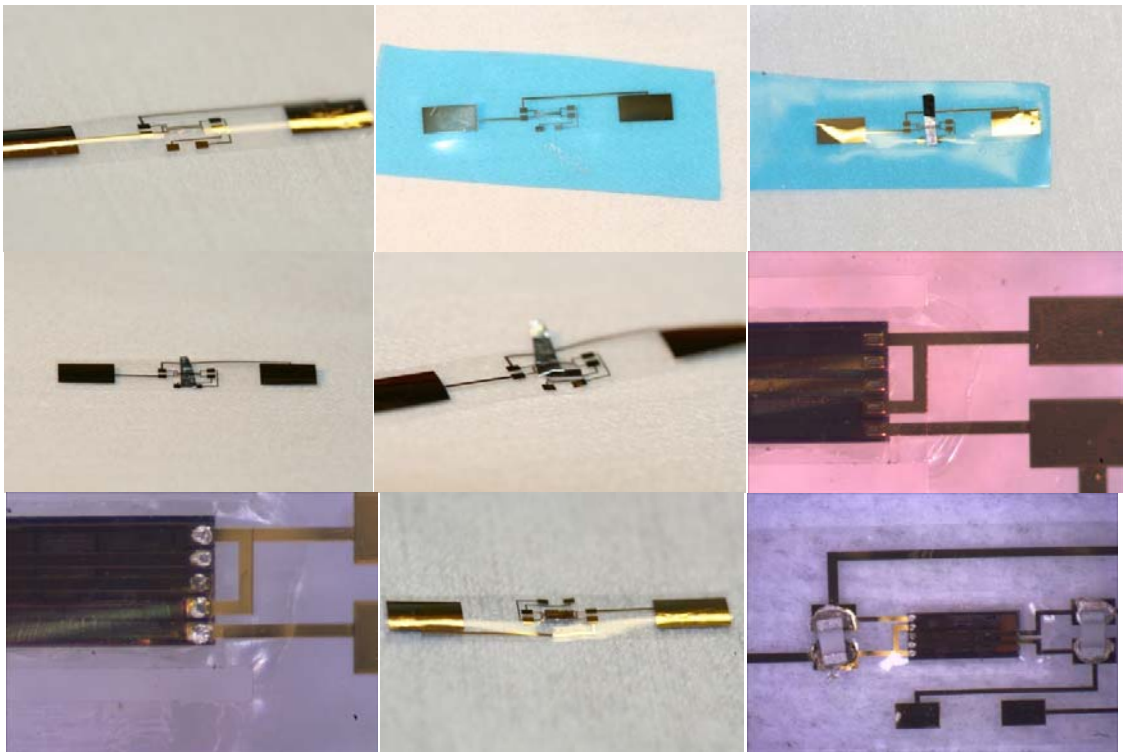


Figure 3.12. Step-by-step integration process of the BION chip.

The only difference between the integration of the BION chip and the RFID chip is the need for external discrete components. Two capacitors are needed to complete the BION system circuit. C_2 is a capacitor with capacitance of 22 nF, and C_1 is a tuning capacitor in parallel with the receiving coil in order to achieve a resonant frequency of approximately 480 kHz. These two capacitors are bonded onto the bonding pads of the parylene substrate with drops of biocompatible conductive epoxy. It should be noted that

the parylene pocket technology for discrete component can also be included in the design for the next iteration.

The bonded structure is cured in the oven at 80ºC for 90 minutes, followed by a 30 μm parylene C deposition to encapsulate the device, similar to the postprocess of the RFID integration. It should be noted that the parylene C and the biocompatible silicone protective layer deposition after the bonding process have become standard procedures for all fabrication of biological implantation devices fabricated in our lab. Its sealing capability will be characterized in chapter 4.

3.3.3 Functional System Testing

After the device has been assembled and coated, the structure is connected to a hand-wound receiving copper coil, which has Q factor of 250 at ~500 kHz. An iron core is used to magnify the electromagnetic field to increase the wireless transmission efficiency. Figure 3.13 shows the configuration ready for functionality testing.

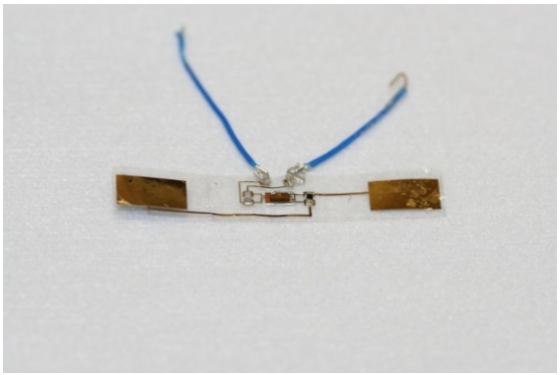


Figure 3.13. Packaged BION chip in the parylene substrate.

After the assembly, the functionality of the system is then validated with the setup similar to a clinical trial conducted by Dupont et al. [109], where a microprocessor based controller called “personal trainer” (built by Aztech Associates, Kingston, Ontario, Canada) is connected to a coil and a coil driver to send out the control signal that drives the BION

chip. This controller can be programmed to store pulses that vary in frequency, intensity, and duration. The pulses will be transmitted out by the hand-wound transmitting coil that was originally designed to be worn over the arm for muscle stimulation experiments (shown in figure 3.14)

The structure is then immersed in saline solution for an *in vitro* measurement. The device was immersed in saline and its output voltage recorded. Figure 3.15 shows the pulse measured from the electrode site when the personal trainer is transmitting signals. The pulse width is measured to be approximately 500 μs wide and has amplitude of approximately 7 V.

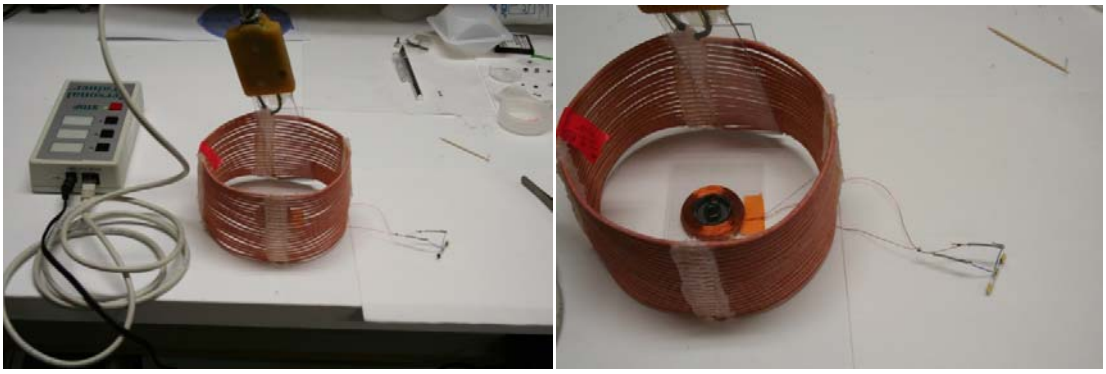


Figure 3.14. A telemetry setup for functionality test of the assembled BION system; (left) the complete set up with the personal trainer and the transmitting coil; (right) the receiving coil sitting inside the transmitting coil.

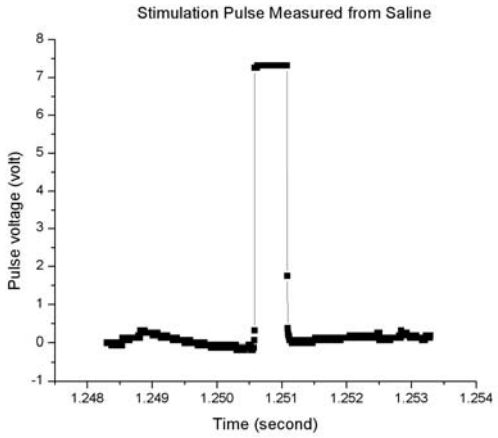


Figure 3.15. Typical simulation pulse measured from the electrode site.

3.4 Conclusion

In this chapter, the flexible parylene pocket chip integration technology has been successfully demonstrated by integrating two different commercially available ICs, including the RFID and BION chips. Additional discrete circuit components are also bonded to the muscle stimulator structure and both systems are functional tested. The fabrication process of the pocket, the detailed chip insertion, packaging and alignment process are also discussed and demonstrated. Preliminary integration result validates the efficacy and the functionality of the technology. The process is very scalable and has the potential to be fully automated; these two examples thus serve as very good guidelines for future integration schemes and excellent basis for the development of more intricate and elegant bonding and alignment process. A monolithic process to integrate MEMS coil and the parylene pocket is underway, and it would not be long before a totally integrated, implantable system could be tested *in vivo* in animal subjects. These positive results show promise for the development and advancement of technology for other more complex integrated biomedical implants for prosthetic applications.

4 PACKAGING, ACCELERATED LIFETIME TESTING AND MODELING

4.1 Introduction

Parylene C has been used extensively in biomedical device and interfaces as a conformal, biocompatible coating; it has also recently become an integrated part of our parylene-cabled silicon probes and parylene pocket. Because of its extensive use in these applications, its long-term stability in adverse implanted environments becomes increasingly important. The water permeability of parylene films [88, 130–134] and the parylene skin stability have been extensively studied by Li et al. [107]. It is shown that parylene can perform sufficiently well as a biocompatible insulator and that parylene protected gold is able to survive in human body temperature for over 60 years by the Arrhenius model. In this chapter, additional studies that are crucial to the success of a totally integrated and reliable biomedical device that involves silicon are presented.

It is found over the years that the adhesion capability of parylene to silicon may be compromised after thermal treatments, cleaning, handling, bench testing and implantations and may become a major failure mode for our parylene pocket on silicon substrate structure. The first part of this chapter will explore extensively new techniques including annealing, melting, anchoring, and XeF_2 silicon surface roughening to enhance the adhesions that are crucial to the successful implementation of our parylene pocket on silicon substrate. This chapter also reports the first quantitative experimental data on the

effectiveness of each through tearing, soaking, etching and ASTM peeling tests. The results show various improved adhesion means over the standard A-174 adhesion promotion. This improvement can greatly benefit the use of parylene on other applications as well.

Furthermore, a discussion of the efficacy of polymer and silicone protection of commercially available IC chips is also presented in this chapter. It can be shown that a combination of parylene C and biocompatible silicone coating greatly enhances the lifetime of the packaging technology and should be incorporated into our development process.

With positive results from the previous two experiments, the chapter concludes with an *in vivo* implantation of a mechanical model for the next generation retinal implant device for retinal prosthetic applications. Experiments need to be done on the retinal prosthetic system prior to the official clinical trial to optimize the geometry, surface treatment and packaging efficacy to ensure a reliable application. We have thus developed a pure mechanical structure for this purpose. It consists of a multielectrode array that has been heat formed to conform to a spherical shape, a parylene pocket structure with a silicon chip embedded and two coils that will be used for power and data transfer. The result of the surgery and future work are also presented.

4.2 Parylene to Silicon Interfacial Adhesion Enhancement

Recent technology developments in neural and retinal prosthesis have shown great promise; enabling the decoding of movement intention of those who have lost control of their limbs and the perceiving of visual data of blind subjects [10, 112]. The next milestones, however, include achieving a hermetic and biocompatible packaging scheme

for long-term total implantations. Parylene C has been utilized as a biocompatible packaging material for many applications [10, 112, 135–136]. It has superior insulative capability [137], pinhole-free conformality, low water permeability and its USP (United States Pharmacopoeia) Class VI biocompatibility. However, with the advancement of integrated parylene-cabled silicon probes [112] and parylene pocket IC integration technology [138], its adhesion abilities to silicon needs to be fully investigated and understood since it may otherwise cause severe damage and failure to the devices (figure 4.1).

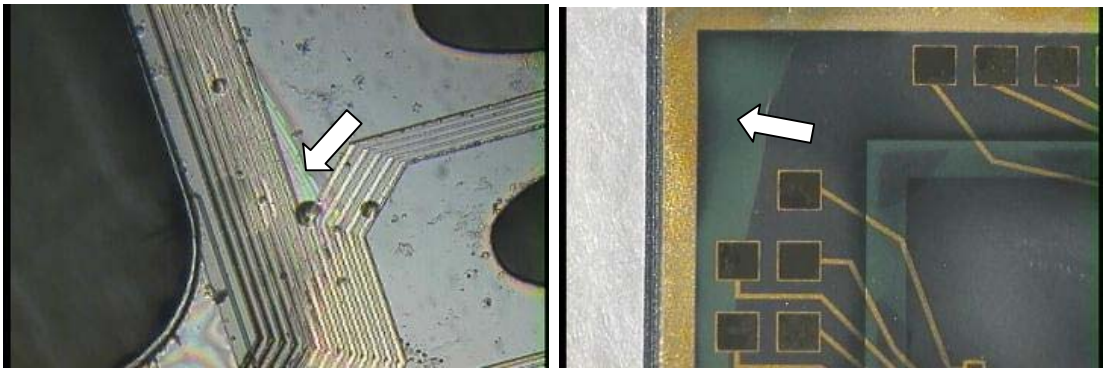


Figure 4.1. (left) Delamination occurs on an integrated parylene-cabled silicon probe and may eventually separate the parylene and the silicon probe; (right) delamination on the edge of an integration chip with parylene layers on top. The performance of the pocket is compromised due to the separation of parylene and silicon. The white arrows point out the difference in color, which indicates saline undercut.

Traditional parylene adhesion mechanisms include, but are not limited to, the application of A-174 adhesion promoter, which is a molecule with a hydrophilic silane head that adheres to the oxide and a carbohydrate tail that effectively “entangles” the parylene, and parylene anchoring [108], which is a physical mechanism to secure parylene in a trench created by both isotropic and anisotropic etching. However, the effectiveness of A-174 is limited by the thermal budget [139]. Parylene anchoring, on the other hand, requires advance DRIE techniques.

In this section we present several techniques for parylene adhesion enhancement and study their performances with numerous mechanical tests and soaking tests in saline (0.9 wt% NaCl solution), and provide quantitative experimental data on each. The purpose of these tests is to simulate the handling, dicing, testing, cleaning and implantation of real devices. We attempt to find adhesion techniques that (1) help parylene adhere well to silicon surfaces in pulling tests, (2) reduce undercut rate in accelerated soaking tests, (3) have low thermal budget and (4) are easy and inexpensive to implement. These properties are crucial to the fabrication of the parylene pocket on silicon substrate.

4.2.1 Sample Preparation

For the experiments, we use 500 μm thick, single side polished silicon prime wafers. The silicon substrate samples are treated prior to a 10 μm parylene C chemical vapor deposition. Figure 4.2 shows the process steps for each type of treatment. The list includes:

1. Buffer HF cleaning only, on prime wafer to achieve hydrophobic surface
2. XeF_2 silicon [80] surface roughening (with etching depth of 6.5 μm) to increase surface area and to enhance mechanical adhesion of parylene to silicon
3. Parylene anchoring with a continuous circular trench depth of 10 μm and a trench opening of 10 μm
4. Parylene melting [140]—the entire layer of parylene (10 μm) is deposited by room temperature CVD process and later melted in hydrogen gas filled oven at 350ºC.
5. A-174 adhesion promotion for 30 minutes under room temperature, and
6. Regular parylene (10 μm) on top of a thin (1 μm) layer of molten parylene. This thin molten layer acts as the adhesion layer for the regular parylene layer.

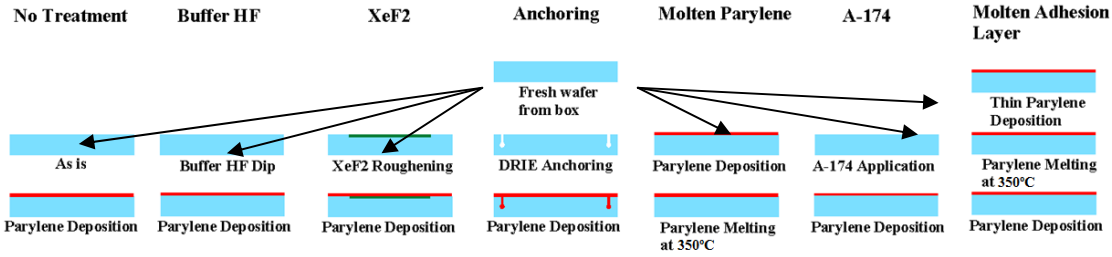


Figure 4.2. Process steps for different treatment; all of the process steps start with a 500 µm thickness prime silicon wafer that goes through the treatment and then has parylene deposited on top of it. The control sample of this experiment has parylene deposited on top of a blank wafer without any type of treatment.

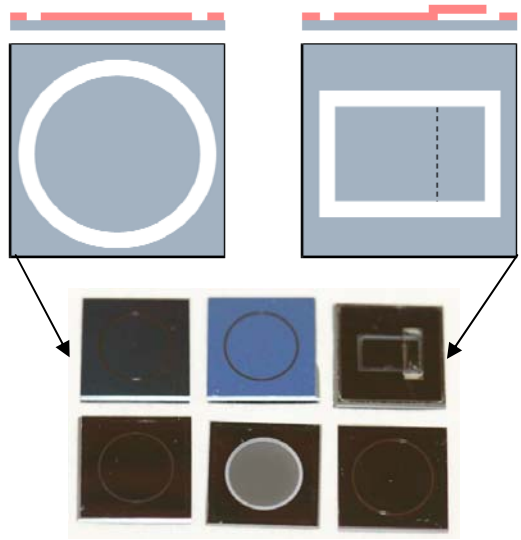


Figure 4.3. (top left) Sample layout for soaking tests. The diameter of the circle is 6.8 mm; (top right) sample layout for peeling tests (3 mm × 5.7 mm). For those used for peeling tests, photoresist is used as sacrificial layer to create the partial film. All trenches are 250 µm wide; (bottom) actual samples.

Two layouts are designed to accommodate the different types of tests (figure 4.3). For the samples used to release partial films for force peeling tests, sacrificial photoresist of 2 µm is first spun onto the wafer before the treatments. This sample is then released in acetone and photoresist stripper at room temperature to achieve the partial film structure.

4.2.2 Experiments

Four different types of peeling and soaking tests are conducted on the samples. The tests include partial film standard peeling test, ASTM tape peeling test, accelerated

soaking test, and HF soaking test. These tests are to simulate the process steps that a sample goes through during a standard MEMS process for biocompatible and implantable devices.

4.2.2.1 Partial Film Peeling Test

In the partial film peeling test, we attempt to examine the force the parylene coating is able to accommodate during handling of the device before the biocompatible layer is compromised. We do so by recording the adhesion force from pulling the partial film away from the silicon substrate. A force gauge (Chatillon DFS Series Digital Force Gauge S-DFS-0002, Ametek TCI Division, Florida, USA) is used to pull the partially released film at 90 degree and 100 μm/s. Maximum forces achieved are recorded to compare the adhesion force for different treatments. The maximum force can occur either just before the film is starting to peel away from the substrate or just before it is torn (figure 4.4). A sample pulling force vs. time plot of a film that achieved maximum force before the film is peeled away is shown in figure 4.5. Table 4.1 shows that the molten parylene has the highest adhesion force among all treatments. The table also implies that annealing at 200ºC degrades the adhesion force for all treatment samples (figure 4.6), while the nonannealed samples exhibit adhesion forces greater than the tearing force of a 3 mm wide, 10 μm thick parylene film. This degradation of the adhesion force may be due to thermal stress and the removal of physically absorbed water in silicon at the annealing temperature (200ºC) leaving hydroxyl group and voids in contact with the parylene film [141]. Annealing has little effect on the adhesion force from the parylene anchoring treatment and parylene on molten adhesion layer.

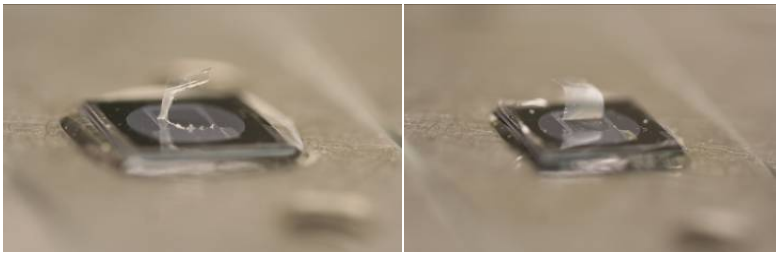


Figure 4.4. (left) Partial film torn before the film is peeled away from the substrate; (right) partial film completely peeled away.

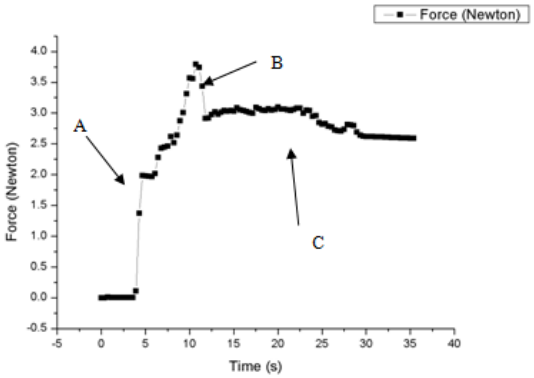


Figure 4.5. Time vs. force plot of a parylene film being pulled away from the silicon substrate. Section A is the elastic part of the pulling process, where section B represents rupture and C represents the residual constant force.

Table 4.1. Force gauge maximum force readings of the peeling test (n = 4). NA = nonannealed, A = annealed. Molten parylene has the highest adhesion force.

Treatment	Annealed	Max Force (N)	Parylene Tear?
No Treatment	No	0.12 ± 0.03	No
No Treatment	Yes	0.22 ± 0.04	No
HF Cleaned	No	1.41 ± 0.16	Yes
HF Cleaned	Yes	0.41 ± 0.08	No
XeF_2	No	1.46 ± 0.19	Yes
XeF_2	Yes	0.92 ± 0.10	No
Parylene Anchoring	No	1.62 ± 0.16	Yes
Parylene Anchoring	Yes	1.47 ± 0.10	Yes
Molten Adhesion Layer	No	1.51 ± 0.05	Yes
Molten Adhesion Layer	Yes	1.47 ± 0.05	No
A-174	No	1.78 ± 0.21	Yes
A-174	Yes	0.66 ± 0.12	No
Molten Parylene	-	2.52 ± 0.12	Yes

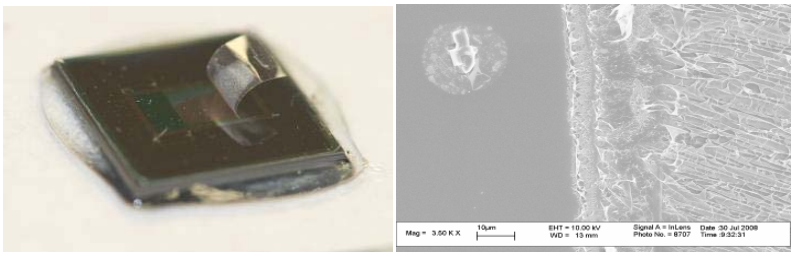


Figure 4.6. (left) Molten adhesion layer sample (after testing) for pulling test; (right) SEM of the peeled interface.

In the partial film peeling test, some of the annealed parylene partial films are torn before they are peeled off from the substrate. Thus, a parylene tearing test is conducted to investigate the mechanical property of annealed parylene. Strips of parylene films are made and pulled from one side with the other side fixed. The maximum length before the tearing is recorded. Result shows nonannealed parylene is able to stretch more than 100% of its own length while annealed parylene is more brittle and is not able to stretch more than 10% before tearing. This is due to the recrystallization of the polymer chains above the glass transition temperature and the larger grain size in parylene after the annealing. Further work in this section include constant tension test on parylene strips to observe the failure modes.

4.2.2.2 ASTM Standard Tape Peeling Test

In the ASTM standard tape peeling test, we attempt to examine the adhesion performance of each treatment after sterilization step for bioimplantable devices. We do so by soaking the samples in saline solution at 121ºC for one hour, simulating the steam heating sterilization environment. A 5 cm Scotch brand tape (#810) segment is then used to peel a 4 by 4 grid pattern cross cut on the parylene sample in 1 mm pitch by razor blades in accordance with ASTM D3359B. The result of the peeling is then classified

based on how much of the original film is left on the substrate. The classification of the peeling test is shown in table 4.2.

Table 4.3 shows the result of the peeling test. It is observed that parylene adheres best on surface treated with XeF_2 etching and when it is melted. These two samples are able to withstand the tape peeling force (figure 4.7) while other samples treated with parylene anchoring and A-174, for example, have no adhesion left after the tape is peeled off.

Table 4.2. ASTM D3395B Grading (% film removed).

Grade	**5B**	**4B**	**3B**
% removed	0%	<5%	5%–15%
Grade	**2B**	**1B**	**0B**
% removed	15%–35%	35%–65%	>65%

Table 4.3. Result of the ASTM cross-cut test (n = 2).

	After 1 hour sterilization @ 120°C Before Peeling	**After Peeling**
No Treatment	0B	0B
HF Cleaned	5B	1B
XeF_2	5B	4B
Parylene Anchoring	5B	0B
Molten Adhesion Layer	5B	5B
A-174	5B	0B
Molten Parylene	5B	1B

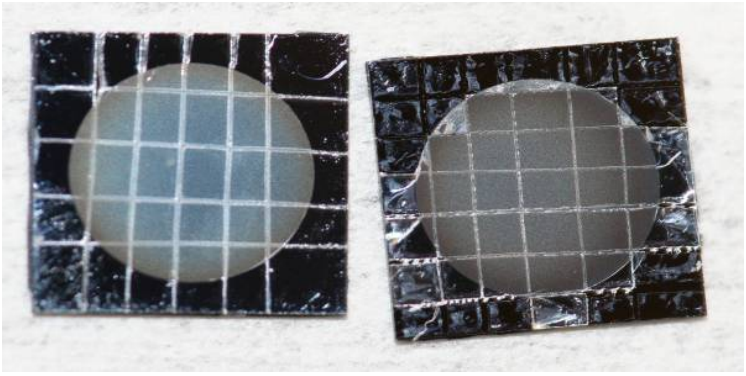


Figure 4.7. ASTM cross-cut test; (left) XeF_2 treated surface with parylene before 120ºC one hour soaking; (right) after Scotch tape peeling, parylene on the treated surface is still intact. The circular shape surfaces in the samples are XeF_2 treated surfaces.

4.2.2.3 Accelerated Soaking Tests

In the accelerated soaking tests, samples are immersed in 60ºC, 80ºC, 90ºC saline solution to allow daily observation of the delamination/undercut rate of the interface. We can then use this data to extrapolate the MTTF (mean time to failure) of the adhesion for the parylene-coated device during chronic long-term implantation at normal body temperature (37ºC).

The Arrhenius relationship calculation is used to extrapolate the MTTF at body temperature [142] by taking MTTF at two data points at a higher temperature. The equation of the relationship at a given system temperature T (in Kelvin) is expressed by

$$MTTF = Aexp\left(-\frac{E_a}{kT}\right),$$

where A is the preexponential constant, E_a is the activation energy of failures (in eV), and k is the Boltzmann's constant (8.62×10^{-5} eV–K^{-1}).

From the result, nonannealed parylene anchoring and molten adhesion layer show no undercut for over 30 days (figure 4.8) while annealed A-174 and XeF_2 treated samples show undercut rate of more than 100 μm a day at 60ºC (table 4.4). Results also suggest

that annealing increases the undercut rate of the parylene samples during the soak test (figure 4.9).

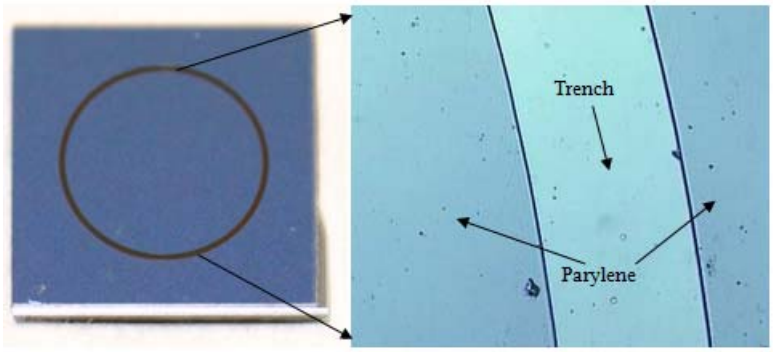


Figure 4.8. Annealed sample with molten adhesion layer 90ºC soaking result.

Results also show that the saline solution penetrates the parylene from the top of the film and creates delamination bubbles for nonannealed samples, while the annealed samples have no such problem.

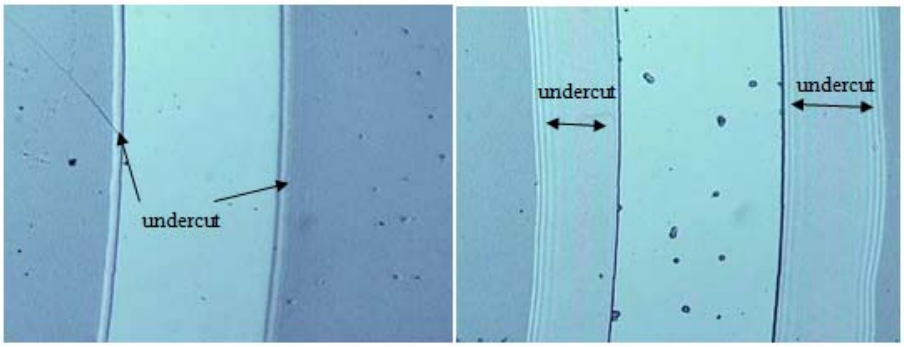


Figure 4.9. Sample with molten adhesion layer 90ºC soaking result; the trench is 200 µm wide. (left) Nonannealed samples have lower undercut rate than their annealed counterparts (right)

Table 4.4. Accelerated life time testing to observe the undercut rate of the parylene/silicon interface (n = 3).

		Soak peeling 30 days			
		Annealed		**Nonannealed**	
Temp. °C	**Treatment**	**Undercut Rate (µm/day)**	**Vertical Attack?**	**Undercut Rate (µm/day)**	**Vertical Attack?**
60	HF Cleaned	10.0	No	7.8	No
80	HF Cleaned	11.7	No	13.3	No
90	HF Cleaned	14.0	No	16.7	Yes

60	XeF_2	>100	No	8.2	No
80	XeF_2	>100	No	9.2	No
90	XeF_2	>100	No	23.3	Yes
60	Parylene Anchoring	0.0	No	0.0	No
80	Parylene Anchoring	0.0	No	0.0	Yes
90	Parylene Anchoring	0.0	No	0.0	Yes
60	A-174	>100	No	14.7	No
80	A-174	>100	No	26.7	Yes
90	A-174	>100	No	51.7	Yes
60	Molten Adhesion	0.8	No	0.0	No
80	Molten Adhesion	1.0	No	0.0	No
90	Molten Adhesion	1.2	No	0.0	Yes

4.2.2.4 HF Soaking Tests

Finally, samples are immersed in 48% HF to simulate device cleaning. The result shows heavy undercut for all samples except parylene anchoring. However, HF is able to vertically penetrate all films regardless of treatment in less than a minute (figure 4.10).

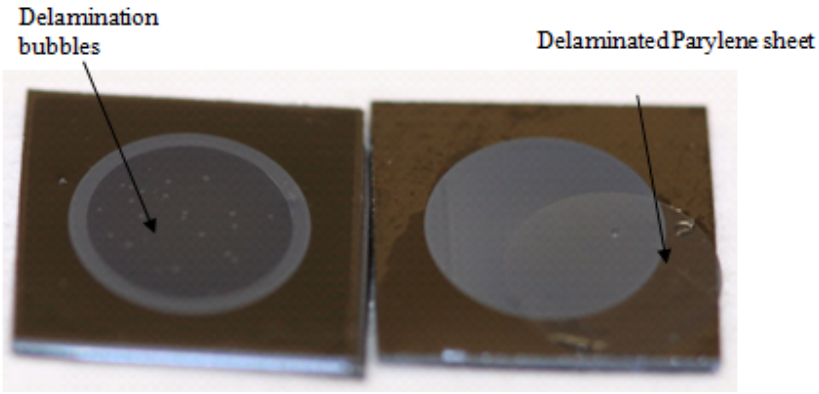


Figure 4.10. XeF_2 treated samples after 48% HF cleaning for (left) 1 minute; (right) 10 minutes. The delamination bubbles in the middle of the island are clearly shown.

4.2.2.5 Conclusion

In conclusion, the parylene molten adhesion layer provides the most promising result among the adhesion enhancement processes in the above four experiments. However, this result remains unsatisfactory as parylene still does not have a permanent

adhesion on silicon and can still delaminate or deteriorate under the adverse environment in human tissue and/or during handling and testing of the structures. Additional studies and methods must be investigated to further evaluate the performance of our packaging paradigm.

4.3 Accelerated Lifetime Soaking Test of Protected ICs

The parylene pocket technology discussed in the previous chapters can either be implemented on silicon or parylene substrate. However, having learned that parylene does not have perfect adhesion on silicon, it becomes extremely crucial to characterize the mean time to failure and the reliability performance of our packaging technology.

At the end of every integration process, the IC that is to be integrated with our system is coated with another layer of protective parylene and sealed with a layer of biocompatible epoxy. This section studies the sealing performance of each of these treatments and investigates the failure mode of each sample. In order to do this, dummy chips with conduction traces are fabricated in-house and accelerated lifetime testing is performed on them. Commercially available chips are not used, in order to isolate the failure modes of the life time soaking test.

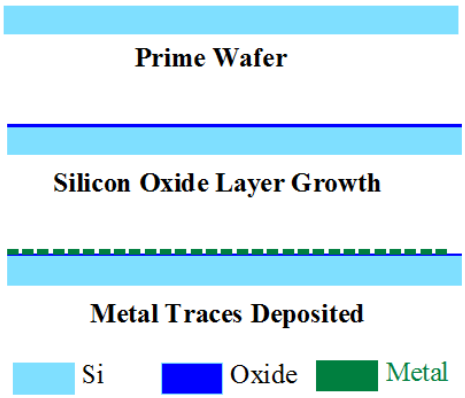


Figure 4.11. Conduction chip fabrication process.

The chip is fabricated with the following process steps (figure 4.11). First, 1 μm of thermal oxide is grown on a prime untreated silicon wafer after piranha treatment. Cr/Au (0.05/0.2 μm) is then deposited on the wafer with electron beam evaporator. This layer of metal is subsequently patterned with a lithography step and metal etching step to make the conduction traces. The wafer is then diced to harvest the individual conduction chips that are 5 mm × 5 mm × 200 μm in size.

4.3.1 Samples Preparation

We plan to observe and compare the sealing and packaging performance of different integration schemes. The following samples are prepared:

1. Parylene pocket on parylene substrate coated with 30 μm protective layer of parylene and biocompatible silicone
2. Parylene pocket on silicon substrate coated with 30 μm protective layer of parylene and biocompatible silicone
3. Bare die coated with 30 μm protective layer of parylene
4. Bare die coated with 10 μm protective layer of parylene
5. Bare die coated with protective layer of biocompatible silicone
6. Bare die

Samples 1 and 2 are used to compare the reliability and the performance between parylene pocket on parylene and silicon substrate. The hypothesis is that the pocket on silicon substrate has a shorter MTTF than the pocket on parylene substrate due to an inferior adhesion performance of parylene to silicon. Samples 3 and 4 are used to compare the effectiveness of parylene thickness on lengthening the MTTF. It is believed that the thicker the parylene that is coated on the device, the longer it would survive in harsh environments such as this. Sample 5 is used as a control sample to observe if biocompatible silicone alone would be sufficient to protect the device in saline for long-term

implantations. Sample 6 is used as another control to show how long it would take metal to degrade in saline environment without any means of protection. Both passive and active soaking tests are conducted to observe different failure modes. The silicone used in all of the experiments is MDX4-4210 (Silastic MDX4-4210 Biomedical Grade Elastomer with Catalyst, Dow Corning Corporation, Midland, Michigan, USA), a two-part silicone elastomer.

4.3.2 Passive Soaking

A soaking test without any connected circuitry on the chip is first performed to observe metal corrosion failures. The samples are placed in a bottle with saline solution and heated to the desire temperature in a convection oven. The samples (shown in figure 4.12) are prepared by cleaning chips with isopropanol alcohol and DI water, followed by their respective coatings and treatments as mentioned in the previous section. During the soaking period, the samples are daily examined under optical microscope to observe metal delaminations, corrosions and other failure modes. An undamaged bare chip with metal traces is shown in figure 4.13. For the passive soaking test, 1 mm of biocompatible silicone is coated on each side of the chip (2 mm total).

After the testing period, the chips are taken out of the hot saline solution for conduction test. A Wentworth Labs 11PO900 probe station (Wentworth Laboratories, Brookfield, CT, USA) is used to probe the traces. The coatings and the packaging on the chip are removed before the conduction test is performed. Result shows the bare chip without any parylene and silicone coating suffers from metal delamination (shown in figure 4.14) and corrosion after 1 day in 110ºC, after 2 days in 90ºC and 5 days in 60ºC. The results for the rest of the experiment are summarized in table 4.5. MTTF (mean time

to failure) is defined as the time when the first sign of metal delamination is seen on the chip.

It has been studied that plasma treatment of the external surfaces may be beneficial due to the increase in hydrophilicity behavior of the overall structure, thus promoting the blood biocompatibility of the device [143] and additional epoxy/silicone coating.

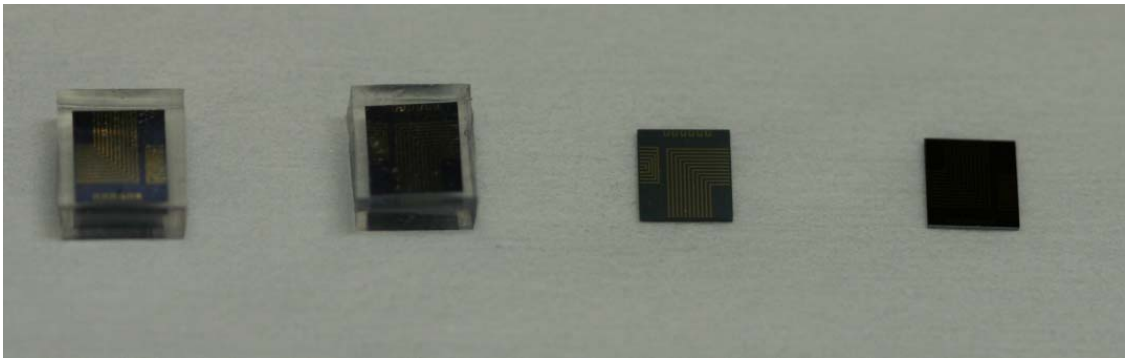


Figure 4.12. Soaking samples from left to right: bare die coated with both biocompatible silicone and parylene, bare die coated with biocompatible silicone, bare die coated with parylene, bare die.

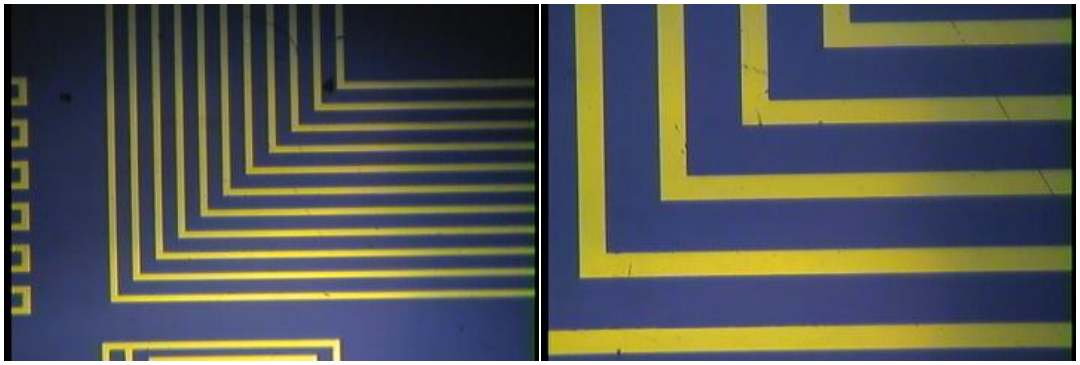


Figure 4.13. Undamaged metal lines on the bare die before soaking.

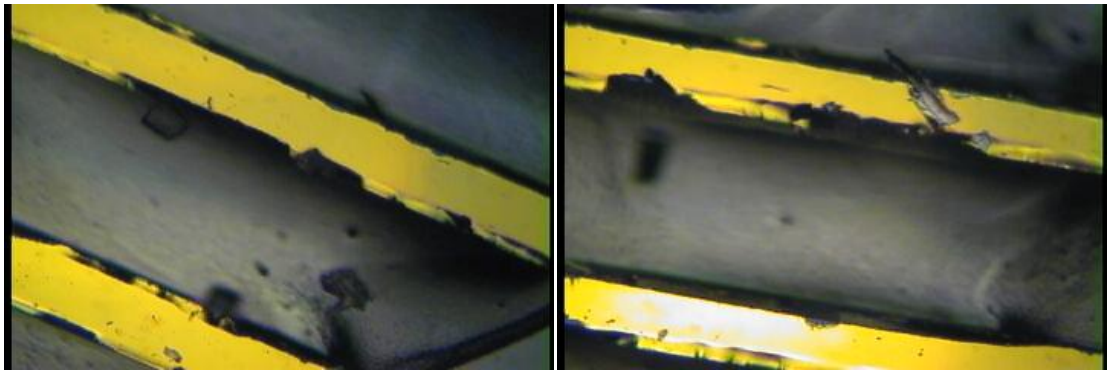


Figure 4.14. Delaminated metal lines on the bare die after 2 days of soaking at 110ºC.

Table 4.5. MTTF of conduction chips in different packaging.

	Sample 3	**Sample 4**	**Sample 5**	**Sample 6**
110°C	8 days	6 days	6 days	1 days
90°C	25 days	10 days	15 days	2 days
60°C	40+ days	40+ days	40+ days	5 days
37°C (From extrapolation)	2.8 years	2 months	0.83 years	20 days
Q (Activation Energy)	−0.68 eV	−0.3 eV	−0.58 eV	−0.41 eV

4.3.3 Diffusion of Electrolyte in Silicone

It is shown in the previous section that the biocompatible silicone that is used in the packaging of the chips would still fail after long-term exposure in high temperature and high humidity condition. Humidity, being one of the main causes of failure in organic compounds like silicone and parylene when implanted, needs to be investigated to more accurately estimate and understand the exact failure modes. Knowing how much moisture has penetrated the silicone protection layer will allow us to more accurately predict the mean time to failure of the metal lines. From studies of Riggs et al. [144], Almquist and Hwang [145], and De Kee et al. [146], it has been shown that the moisture absorption process follows Fick's law.

Diffusion of saline solution through a membrane can be modeled by Fick's diffusion law.

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2} + \frac{\partial^2 c}{\partial y^2} + \frac{\partial^2 c}{\partial z^2}$$

where D is the coefficient of diffusion, c is the concentration of media and t is the time.

The model can be simplified into one-dimension

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2}$$

where

$$D = \frac{{x_0}^2}{\pi t}$$

Also, if we take into account the edge effect [147], the new diffusion constant would become

$$D = D_x\left[1 + \left(\frac{d}{b}\right) + \left(\frac{d}{l}\right)\right]^2$$

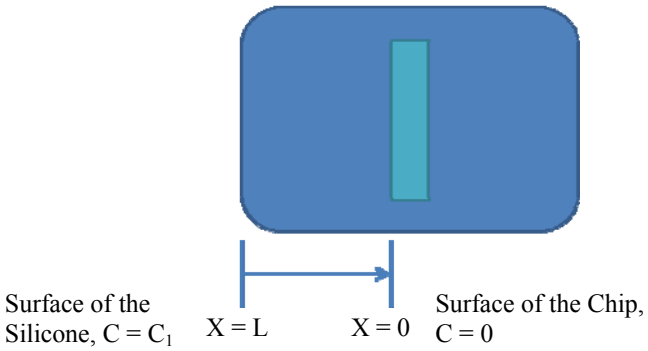
where b and l are the sample breadth and length. In our case:

$$D_x = \frac{{x_0}^2}{\pi t}\left[1 + \left(\frac{d}{b}\right) + \left(\frac{d}{l}\right)\right]^{-2}$$

$$= \frac{(2\ mm)^2}{\pi(\sim 10\ days)}\left[1 + \left(\frac{2\ mm}{5\ mm}\right) + \left(\frac{2\ mm}{5\ mm}\right)\right]^{-2}$$

$$= 4.548 \times 10^{-7}\ mm^2/s$$

Since this packaging is immersed in saline during the reliability testing.



$$c = c_1, x \leq 0 \; and \; t = 0$$

$$c = c_0, 0 < x < L \; and \; t = 0$$

$$c = 0, x = L \; and \; t = 0$$

This is the case for uniform initial distribution with surface concentrations different. One face of the membrane $x = 0$, is kept at a constant concentration $c = c_1$, and the other $x = L$, at $c = c_2 = 0$. The membrane is initially at a uniform concentration $c = c_0 = 0$. During steady state condition, the concentration can be solved by separation of variables [148] and follows:

$$C = C_1 + (C_2 - C_1)\frac{x}{L} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{C_2\cos n\pi - C_1}{n}\sin\frac{n\pi x}{L}e^{-\frac{Dn^2\pi^2 t}{L^2}}$$

$$+ 4\frac{C_0}{\pi}\sum_{m=1}^{\infty}\frac{1}{2m+1}\sin\frac{(2m+1)\pi x}{L}e^{-\frac{D(2m+1)^2\pi^2 t}{L^2}}$$

As M_t denotes the total amount of diffusing substance that enters the sheet during the time t and M_∞, the corresponding amount during infinite time, then

$$\frac{M_t}{M_\infty} = 1 - \frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\exp\left(-\frac{D(2n+1)^2\pi^2 t}{l^2}\right)$$

In this case

$$M_\infty = L\left(\frac{C_1 + C_2}{2} - C_0\right)$$

An experiment was done to monitor the weight change of the packaged chip to determine absorption process of 0.9 wt% NaCl solution. However, if we consider the sample that was used in our regular soaking test, the diffusion length would equal 1 mm, and our equations would become

$$M_\infty = 1\,mm \times \left(\frac{1.54 \times 10^{-7}\,mol/mm^3 + 0\,mol/mm^3}{2} - 0\,mol/mm^3\right) \times 58 g/mol$$

$$= 4.466 \times 10^{-6} g/mm^2$$

The samples are cleaned with alcohol and dried before saline immersion. The result is shown in figure 4.15, which predicts that the moisture diffusion in silicone occurs in matter of days under elevated temperature and would corrode the metal lines inside the packaging.

Although this model gives a fit for the water sorption ability of the silicone for thin layers and for absorption in short-term, there are second-order effects that would affect the absorption for thicker samples in the long run. Thus, further diffusivity, degradation and solubility tests that fully comply with ASTM standards should be conducted. The result from these investigations will allow better understanding of the packaging failure modes. It not only will allow us to determine how much moisture is diffused into the packaging, but also enables a more accurate modeling of the lifetime of the metal line on the packaged chip due to corrosion.

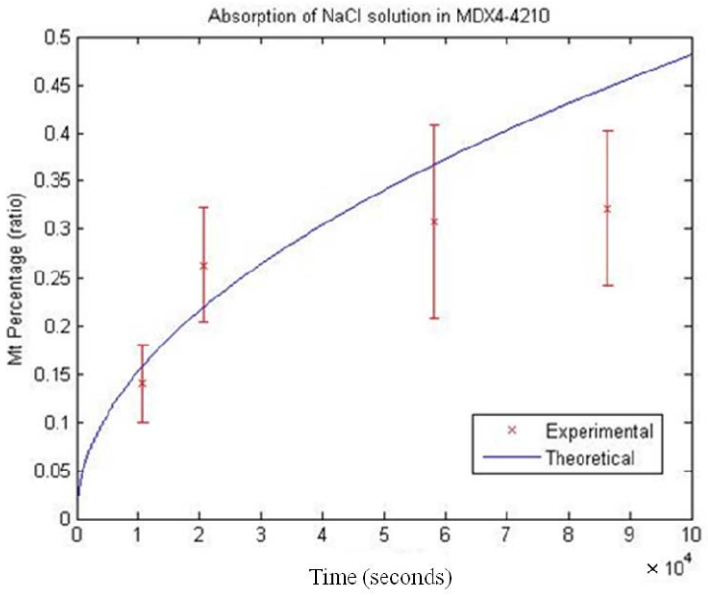


Figure 4.15. Absorption of NaCl solution in silicone.

4.3.4 Active Soaking

The result from the passive soaking test shows that coating with parylene and a layer of biocompatible silicone dramatically increase the lifetime of a chip. The result of the diffusion modeling also suggests that increasing the thickness of the biocompatible silicone will increase the time it takes for moisture to reach the chip. In order to further evaluate the mean time to failure of our packaging technology, the chip is packaged in the parylene pocket on both parylene and silicon substrate with parylene and a biocompatible silicone coating for active soaking. A 5 V DC power supply is connected to the chip, and its current is constantly monitored using an HP 54503A oscilloscope. The mean time to failure is defined as the time when the current dramatically changes, which signifies the failure on the trace lines. In this active soaking, 2 mm of biocompatible silicone is coated on each side of the chip (4 mm total). This coated layer is thicker than that of the passive soaking (which is just 1 mm on each side).

The main failure that we want to observe in this experiment is the line corrosion due to moisture diffusion into the package. The failure is defined by a 50% change in the line resistance. Figure 4.16 shows the line resistance versus time soaked in saline.

The samples are soaked in saline solution at three different temperatures. Three samples of each category are tested under each condition. In fact, all samples are able to survive in 110ºC for around 20–25 days before signs of deterioration and failure. This result translates to more than 7 years of survival period in human body temperature of 37ºC, shown in table 4.6. It is observed, however, that the silicone is easily delaminated in saline from the silicon substrate under high temperature soaking.

It was anticipated that failure modes such as parylene cracking (possibly due to glass transition temperature and/or thermal stress from the electrical connection) and difference in thermal expansion coefficient of parylene, metal and conductive epoxy would occur during the soaking test. We have not, however, observed any failure in this regard. It is believed that the combination of parylene and an extra layer of biocompatible silicone contribute to the enhanced protection of this packaging technique. The active soaking test is still ongoing, and more experimental results are expected to enable a complete understanding of parylene pocket packaging behaviors.

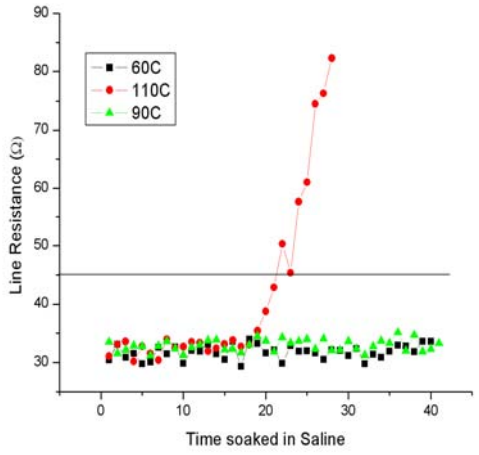


Figure 4.16. Line resistance vs. time soaked in saline solution.

Table 4.6. MTTF of conduction chips in parylene pocket (estimation assumes an Arrhenius activation energy factor of 2 for every 10ºC).

	Sample 1	**Sample 2**
110ºC	25 days	20 days
90ºC	40+ days	40+ days
60ºC	40+ days	40+ days
37ºC (From estimation)	At least 8 years	At least 7 years

4.3.5 Conductive Epoxy

In addition to soaking the packaging of the chip, the conductive epoxy that is responsible for providing the electrical and mechanical connection between the bonding pads are also soak tested in this experiment. Copper wires are bonded together and fixed on parylene and silicon surface for this test to investigate the failure mode of the epoxy bonding without any type of protection.

It is found that the conductive epoxy degrades and the conductive material contaminates the saline while 100% exposed in the solution. However, this degradation effect is not observed in these samples when parylene and the silicone are applied around them (shown in figure 4.17).

It is also found that the adhesion lifetime of the conductive epoxy on silicon is longer than that of the conductive epoxy on parylene (shown in table 4.6). Delamination is not observed in these samples when parylene and silicone are applied around them.

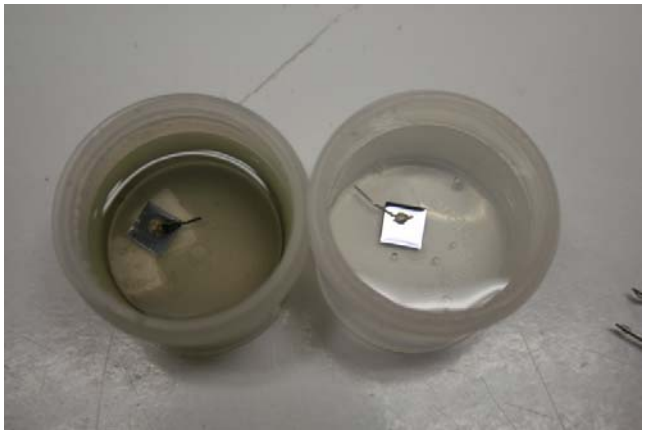


Figure 4.17. (left) Conductive epoxy filling diffused into surrounding saline solution; the silver residue can be seen coated on the side of the container; (right) this effect is not observed in sample coated with parylene and biocompatible silicone.

Table 4.7. MTTF of conductive epoxy adhesion on different surfaces.

	Epoxy on Silicon	**Epoxy on Parylene**
110ºC	16 days	31 days
90ºC	40+ days	40+ days
60ºC	40+ days	40+ days

Finally, a fully integrated RFID chip in parylene pocket is soaked in saline. This experiment allows us to observe different failure modes such as corrosion of line in parylene skin, corrosion of conductive epoxy and corrosion of bonding pad on the chip. The setup can be seen in figure 4.18. This 60ºC soaking test is on-going and is expected to last several months before signs of failure.

It should be noted that the Arrhenius relationship, while useful in estimating the mean time to failure of one specific failure mode at different temperatures, should not be used for full system failure mode analysis. In other words, instead of treating the entire system as one failure, each failure mode in the system should be individually identified and analyzed.

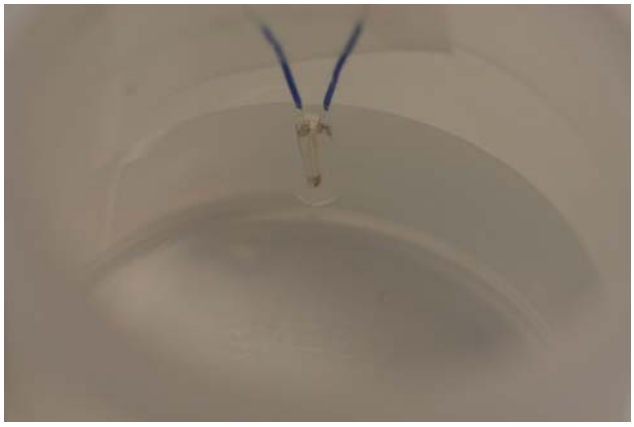


Figure 4.18. Active soaking of parylene pocket that houses an RFID chip.

4.4 Mechanical Model for Implantation Studies

Previous chapters have shown the fabrication process and integration techniques for the parylene pocket technology by integration with different circuits and device components. Previous sections have also shown the performance of such technology in harsh environments *in vitro* by soak testing in saline solutions under different temperatures. In this section, a mechanical model of an intraocular system is developed and built based on these results to investigate the feasibility and the details of the surgical implantation process *in vivo*. It is crucial to determine the optimal system geometries before a chronic implantation for animal testing due to the limited availability and the complexity of obtaining animal models. It is also important to observe and consider all possible failure modes during surgery and develop a comprehensive disaster-proof surgical protocol to prevent possible catastrophes during chronic implantations. In all, the robustness of a complete integrated system can only be realistically verified via an *in vivo* implantation.

An intraocular test platform is designed and fabricated. This geometry platform simulates the overall profiles of the required components without the functionality complexities and is fabricated with RIE etching process. The overall fabrication process for the parylene sections is shown in figure 4.19.

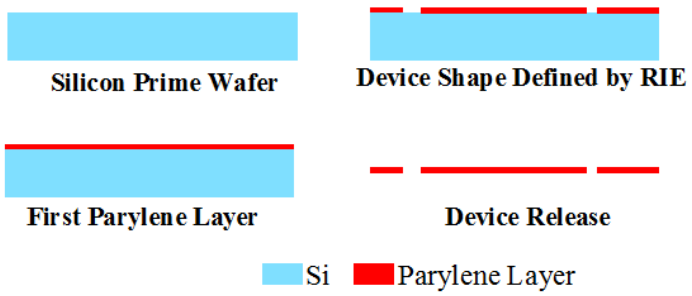


Figure 4.19. Fabrication step of parylene-only structures for mechanical model.

The overall mechanical design includes an a multielectrode array region to be attached to the retina using a retinal tack, a RF coil region intended for implantation in the lens capsule, a dummy chip parylene pocket section partway down the parylene cable and a flexible cable section that connects these components together. The array part is heat shaped using a custom 6061 aluminum mold comprising a recessed concave region and a mating stainless steel sphere that approximates the curvature of the canine retina (diameter ~22 mm), as shown in figure 4.20. During the heat-shape process, the multielectrode array parylene section is sandwiched between the spherical ball and the molding surface, while the cable is pressed flat against the aluminum surface. Finally, dummy chips are bonded inside the parylene pocket and bonded on one of the possible positions anticipated for the ASICs. In order to reduce fabrication complexity, the coil part and the array part are separately fabricated in this dummy system. Finally, the two separate parts (the coil region and the array region) are bonded together using epoxy. After all components are glued together, the final devices is coated with a layer of biocompatible silicone and sterilized to increase the biocompatibility for surgery.

Figure 4.20. Custom heat-forming mold.

4.4.1 First Version Mechanical Model

An intraocular model was designed using coiled and coated stainless steel wire of 0.991 mm diameter to model the power coil. The box of electronics was modeled with a 6 mm × 6 mm × 2 mm rectangular silicone block. The data coil was modeled with a

commercially available anterior chamber intraocular lens (ACIOL) (Model # 122UV, Bausch & Lomb, Rochester, NY, USA). Parylene C was used to connect the components together and to model the electrode array. This first-generation intraocular model can be seen in figure 4.21.

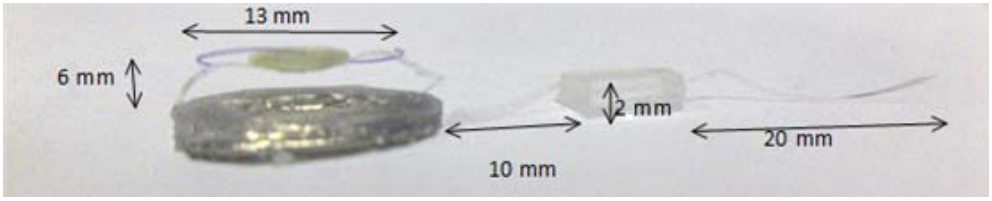


Figure 4.21. First generation completely intraocular model.

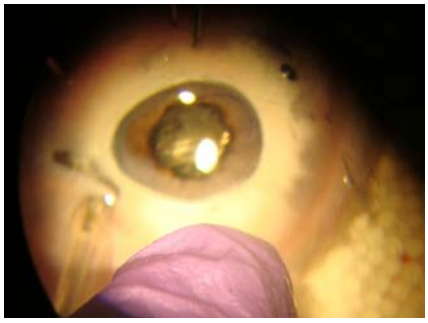


Figure 4.22. First generation completely intraocular model in porcine eye.

This model was first implanted September 18, 2009 into porcine eyes as seen in figure 4.22. However, after a few porcine eye surgeries, it was decided that the all-intraocular model would not work at this time because of the large dimensions necessary for the intraocular power coil. Also, there was an unresolved issue of securing the intraocular power coil so that there would be minimum movement within the eye. Excessive movement, especially when combined with the size of the power coil, would likely damage the eye.

4.4.2 Second Version Mechanical Model

A partial intraocular and partial extraocular design was evaluated after the first set of surgeries, as shown in figure 4.23. In this new design, the power coil sits outside the eye

with a wire cable entering the eye and connecting the box of electronic components to supply it with power. This box is then connected to the parylene cable and subsequently to the heat molded parylene multielectrode array. The design for this parylene cable is shown in figure 4.24.

The intraocular lens models for the data coil and a parylene C cable connects it to the box of electronics. The wire used for the power coil was 99.99% gold wire with 5 mil, (or 0.125 mm) diameter and is coated with the biocompatible silicone. The final thickness of the coil is 0.4 mm with the major axis of the ellipse being 23.25 mm and the minor axis being 9 mm. The intraocular lens has dimensions of ~7 mm in inner diameter, ~14 mm in outer diameter including the haptics, and ~1.5 mm in total thickness (figure 4.25).

In this design, the parylene pocket is used as the mechanism to house the chip that models the real ASIC. In the final system, this part is a rectangular silicone prism that houses all electronic components, including IC chips and discrete components integrated and packaged in it. It can be seen in figure 4.26 how the intraocular lens can be fixed onto the iris. Figure 4.27 and figure 4.28 show the fabrication process of the entire device and how each individual component is assembled together.

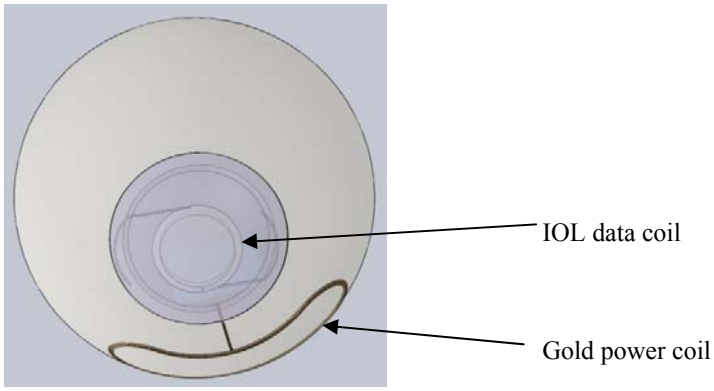


Figure 4.23. Design of the part intraocular, part extraocular model. The gold wire sits outside the eyeball while the rest of the systems are implanted inside.

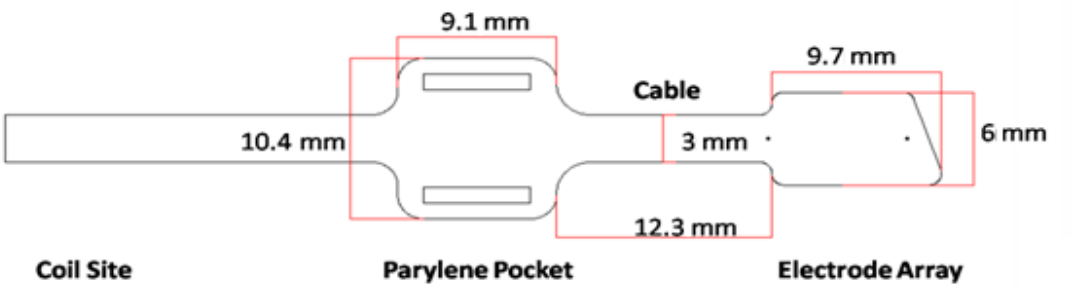


Figure 4.24. Prototype geometry for a part intraocular, part extraocular parylene-based device with all required component regions for a completely implantable system.

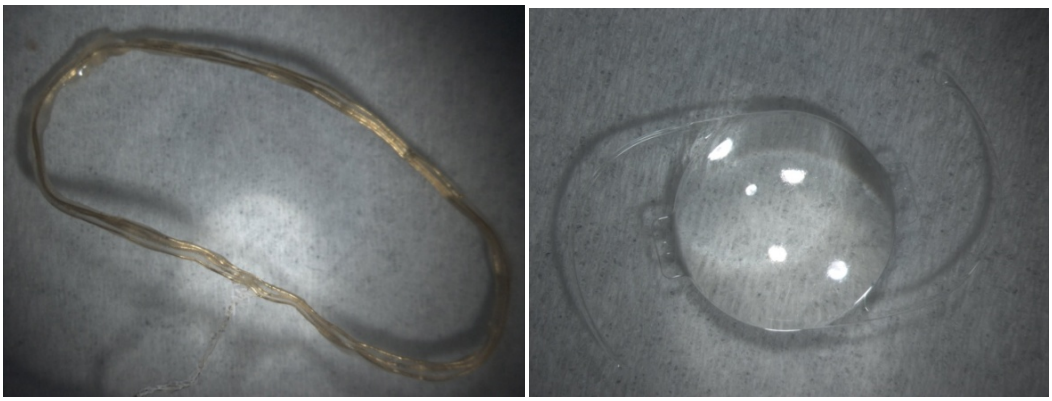


Figure 4.25. (left) The power coil made from gold wires; (right) the intraocular lens acting as data coil in this mechanical model.

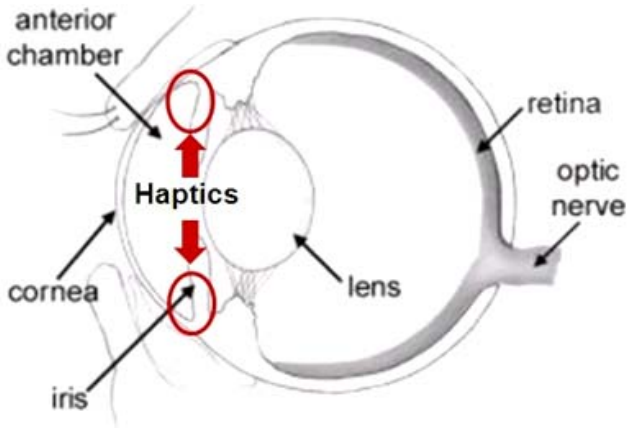


Figure 4.26. Example of a coil with intraocular coil haptics attached.

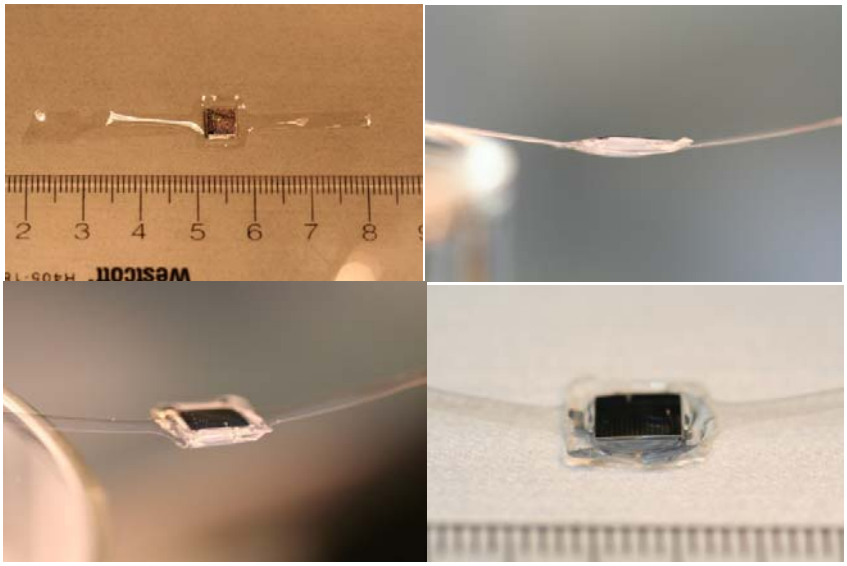


Figure 4.27. Chip packaging in parylene pocket in mechanical implantation model; (top left) parylene sheet before assembly with chip inserted; (top right) thickness of the chip section is approximately 1.6 mm; (bottom left) parylene pocket after biocompatible silicone coating; (bottom right) the parylene pocket after curing and annealing.

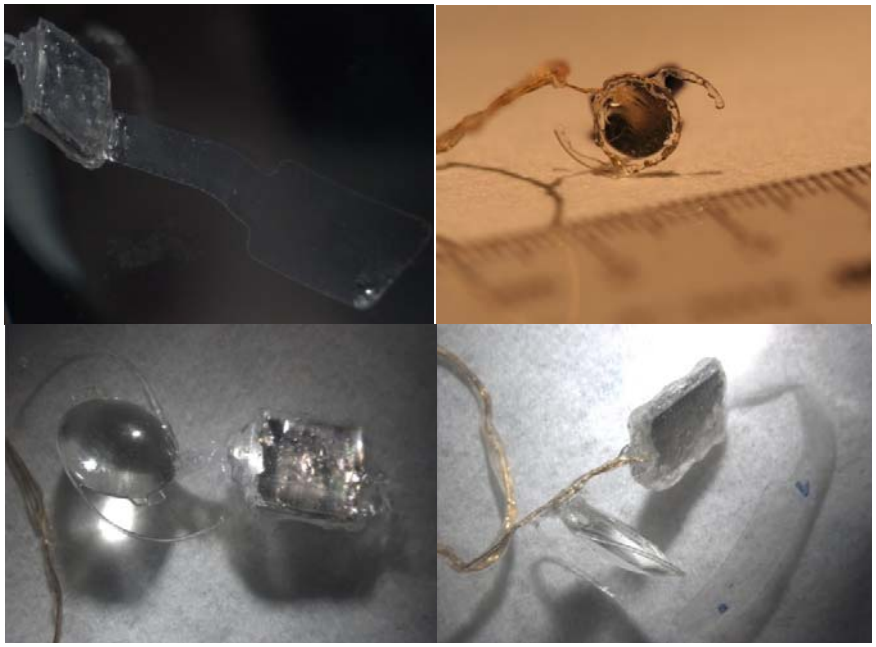


Figure 4.28. Assembled devices; (top left) the parylene electrode area; (top right) the intraocular lens acting as the data coil; (bottom left) the intraocular lens with the packaged chip structure; (bottom right) the entire device consist of a gold wire power coil, an intraocular lens as data coil, a parylene pocket with chip and a parylene electrode sheet.

This model was fabricated and tested for *in vivo* implantation at the Keck School of Medicine of the University of Southern California. First, an incision approximately 10 to 11 mm long is cut in the cornea. The lens is then extracted using phacoemulsification. The chip and array parts are then inserted into the posterior chamber through both holes in the lens capsule, leaving the coil part anchored in front of the iris. Vitrectomy is performed through the sclera ports, and the array part is tacked in place on the retina (figure 4.29). Finally, the cornea and the sclera ports are sutured closed, figure 4.30 gives examples of intraoperative surgical photographs and figure 4.31 shows the post surgery dissection of the eyeball.

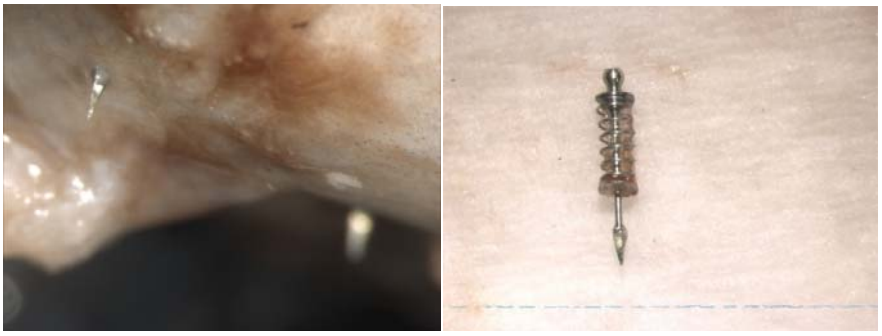


Figure 4.29. Retinal tack used for attaching the parylene electrode sheet onto the retina surface; (left) view from outside of the eyeball. One can clearly see the tacks coming out; (right) retinal tack.

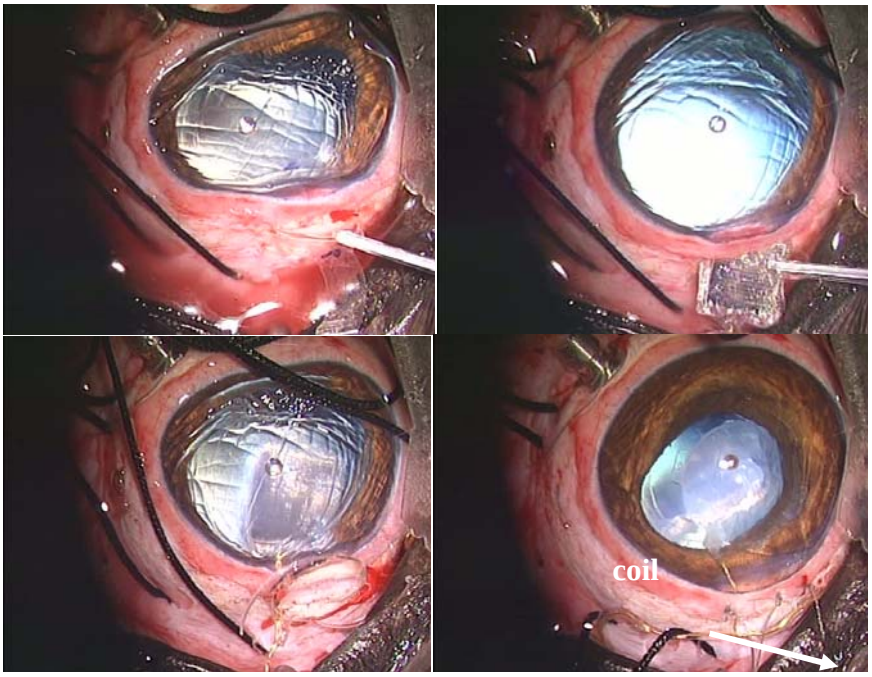


Figure 4.30. Intraoperative surgical photographs; (top left) the parylene electrode area being inserted into the opening; (top right) the parylene pocket with chip being inserted into the opening; (bottom left) the intraocular lens being inserted; (bottom right) the opening being sutured, leaving the gold wire power coil outside.

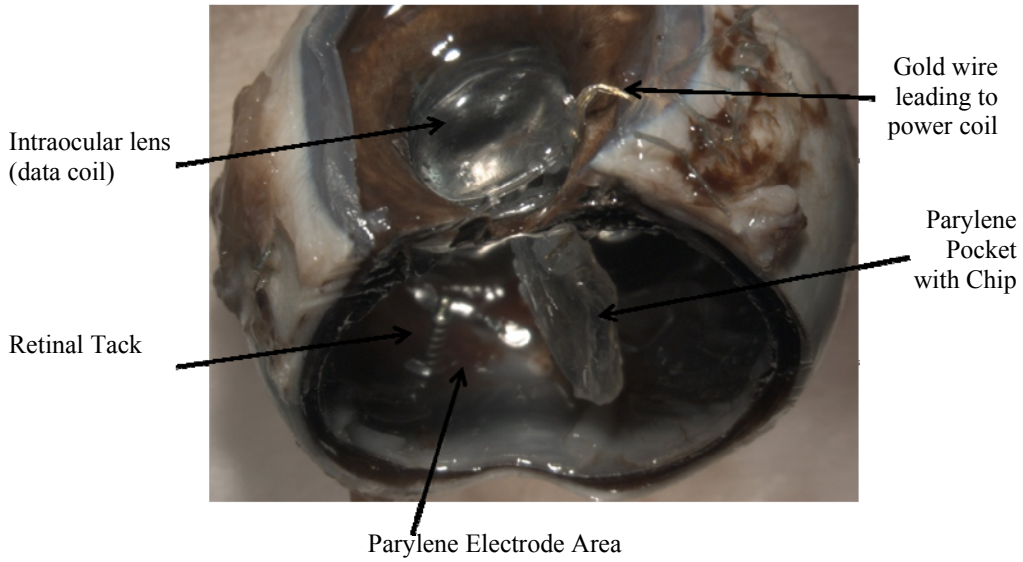


Figure 4.31. Postsurgery dissection of the eyeball.

Future work is underway to (1) implant another design with different points of contact on the data coil to create a better orientation for the array and to facilitate the tacking of the array onto the retina behind the intraocular coil and (2) evaluate the model

in vivo in a chronic implantation test to determine the stability of the design as well as needs for mechanical weight support of the ASIC chips.

4.4.3 Discussion

Human beings have more than 2 million cells in the retina responsible for light detection and eye sight, and it would take from 800 to more than 1,000 electrodes to stimulate them so the resolution can be minimally sufficient for patients to read large print and to recognize facial features. However, the device that will eventually be utilized will all be powered and controlled by the 6 mm × 6 mm × 2 mm box that is integrated with this model and requires at least 45 mW of power [149]. This higher power requirement, combined with movement of the device in the eye and the challenge in making a dense electrode device will make it difficult to implement wireless power.

There are more direct alternatives for providing power for this retinal prosthetic system such as wired transmission. However, possible irritations and intraocular pressure stability become challenges that could potentially render this approach unrealistic. If a wired approach is realized, the site of incision must be watertight but the box of electronics and array must pass through it, extra care and anti-inflammatory precautions must be taken to prevent any possible infections and biological complications. In all, it is still believed that a wired system is a viable option for providing the one thousand electrode array and box of electronics with a power source if all the challenges can be overcome.

4.5 Conclusion

Early in this chapter, several techniques for adhesion enhancement between parylene C and silicon substrate were introduced and investigated. It is found that

annealing at 200ºC increases the undercut rate when the samples are soaked in saline and reduces the adhesion during the partial film peeling test. Molten adhesion, in which only a thin molten layer is used, serves as an excellent alternative for the traditional A-174 and anchoring treatment for its long-term stability, low thermal budget and ease of use. Although parylene does not have a permanent adhesion on silicon even after the enhancement, these results still greatly facilitate our development in parylene pocket IC integration and other bioimplantable devices.

A study on the sealing capability of silicone and parylene were conducted in the second part of this chapter. From the result, one can clearly see that coating with parylene and biocompatible silicone greatly increases the mean time to failure of IC chips and encapsulated components. Active experiments show that devices packaged with both of these treatments are able to survive in 110ºC saline solution for more than a month. This result translates to 7+ years of lifetime in body temperature.

Finally, a novel geometry for a part-intraocular, part-extraocular system has been devised and surgically tested, giving preliminary evidence that it is possible to introduce and anchor the components of the full monolithic device in the target regions of the eye in such a way that the relevant parts are either implanted into or fixed onto the eye.

5 HIGH DENSITY CHIP INTEGRATION

5.1 Introduction

Much effort has been put into developing multielectrode arrays for retinal prosthetic applications. Current state-of-the-art technology is able to achieve 1,024 electrodes on a 1 cm × 1 cm substrate [124, 150]. However, the actual retinal prosthetic systems that are currently in use lack the high density control capability and have the number of channels significantly less than that. These systems also suffer from complicated IC integration schemes or depend heavily on process variables [67, 151]. To be able to match the gap between the number of functional electrodes and the number of electrodes that can be fabricated, and to overcome these challenges and to accommodate the increasing number of retinal prosthetic chips [152], we utilizes the parylene pocket technology and develop a novel integration scheme that will allow us to connect more than 280 bonding pads on an area less than 5 mm × 5 mm with high efficiency. As described in previous chapters, this packaging technique can also house any IC chip or discrete component and provide electrical connection to it. The chip that is to be modeled after is developed by Dr. Wentai Liu from University of Santa Cruz and has 256 controllable channels designed to stimulate photoreceptive cells in the retina [153]. In order to illustrate the functionality of this system integration, an intermediate printed circuit board integration approach is taken. It should be noted that, the final implanted device will look like the implanted physical model presented in chapter 4.

On the actual IC chip, the 256 pads (channels) in the center of the chip, as shown in figure 5.1a, send signals to stimulate the cells. The peripheral pads that surround the chip are input voltages, clocks or test outputs that facilitates debugging and troubleshooting. The dimensions of the chip are 5.3 mm × 5.1 mm × 700 μm. A dummy chip that has the exact same layout of the actual chip is fabricated (shown in figure 5.1b). The printer circuit board approach is also illustrated in figure 5.2. In the figure, the PCB acts as the substrate and the intermediate platform to connect to testing equipments and external circuits and controls. The bonding pads are grouped in terms of functionality such as test connections, discrete components, controls and outputs.

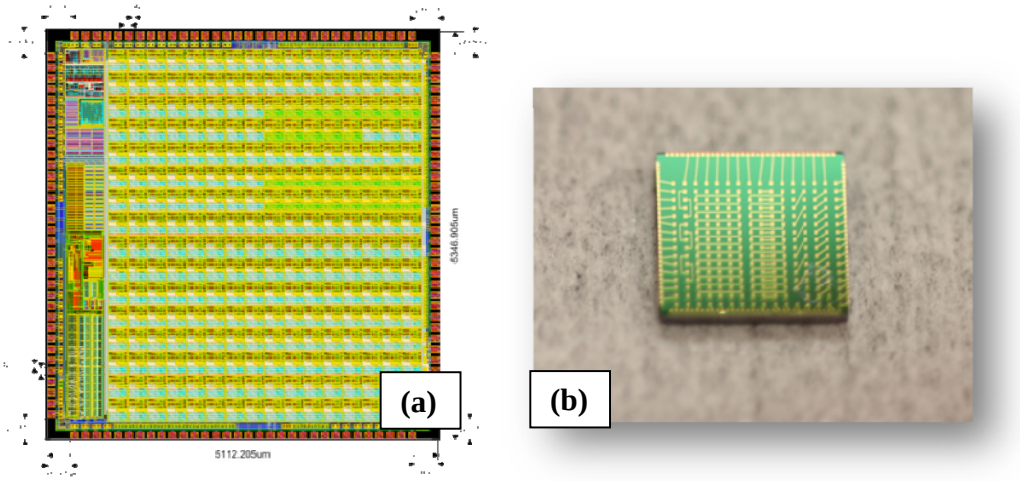


Figure 5.1. (a) Layout of 256-channel stimulation chip from UC Santa Cruz. The pad size is 100 μm × 100 μm. There are about 120 functional peripheral pads on the edge of the chip; (b) dummy chip with conductive traces is fabricated to emulate the actual chip.

The main purpose of this platform is to access the pads on the chip so the users can both control and observe the output. Because the bonding pads on the chip are very small (100 μm × 100 μm), in order to monitor individual channels on a macro scale using probe stations and to enable future integration for *in vivo* experiments, a special bonding technique has to be developed to enable the electrical connective capability of this parylene pocket platform to the chip.

The parylene film platform first provides the connection from the pad on the chip to the pad array located on the same parylene film. These pad arrays are going to be connected to the bonding pads on the PCB on the corresponding locations, which are further routed to the connectors to allow access for the users. The circle on the left side of the figure represents the wireless RF inductor for power and data transfer, which is going to be connected after integration.

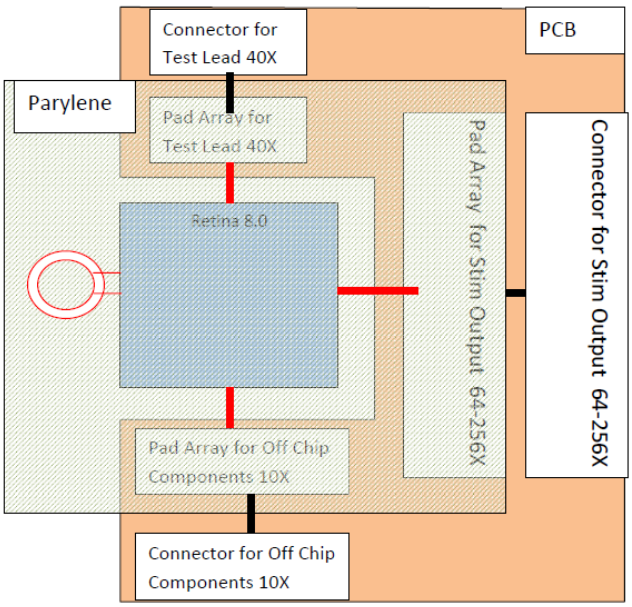


Figure 5.2. Printed circuit board integration approach with parylene pocket platform for retinal prosthetic prototype testing.

5.2 Parylene Pocket on Silicon Substrate

5.2.1 Fabrication

The parylene pocket structure is fabricated with a combination of RIE and DRIE processes (figure 5.3) and is similar to that of the parylene-cabled silicon with pocket [138]. After the fabrication process, the devices are released from the wafer. An IC chip is then inserted by hand into the parylene pocket, aligned, bonded and tested. It is then totally coated with parylene and silicone for overall biocompatibility.

The mask layout for this device is shown in figure 5.4. The squares on the perimeter of the structure are for bonding epoxy to go through to mechanically fix the parylene platform onto the PCB (figure 5.5). The dense lines are the metal trace lines, and there are parylene openings exposing the metal underneath for all the metal pads. Due to the thickness of the chip (700 μm), it takes a large real estate on the device to accommodate the "pocket" that can house the chip. This results in a big empty space in the middle of the device. The PCB is fabricated commercially and contains bonding pads that are to be bonded with the bonding pads on the parylene platform via conductive epoxy by hand.

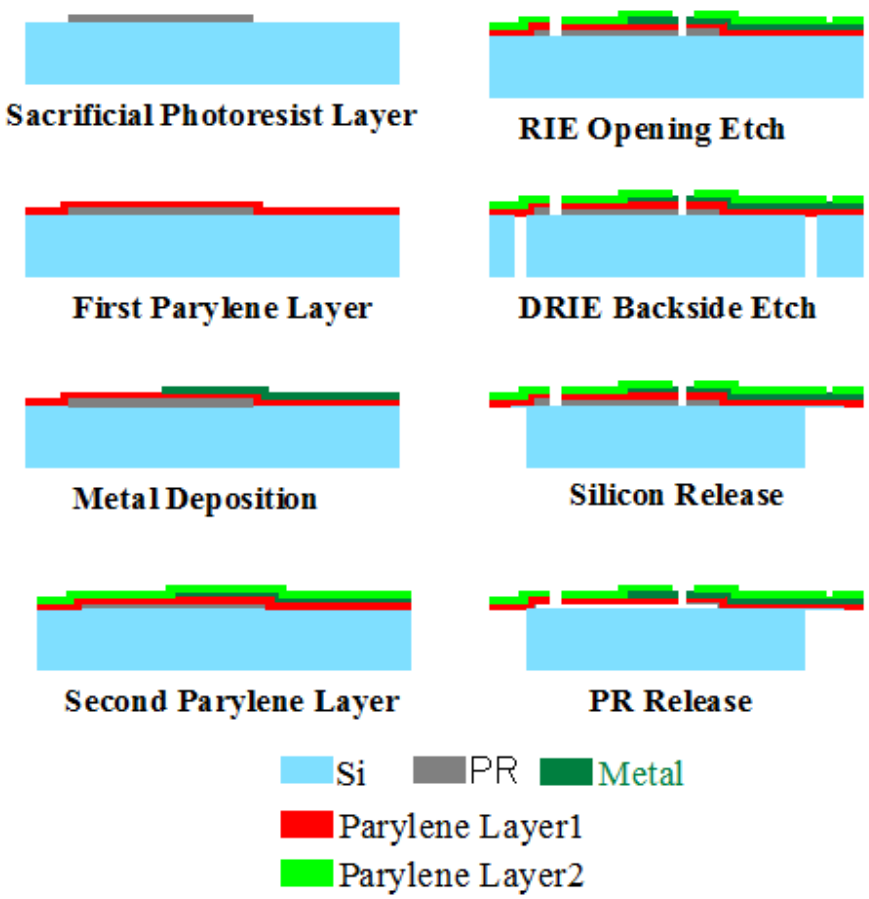


Figure 5.3. Process step for the parylene pocket platform on silicon substrate.

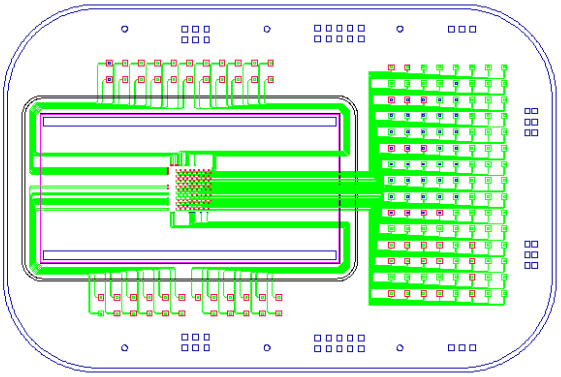


Figure 5.4. Layout of the parylene pocket on silicon substrate platform.

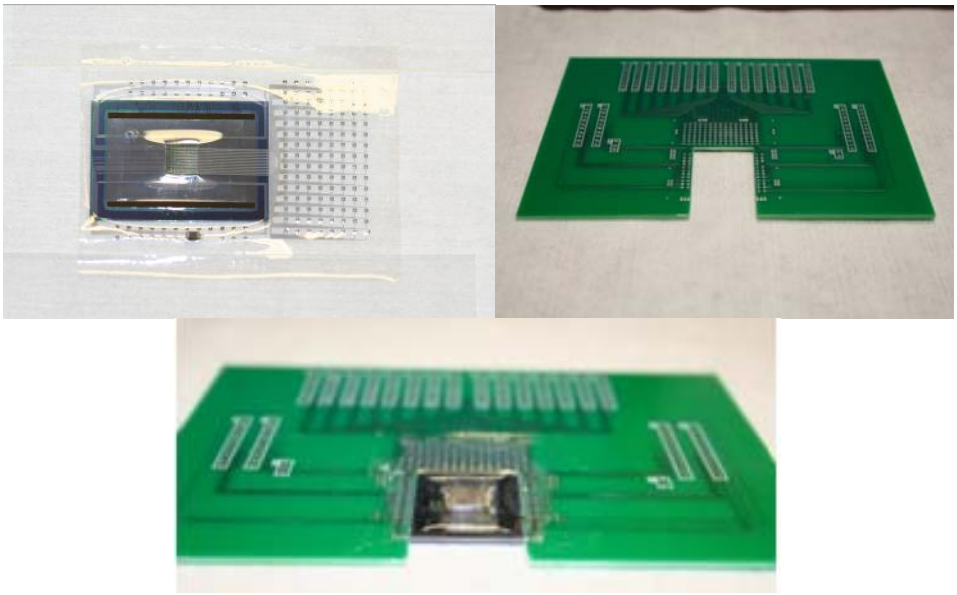


Figure 5.5. (top left) Fabricated parylene pocket platform with silicon substrate with chip integrated; (top right) printed circuit board to accommodate the parylene pocket platform; (bottom) complete integrated and bonded device.

5.2.2 Fabrication Challenges

5.2.2.1 Lift-off Metal Patterning

Due to the limit on the size of the pocket and the number of connections that needs to be made (figure 5.6), line width of 5 μm with 5 μm pitch needs to be achieved. The standard metal line etching process, however, is greatly affected by the isotropic etching time and the metal etching solution. This means thin metal lines are very easily

etched away, and the maximum achievable resolution becomes difficult to control. Shown in figure 5.7, the chrome layer underneath the gold lines has been etched away, resulting in floating, unusable traces.

On the other hand, lift-off process is an excellent alternative to metal etching; unlike metal etching process where the metal is deposited before the lithography step, lift-off process requires the lithography step to be taken before the metal deposition so the metal can be deposited in the "trenches" to achieve very high resolution metal lines. A detailed fabrication step of lift-off lithography is illustrated in figure 5.8.

In addition to the regular photoresist used in the standard lithography process, a special photoresist for lift-off purposes; lift-off Resist (LOR), has been developed by Microchem Corp. (Newton, MA, USA). The development rate of this photoresist can be controlled by the softbake temperature and time. This means one can tune the lithography development step so that the LOR resist develops slightly faster than the standard photoresist.

In the actual lift-off process, the LOR is first spun on the substrate at 3,000 rpm for 40 seconds and softbaked for 15 minutes at 140ºC, followed by a layer of AZ 1518 photoresist spun at 3,000 rpm for 40 seconds for 30 minutes at 100ºC to achieve a 0.3 μm + 1 μm dual layer photoresist structure to make the pattern for the metal lines. Because of the difference in development time, LOR develops isotropically and creates a "bilayer reentrant" structure, which is known as the "undercut," as shown in figure 5.9. The undercut structure provides a very clear edge to the patterned metal lines, but requires very delicate developing process to ensure perfect geometry. As an example, the wafer is first immersed in the developer solution, after UV exposure, for 30 seconds before

visually inspection under a microscope. This step will be followed by 5 seconds of additional developing before the visual inspection step again, which is followed by another 5 seconds of additional development. This step would repeat itself until an undercut structure can be seen clearly. Figure 5.10 shows the gold lines patterned by lift-off process with 5 μm resolution.

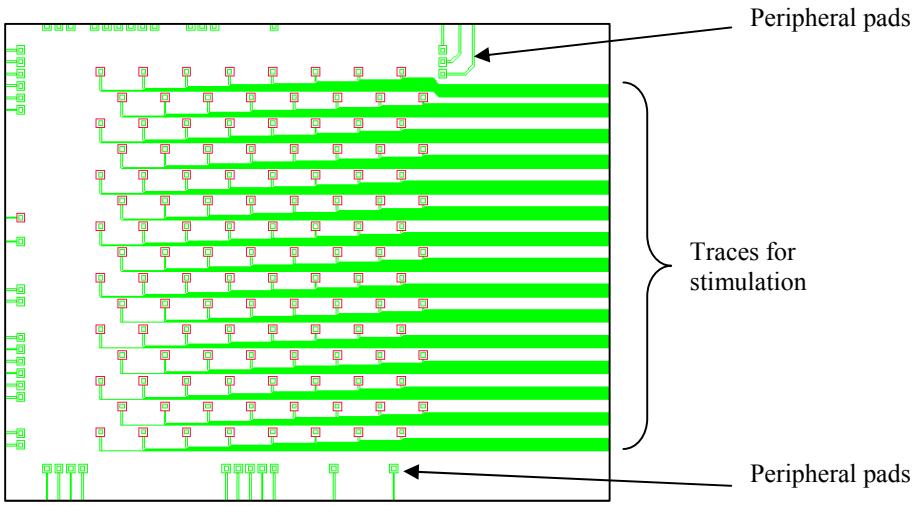


Figure 5.6. Close-up figure of the layout of the traces near the bonding pads for the chips. Due to the location of the peripheral pads, the traces for stimulation are limited to the middle.

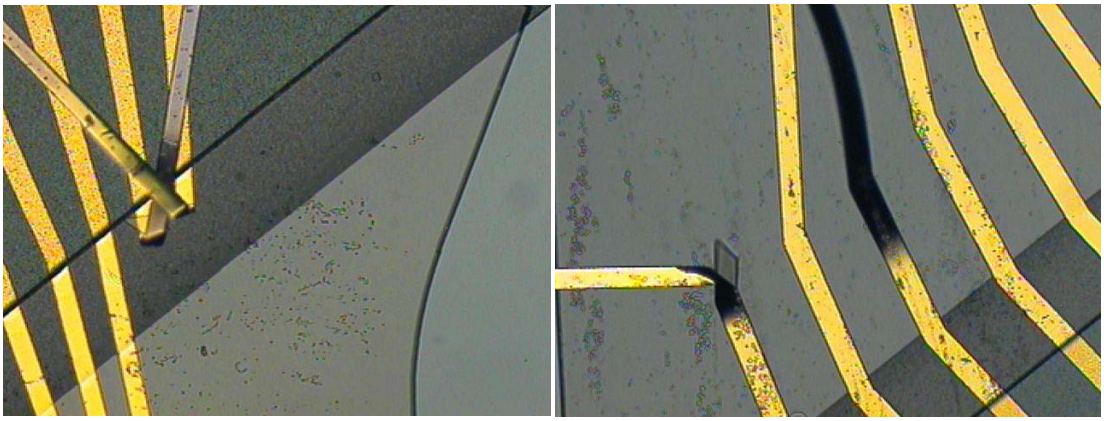


Figure 5.7. Detached gold lines after the underlying chrome has been etched away due to isotropic undercut etching.

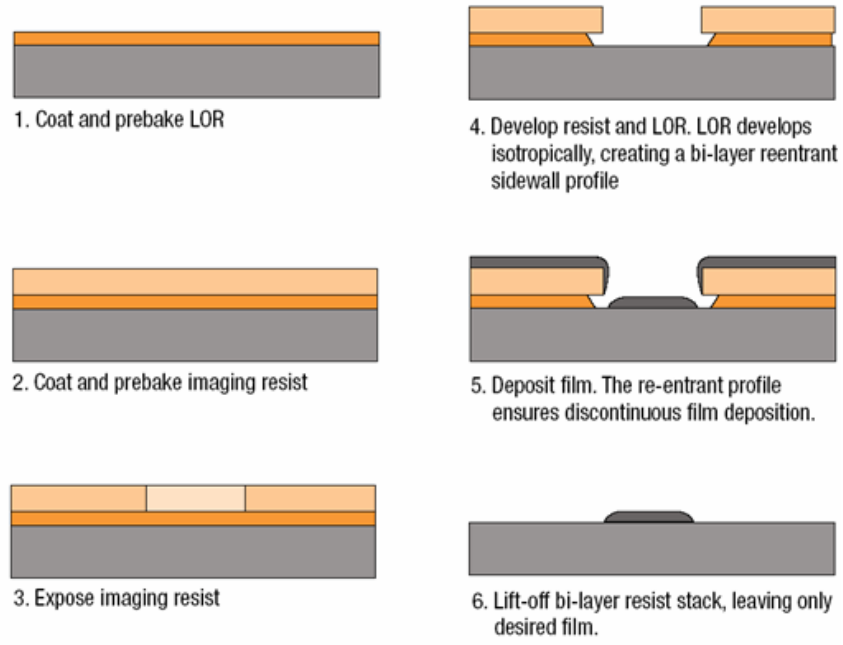


Figure 5.8. Lift-off lithography steps.

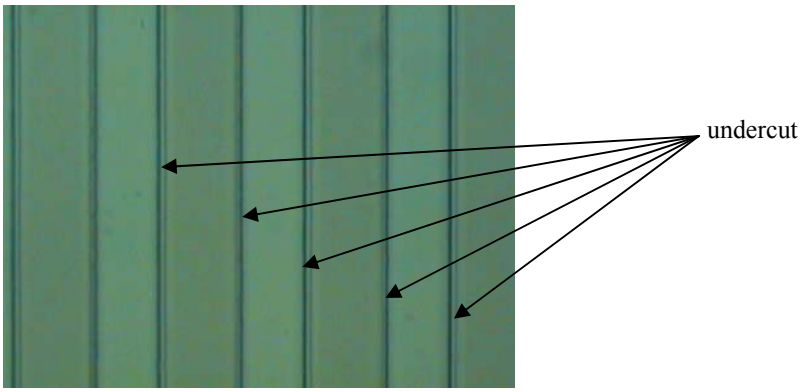


Figure 5.9. Lift-off photoresist after development; the undercut (white strips) can clearly be seen on the edges of the photoresist lines.

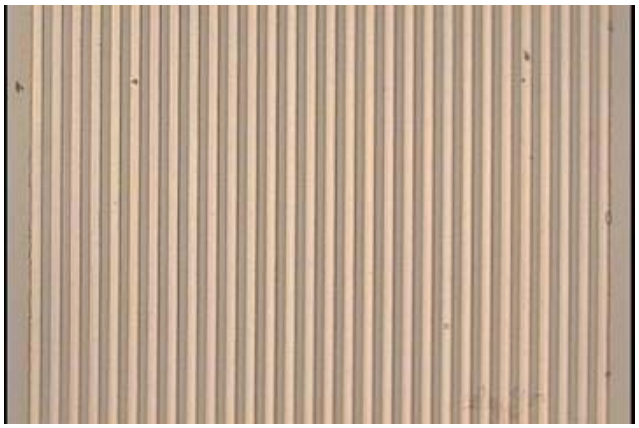


Figure 5.10. Figure of the trace lines after metal deposition and lift-off resist release.

5.2.2.2 Thick Photoresist for Plasma Etching

The main function of the thick photoresist layer is to act as a mask when etching parylene using RIE with O_2 plasma. The structure that is to be fabricated has three parylene layers, including the parylene substrate (5 μm), bottom parylene layer (5 μm) and the top parylene layer (5 μm), which accounts for approximately 15–20 μm of parylene that needs to be etched away in the end to define the device perimeter. Given the etching ratio of parylene and photoresist in the RIE machine to be approximately 1:1.1–1.2, the thickness of the photoresist needs to be at least 25–30 μm in order to prevent damage on the top parylene layer.

As a result, a thick photoresist (>30 μm) with high resolution is needed. AZ 9260, a high resolution thick photoresist, is used for this purpose. It provides high resolution with superior aspect ratios, as well as wide focus and exposure latitude and good sidewall profiles. A dual layer AZ 9260 layer is realized to achieve the desired thickness. The first layer photoresist is spun on the substrate at 800 rpm for 40 seconds and softbaked at 100ºC for 5 minutes before spinning another layer of photoresist on top at 800 rpm for 40 seconds and soft-baking at 100ºC for 30 minutes. The wafer is then naturally cooled by setting the oven to room temperature to alleviate any thermal stress that may be induced during abrupt temperature changes, which may create cracks in the photoresist that cannot be repaired. The wafer is then left in room temperature to set for 24 hours before UV lithography exposure and development.

Due to the delicate nature of the thick photoresist layer, extra care needs to be taken during the RIE etching step as well. A microinterval etching step is often followed to minimize any thermal stress that may occur during the etching process. For example,

the wafer may be exposed to the plasma for 1 minute etching before pausing and cooling down. This process continues until the entire parylene layer is cleared away. It is found, however, that this process is still not 100% reliable and needs additional rendering in the next design iteration.

Thus, for practical use, thinner photoresist layers are generally used in order to avoid the cracks completely. In this case, first layer of photoresist is deposited for the etching of fraction of the parylene. A second layer is deposited just before the first layer of photoresist is used up. This process repeats itself until the targeted parylene layer has been etched through. It is a much safer way to etch a thick layer of parylene, but it is more time consuming, and the structure may be contaminated by the multiple wet development steps.

5.2.2.3 Parylene Cracking

Parylene is a biocompatible layer that is being widely used for insulation and substrate for numerous biomedical applications. It still, however, suffers from failure due to nonuniform stress during fabrication processes due to thermal and assembly steps. Electron beam evaporation is one of the most dominant thermal steps that the parylene is exposed to and can induce cracks and defects in the parylene film. This may have catastrophic effect on the functionality of the device.

It has been shown that cracks were induced in parylene during platinum but not during gold deposition steps. Thermal tags were placed on the back of process wafers to measure the maximum temperature achieved during the electron beam evaporation process. Results show that wafers from gold deposition reaches 70–80ºC and wafers from

platinum deposition reach more than 126ºC during depositions. Hairline cracks can be clearly seen after the lift-off step, as shown in figure 5.11 and figure 5.12.

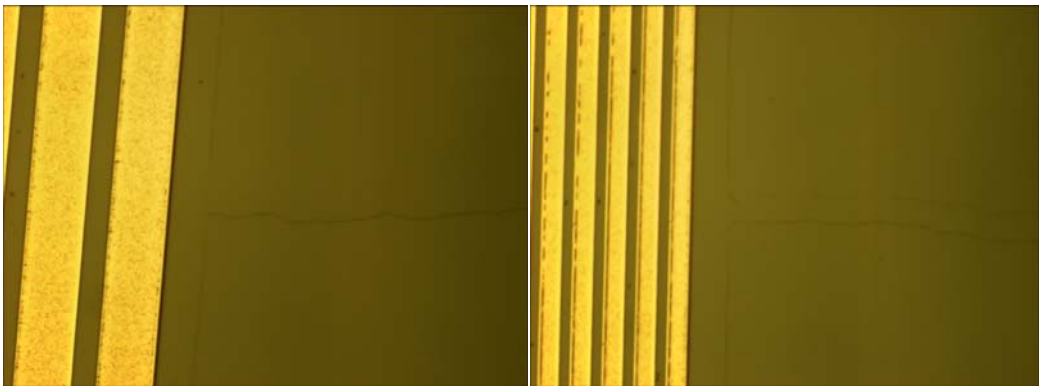


Figure 5.11. Parylene cracks can be clearly seen on the empty areas on the right hand side of both figures.

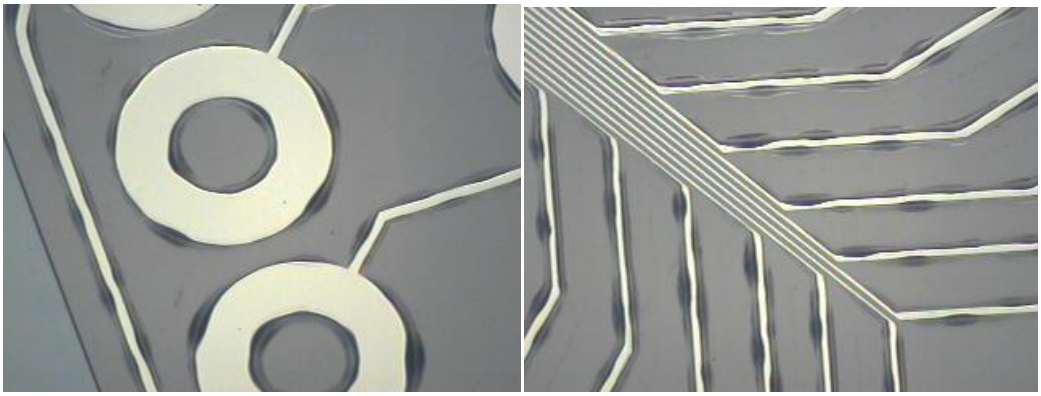


Figure 5.12. Parylene cracks occur on the edges of the metal lines; resulting in solution attack and causes delamination.

The process steps were scrutinized up to this point to determine the exact cause of this problem. The following recipe was found to most effectively eliminate the occurrence of thermal cracks during metal depositions. Starting with a wafer with parylene substrate to be deposited with platinum metal traces:

1. Lift-off resist spin 3,000 rpm for 40 seconds
2. Hotplate softbake at 140ºC for 15 minutes
3. AZ 1518 resist spin 3,000 rpm for 40 seconds
4. Oven air softbake at 100ºC for 30 minutes
5. Lithography–UV light exposure
6. Development until undercut
7. Hardbake at 120ºC for 30 minutes

8. Descum with O_2 plasma for 1 minute at 250 mT with 200 W power
9. Deposit platinum metal 500 Å+ 500 Å + 500 Å + 500 Å with 30 minute rest in between
10. Put machine in standby for 2 hours
11. Vent machine and wait for 30 minutes
12. Lift-off in warm photoresist stripper and acetone.

The photoresist needs to be hardbaked before the e-beam deposition. This step cannot be too long; otherwise the oxidation effect of parylene would dominate during the bake and causes the polymer to crack. The platinum metal is deposited in multiple intervals to reduce the thermal stress induced at any given interval and also to allow the heat to be dissipated away from the wafer. In the end, the machine is put in standby and vented for an extended period of time to gradually let air into the chamber without creating a huge thermal gradient that may further induce cracks in the polymer layer. It should be noted that the photoresist stripper and acetone should be heated with the wafer to eliminate any huge temperature changes. Applying this recipe successfully eliminated the cracks that occurred in the original process.

5.2.2.4 Metal Line over a Step

The sacrificial layer is a crucial step in creating a cavity for the parylene pocket to allow insertion of the integrated circuit chip. The thickness of this layer depends on the type of material used and can range from hundreds of nanometers to several micrometers. Since metal lines need to connect the pads on the IC chip that resides within the pocket area to circuits outside, these lines unavoidably have to go across a vertical height difference (shown in figure 5.13 and figure 5.14) created by these sacrificial layers. As the thickness of the chip increases, the thickness of the sacrificial layer also needs to be increased. This increase may cause discontinuity of the metal lines. An experiment on the

typical sacrificial layer material and heights is thus conducted to study the tolerance of the vertical height allowed for the sacrificial layer. The result is presented in table 5.1, which shows the type of photoresist one should use when creating structure such as this.

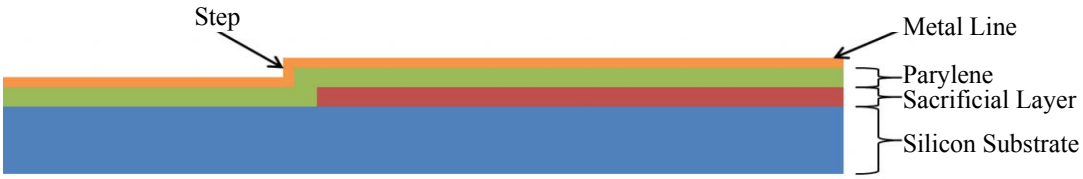


Figure 5.13. Figure of metal line going over a step.

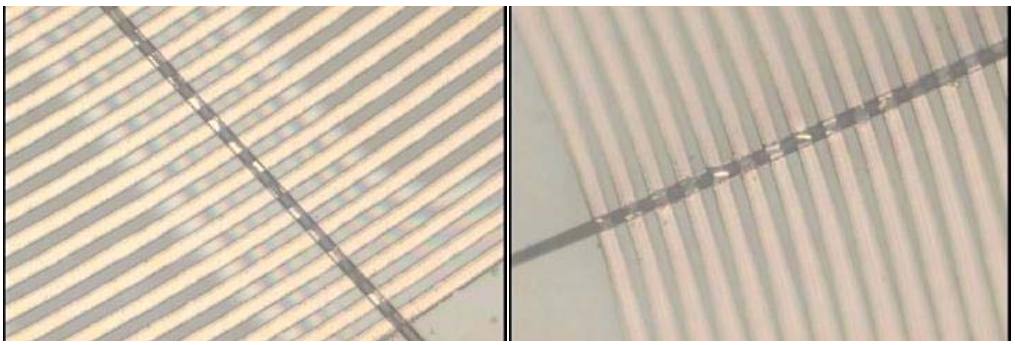


Figure 5.14. Microscope view of the metal line going over a step.

Table 5.1. Step height effect on metal continuity.

Material	Deposition Method	Thickness	Metal conductivity
Aluminum	Thermal Evaporator	2,000 Å	Good
AZ 1518	7,000 rpm spin for 40 seconds	~1 µm	Good
AZ 4400	4,000 rpm spin for 40 seconds	~4 µm	Good
AZ 4620	1,000 rpm spin for 40 seconds	~15 µm	Broken
AZ 9260	1,000 rpm spin for 40 seconds	~16 µm	Broken

5.2.2.5 Pocket Size

In order for the parylene pocket to accommodate a thick IC chip substrate underneath, the structure relies on the mechanical property of the parylene film. It is not reasonable to deposit a 700 µm sacrificial photoresist layer to house the chip, nor is it efficient to etch through the wafer to utilize the technique from Li et al. [67], because the

vertical height between the surface of the chip and the surface of the silicon substrate is still very large. Thus, if a silicon substrate must be used, the area of the sacrificial layer must be increased to give more stress relief to the film to be "stretched" upwards to house the chip. However, from experiment, it takes about 3 cm × 1.5 cm of real estate on the wafer to house a 5 mm × 5 mm × 700 μm chip. Not only has the throughput of the fabrication gone down, the size of the device also has become impossible to implant into an eyeball. A new approach must be taken to overcome this challenge and to enable the implantability and the fabricability of the device.

The parylene pocket on parylene substrate has thus become the ideal candidate for this application. The entire structure is flexible and does not require an additional solid silicon substrate. It is easier to implant and can house extremely thick IC substrates.

5.3 Parylene Pocket on Parylene Substrate

As mentioned in the previous section, the parylene pocket substrate size becomes a big issue when an IC chip with thick substrate is to be integrated with this technology. The thickness makes it impractical to fabricate a device with silicon substrate that is excessive in dimension due to the size of the stress relief that needs to be considered in the design. Thus, parylene pocket on parylene substrate needs to be incorporated in the design to allow more flexible and more accommodating housing for the chip. Its fabrication process (shown in figure 5.15) is exactly the same as what was described in the previous chapter. The process describes a parylene-metal-parylene sandwich layer that is deposited on top of a parylene substrate with a photoresist layer in the middle to define the cavity to house the chip.

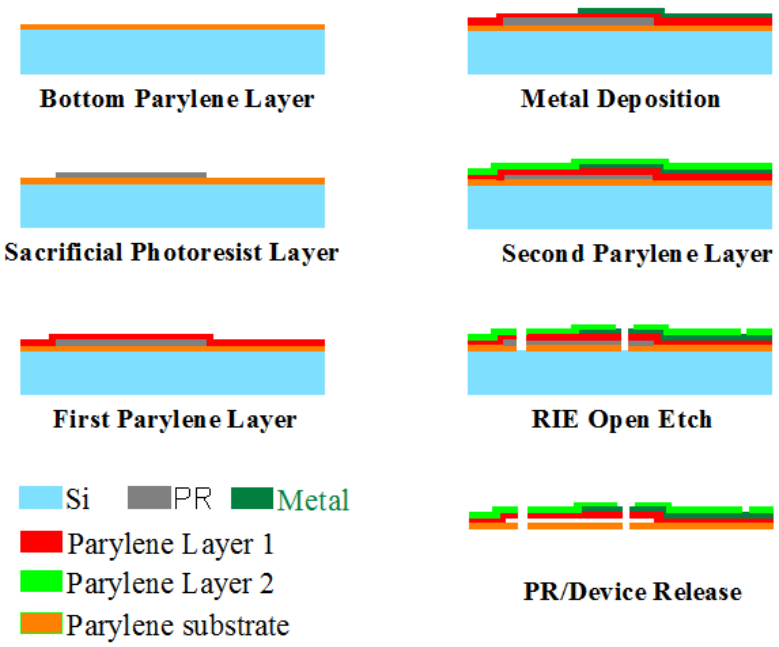


Figure 5.15. Process steps for the parylene pocket on parylene substrate.

It can be seen in the new layout design figure (shown in figure 5.16) that the area allocated for the sacrificial layer is much smaller (1 cm × 1.03 cm) compared to that of the pocket design with silicon substrate (3 cm × 1.5 cm). The dimensions of the overall platform and the surrounding pads and connecting pads remain the same as the previous version. The number of channels, however, has been almost doubled in this second design and the width of the wiring traces have been reduced from 10 µm with 10 µm pitch to 5 µm with 5 µm pitch.

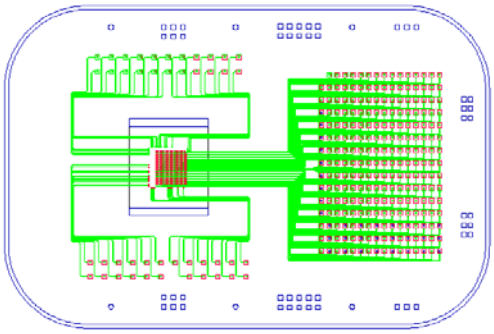


Figure 5.16. Mask layout for the parylene pocket platform on parylene substrate. Note the area for the pocket is much smaller compared to the pocket platform on silicon substrate.

Figure 5.17a shows the fabricated parylene pocket on parylene substrate with the chip inserted before bonding. It is 15 µm thick (3 parylene layers with 5 µm each) and is 6 cm in length and 4 cm in width. It is clearly seen that the overall structure is less stressed than the parylene pocket on silicon substrate and the pocket has ample space for components to be inserted (figure 5.17b).

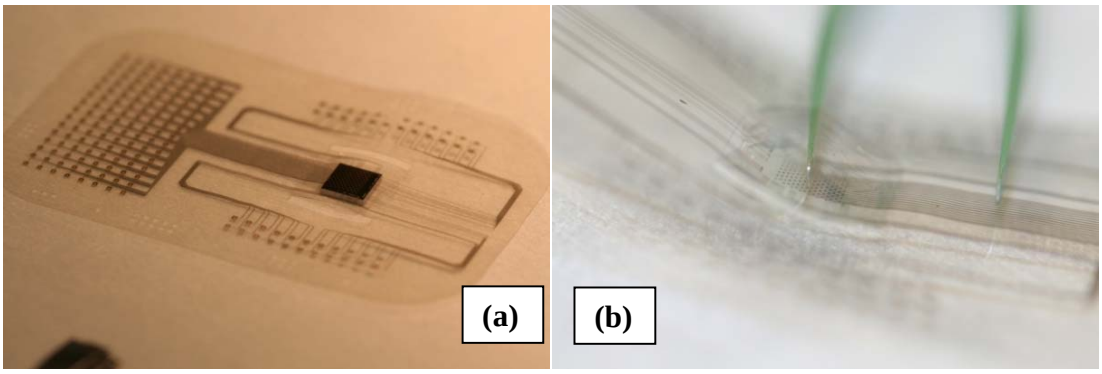


Figure 5.17. (a) Fabricated parylene pocket platform with IC chip integrated and bonded; (b) the parylene pocket structure

5.3.1 High Density Integration

5.3.1.1 Alignment

Because the pocket is now free of a rigid substrate and the IC chip has more freedom to move around in the pocket, the alignment of the chip in the pocket during integration becomes more difficult. Gel-pak is again used in this process to facilitate the alignment and the bonding process. The chip is first inserted into the pocket. The entire device is then placed on this sticky surface so the parylene film is fixed in place. Super glue may be used to assist the fixation of the chip in the pocket after careful alignment. Resolution of approximately 10 µm to 20 µm (as shown in figure 5.18) can be achieved with this process. A more robust protocol needs to be developed to increase the repeatability of this process.

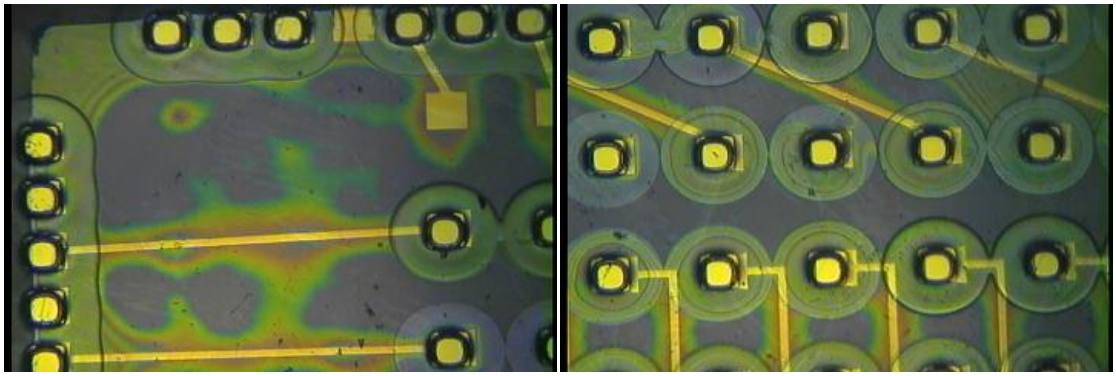


Figure 5.18. Alignment of the pocket bonding pads with the metals pads on the chip. Resolution of 10 μm to 20 μm can be achieved.

5.3.1.2 Squeegee Technique

The next step of the integration process is to connect each pad on the chip with the bonding pad on the pocket to achieve functionality. Several models of the integration, such as muscle stimulator and RFID chips were presented in previous chapters. These IC chips had 2 to 5 bonding pads with some discrete components; connecting the chips to the parylene pocket only required manual painting of the conducting epoxy because the number of metal pads is small and the pads are far away from each other. However, the chip that is to be integrated in this section has a very dense array. The average pad size is 100 μm and are placed 40 μm away from each other (140 μm pitch), and it is impractical and extremely difficult to connect everything manually. With the development of a fully automated process machine in mind, we present here an intermediate solution that is able to globally bond a large number of pads with the pads on the parylene pocket. In this process, an epoxy squeegee setup is used. A commercially available conductive epoxy (118-15A/B, Creative Materials, Tyngsboro, MA, CA) is first mixed and applied on the surface of the edge of the parylene film. The parylene film has holes and wells that were etched during the fabrication process. These holes and wells act as the screen for this squeegee process after they are aligned to the bonding pad of the chip underneath. A

rubber squeegee is then used to push the epoxy across surface (figure 5.19), so the epoxy fills the wells in the parylene film, and electrically connecting the electrical traces that are embedded inside the parylene film and the bonding pads on the chip together.

Extra care must be taken while mixing the epoxy; since low viscosity epoxy would cause epoxy overflow underneath the parylene film and short circuit on nearby circuit. High viscosity epoxy, on the other hand, would not fill the well or is extremely difficult to remove and would create short circuit defects on top of the parylene film (both illustrated in figure 5.20).

However, this squeegee process with the current fabricated device is not 100% repeatable as the wells on the top parylene layer have low aspect ratio and cannot retain the conductive epoxy. Thus, an additional photoresist lithography step is considered to make this process even more reliable. SU-8, a negative photoresist is used to create a higher well after the device is released from the wafer. The well that is created from this step can retain all of the epoxy that is squeegeed on top of it. A comparison of this process is shown in figure 5.21. An experiment was conducted to determine the optimized aspect ratio for this well after evaluating the bonding efficacy. The results of this experiment are presented in table 5.2. The epoxy footprints with different SU-8 screen openings are presented in figure 5.22. Masks that are 30 μm thick with 60 μm opening produce the cleanest pattern for this technique.

In addition, this SU-8 has very high plasma etching resistance and can be used as a mask to etch through a very thick layer of parylene. This property can also be utilized to eliminate the thick photoresist cracking problem. The only trade-off is that SU-8 is not removable after photolithography patterning.

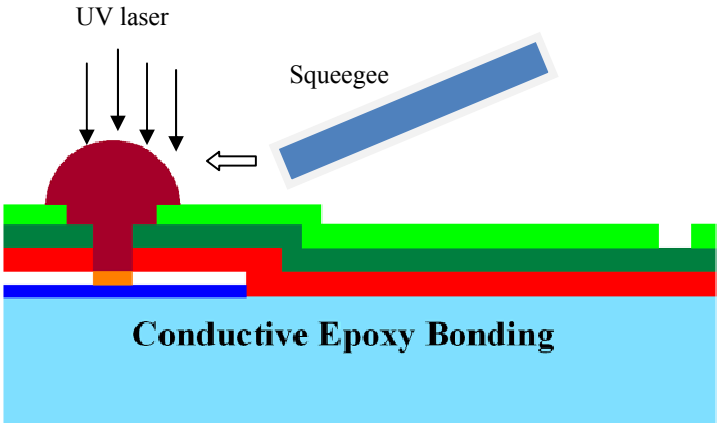


Figure 5.19. The squeegee is used to push the excess conductive epoxy away from the surface; heat is applied to cure the epoxy that remains in the trench to make the connection between the pads of the parylene and the IC chip.

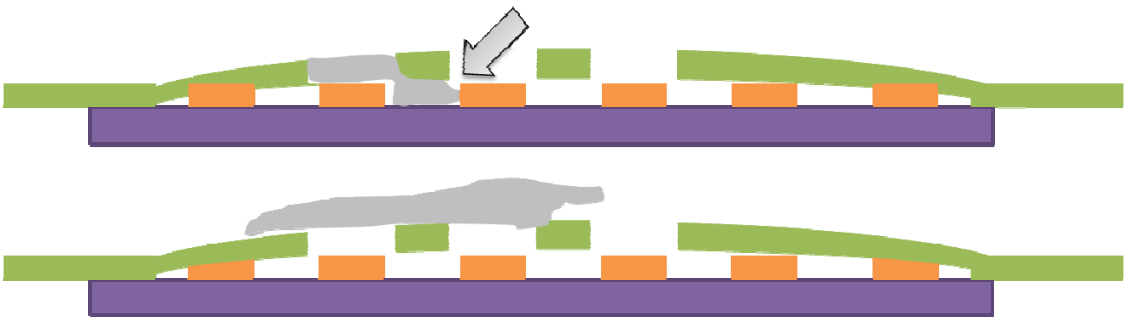


Figure 5.20. (top) The conductive epoxy may short circuit two neighboring metal pads on the chip if the viscosity of the epoxy is too low; (bottom) the conductive epoxy may not provide electrical connection if the viscosity is too high.

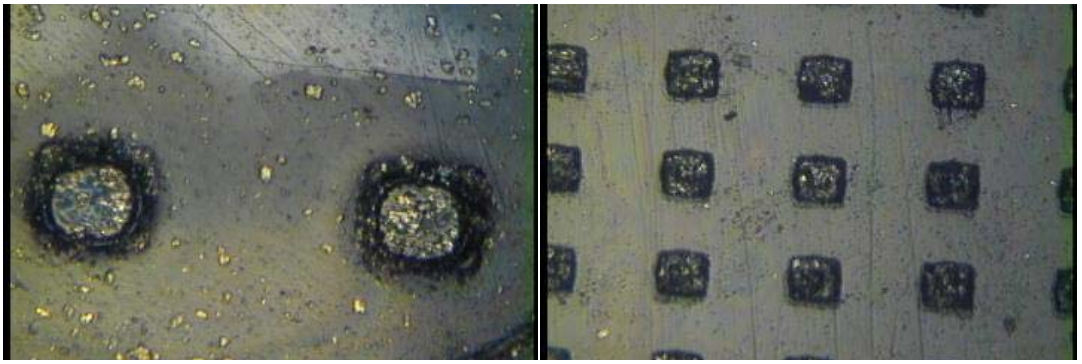


Figure 5.21. (left) The well after the conductive epoxy squeegee process. The well is only 5 microns tall and cannot retain the epoxy, leaving empty spaces in the well. (right) After SU-8 layer application, the wells are completely retained and filled.

Table 5.2. Aspect ratio of conductive epoxy well and its connectivity.

	15 µm thick SU-8	**30 µm thick SU-8**	**50 µm thick SU-8**	**100 µm thick SU-8**
100 µm opening	Epoxy not 100% retained	Epoxy retained; some shortage between pads, flexible film. (figure 5.22a)	Epoxy retained; no shortage between pads. Film becomes stiffer	Epoxy retained; no shortage between pads, some open circuits. Film becomes very stiff.
60 µm opening	Epoxy not 100% retained	Epoxy retained; no shortage between pads, flexible film. (figure 5.22b)	Epoxy retained; no shortage between pads, some open circuits. Film becomes stiffer	Epoxy retained; no shortage between pads, some open circuits. Film becomes very stiff.

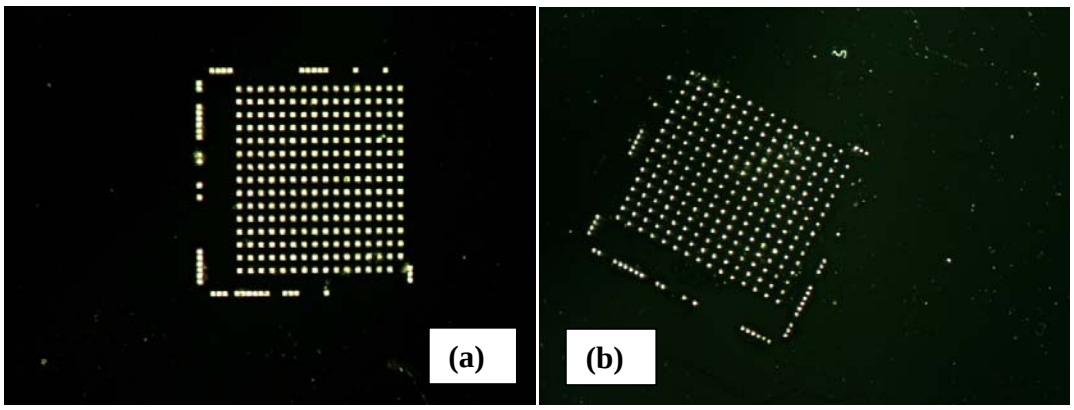


Figure 5.22. The conductive epoxy footprint on a testing substrate after squeegee process. This test is conducted to determine the optimized aspect ratio of the SU-8 well.

After the squeegee process, the conductive epoxy can be cured in two ways; global oven curing and local laser heat curing. In global oven curing, the surface first needs to be cleaned with a very light wipe with acetone to further eliminate shorts and unwanted residues. The entire structure is then placed in the oven at 80ºC for 90 minutes [154] to cure the conductive epoxy. This process is easier, less time consuming and is currently used in our fabrication process. The profile of the bonding epoxy bumps is examined; the maximum height of the applied conductive epoxy is ~25 µm (figure 5.23).

In the second method, ultraviolet pulsed annealing (New Wave Research QuikLaze 50SR Multi-wavelength laser trimming system, New Wave Research, Fremont, CA, USA) can be used to cure the epoxy connections locally. The power of the laser

needs to be tuned so that it is strong enough to cure the epoxy without etching the epoxy wells. The laser system can be automated by programming the software to step through each connection well to anneal. After this annealing, acetone is used to wipe away the uncured conductive epoxy. This step leaves the surface of the bonding pad relatively clean and the space between pads free of unwanted short circuit conductions, as shown in figure 5.24.

Ideally, a UV curable conductive epoxy should be used for this purpose, as the time to cure would be shorter and would make the process more efficient. However, UV curable conductive ink is difficult to make due to reflection of the UV light by the solid fillers inside the epoxy, causing the epoxy resin to not cure properly. Research is being done to develop a reliable UV curable conductive material with secondary reaction [155].

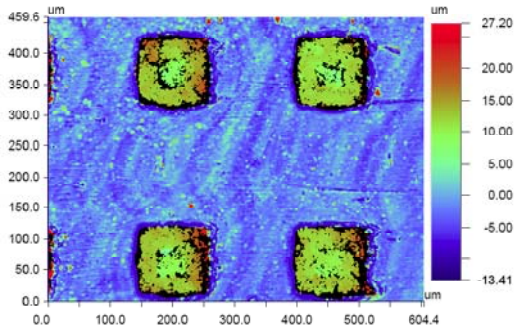


Figure 5.23. The surface profile of the bonded surface. The maximum height of the conductive epoxy bump is about 25 μm

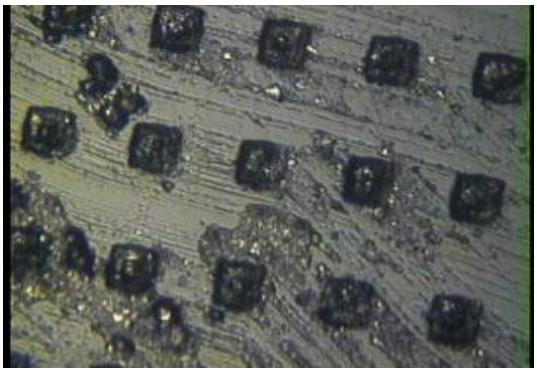


Figure 5.24. The surface of the bonding pads right after the squeegee. There is a significant amount of residue left.

The electrical properties of the conductive epoxy are then measured to determine the additional resistance added during the bonding process. In this experiment, the resistance of the conduction traces on the bare conduction chip is first measured. This resistance is measured again after the squeegee process is applied to determine the resistance of the conductive epoxy. Each epoxy bond adds an average of 3.4 Ω to the circuitry.

5.3.2 Integration Issues

5.3.2.1 Metal Pad on Edge

One of the biggest issues while undertaking the parylene pocket integration process occurs during the squeegee epoxy bonding process. Because of how the parylene film is deposited and how the chip is inserted, the epoxy well on the bonding pads on the edge of the chip becomes very difficult to fill (shown in figure 5.25). The parylene film near the edge would sometimes be damaged during the squeegee process because of the transition from an area with back support to an area without. A PDMS chip molding technique is thus developed to alleviate this problem and to increase the yield and effectiveness of the squeegee epoxy process.

The mold process is shown in figure 5.26. PDMS is poured on top of a dummy chip to create a cavity for the actual functional chip. After the functional chip is fitted into the cavity, the PDMS mold (shown in figure 5.27) is trimmed with a cookie cutter-like cutter to create the final shape to be inserted into the parylene pocket.

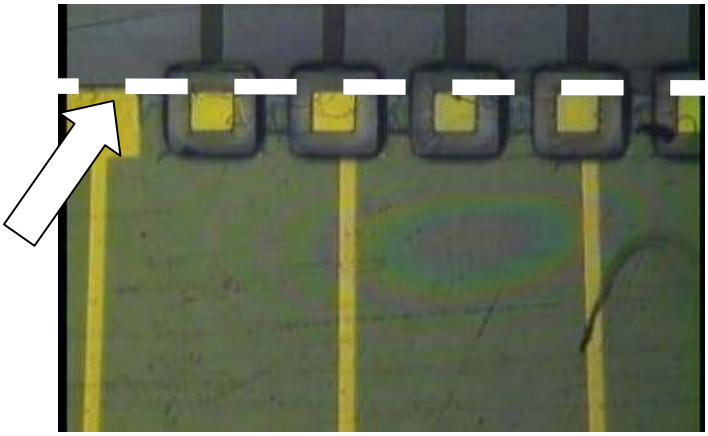


Figure 5.25. Edge of the chip—where the squeegee process may become a problem.

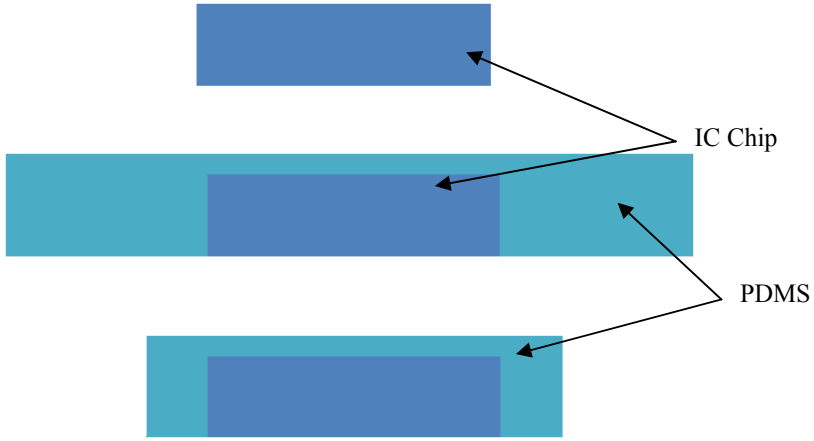


Figure 5.26. Chip edge protection process: PDMS is poured on top of the IC chip and later trimmed to shape to be inserted into the pocket.

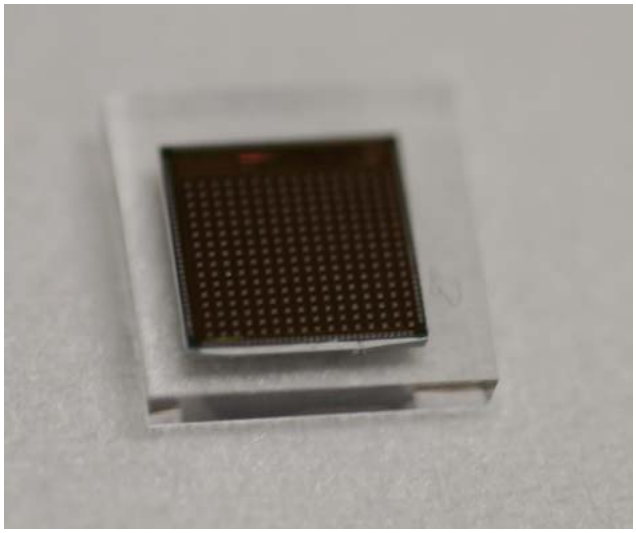


Figure 5.27. PDMS mold fitted with a 256-channel stimulation chip.

5.3.3 Repairs and Enhancements

Due to fabrication defects and contaminations during wafer transport or handling, sometimes short circuits and open-circuits of neighboring traces become unavoidable. In some cases the short circuits may occur on stimulation channel wires. These short circuit defects may have little to no effect to the overall functionality of the system. However, they may have catastrophic effect when they occur on chip control lines or power supply lines, without which the entire system would not function. As a result, repair methods and fixes were developed with the laser system mentioned in the previous section to fix these problems.

5.3.3.1 Laser Fix (Short Circuit)

Figure 5.28 shows a case of short circuit of neighboring traces due to particle contamination during photoresist lift-off lithography process. This type of issue could occur on either stimulation or chip control lines and could have adverse effect of the functionality of the system and must be repaired. A method is presented here to etch away the excess metal that causes the short by laser pulsation with a UV laser trimming system. The software on the laser trimming system allows the user to control the power, size, frequency of each pulse, and the number of total pulses emitted to enables the laser's ability to selectively etch away different materials. Table 5.3 lists the recipe that is used to open different materials and figure 5.29 and figure 5.30 show the etching process of the different layers.

Ideally, in order to open short circuits that are embedded in the parylene sandwich layer, the top parylene must first be etched away to expose the metal underneath. After the metal is exposed, a different recipe must be used to slowly etch the metal away

without damaging the bottom layer parylene in order to retain as much of the original structure as possible. A coat of parylene needs to be done after this process to protect the etched area and to prevent accelerated soaking or mechanical failure. This process is shown in figure 5.31.

However, experiments with the laser system and different structures show that etching through the entire structure with a more powerful laser pulse, leaving a hole through the parylene, can achieve similar results.

Figure 5.28. Short circuit defect on dense metal lines.

Table 5.3. Laser process recipe to etch specific materials on the parylene skin structure.

Layer	Type of Laser	Power	Number of pulses
Top Parylene Layer (5 µm)	UV	15% of full power	200
Gold Metal Layer (0.2 µm)	UV	35% of full power	7

It should be noted that the shortage underneath the parylene film due to low viscosity mentioned in previous section can also be fixed with this laser etching method. Shown in figure 5.32a, the conductive epoxy seeped underneath the parylene film and shorted out the neighboring two pads even though there is no shortage on the surface of the parylene film (figure 5.32b). Ultraviolet laser can thus be used to cut through the film

and clear the shortage underneath (figure 5.33). Conduction test shows that the once-shorted neighboring pads can be successfully separated electrically with this process.

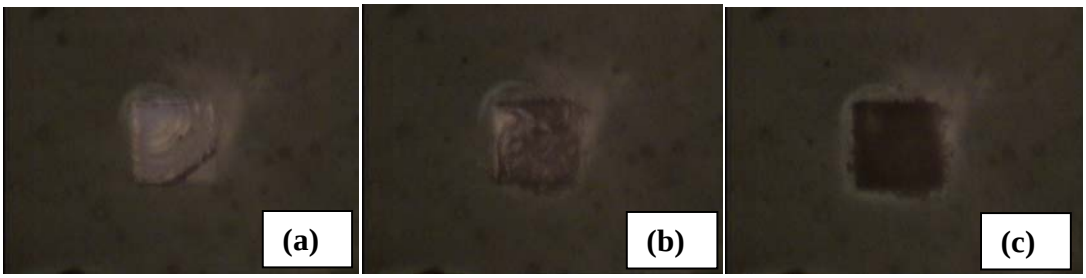


Figure 5.29. Laser etching of the parylene layer; (a) after 30 pulses; (b) after 60 pulses; (c) after 200 pulses.

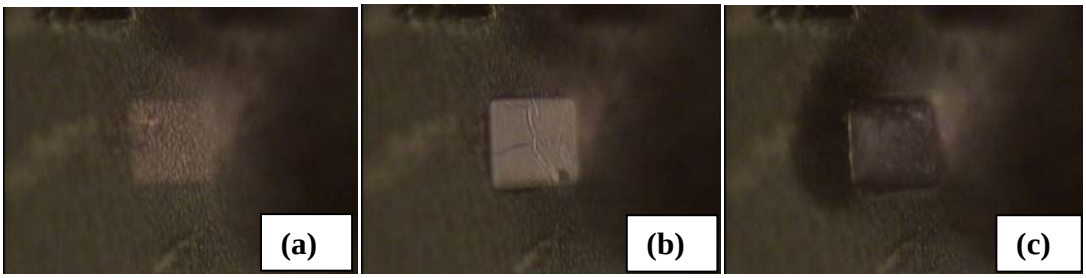


Figure 5.30. Laser etching of the gold metal layer; (a) before; (b) during; (c) after.

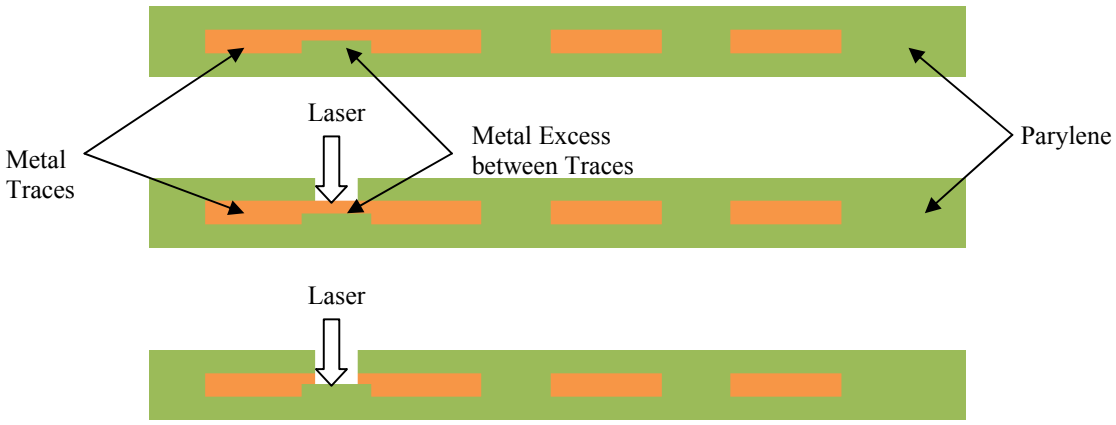


Figure 5.31. Short circuit defect repair process; laser is used to first open the parylene, followed by a short etch of the metal excess in between the metal lines.

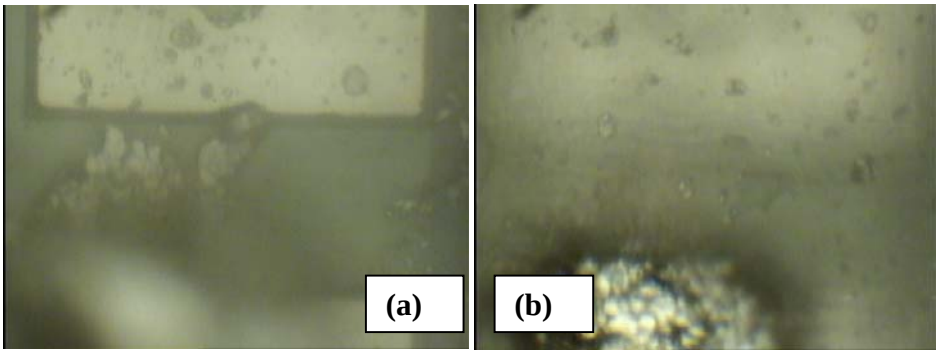


Figure 5.32. (a) Shortage of neighboring metal pads underneath the parylene film due to low viscosity of the conductive epoxy; (b) even though the surface of the parylene film is free of conductive materials.

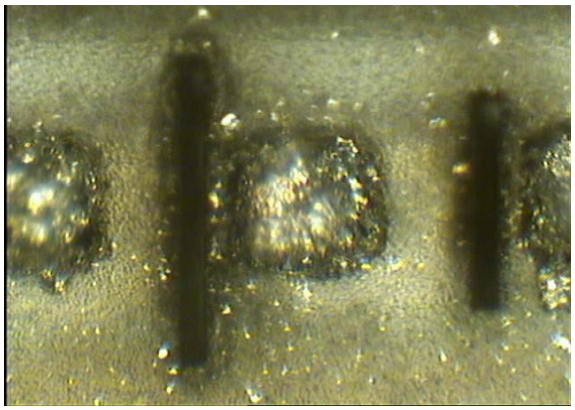


Figure 5.33. After ultraviolet laser cleaning. The laser cuts through the film and clears away the excess conductive material underneath the parylene film and on top of the chip to again electrically isolate the neighboring pads.

5.3.3.2 Conductive Epoxy Failures

The goal of the conductive epoxy application is to make permanent electrical connection from the bonding pad on the parylene film to the metal pads on the chip regardless of the shape or form of the conductive epoxy, as long as it does not short circuit the surrounding pads. However, after the epoxy application, some wells may not have this contact. The following cases were observed and considered (shown in figure 5.34).

In the first case, the conductive epoxy hangs on the two sides of the well, makes contact with the bonding pads on the parylene pocket but not the metal pads on the chip.

This problem occurs most often if the well is not deep enough to retain the conductive epoxy. One can fix this problem by manually applying another drop of epoxy on top of the well.

In the second case, the conductive epoxy completely fills the top of the well but does not make contact with the metal pad of the chip at all. This problem occurs most frequently when the well is too deep (>100 μm) and when there is not enough conductive epoxy to fill the well entirely. One can fix this problem by using the laser to melt the conductive epoxy blob in the middle so it reflows and make contact with the chip pad. One can also manually push the epoxy into the well with a pin to force contact with the chip pad.

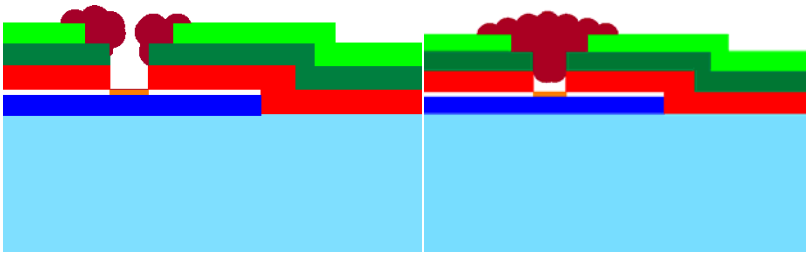


Figure 5.34. Bad electrical contact of the conductive epoxy between the bonding pad on the parylene pocket and the metal pads on the chip.

5.4 Functional Testing

Device testing is performed in three stages: dummy chip integration testing, accelerated life testing and stimulation chip integration testing. In the first stage, five dummy chip integrations were completed (figure 5.35). Result shows all pads that are required can be bonded in less than 1 minute after alignment. On average, less than 10 fixes for short circuits and open circuits are needed after each chip bonding. 100% of

the pads are functional after these repairs. This results in a yield higher than 96% before repair and 100% after repair.

After a complete device is made, commercial discrete components such as capacitors, resistors and inductors are connected to the pads on the parylene (shown in figure 5.36) and are tested with a function generator. Sine waves of different frequency were passed into the chip and the components. The output shown in figure 5.37 concludes a successful functionality testing of our packaging technology. This result shows its potential to be used in a fully integrated system.

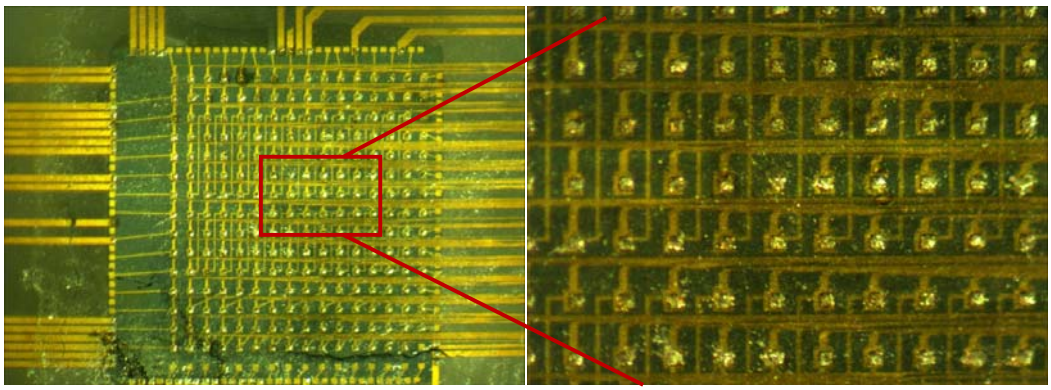


Figure 5.35. Dummy chip integration with squeegee technique

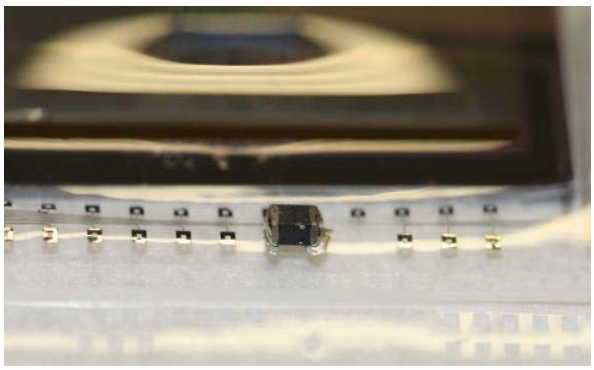


Figure 5.36. Surface mounted resistor bonded on two of the metal pads on the parylene sheet. Note that all discrete components, including MEMS inductive coils, can potentially be integrated with this structure.

In the second stage of device testing, an ongoing accelerated lifetime soaking test is being conducted to determine the mean time to failure of the devices. Testing shows

the pocket structure with 1.5 mm of biocompatible silicone is able to function after soaking in 90ºC saline for more than 30 days. This result translates to years of lifetime in saline at 37ºC, which is also reflected in previous chapters.

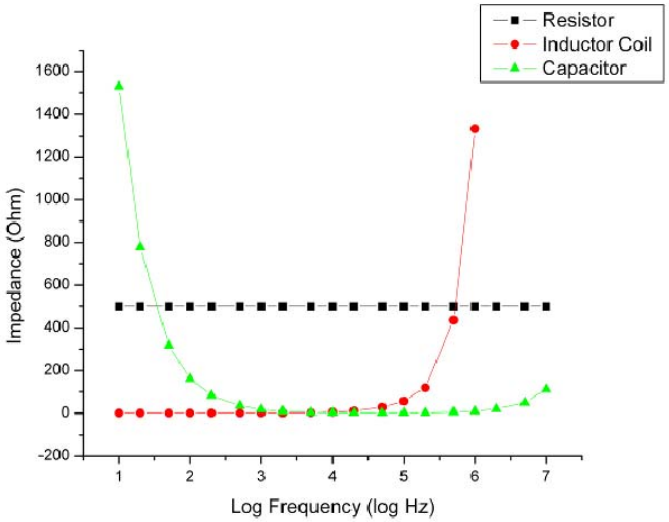


Figure 5.37. Frequency vs. impedance plot of the discrete components that were bonded and tested with our parylene structure.

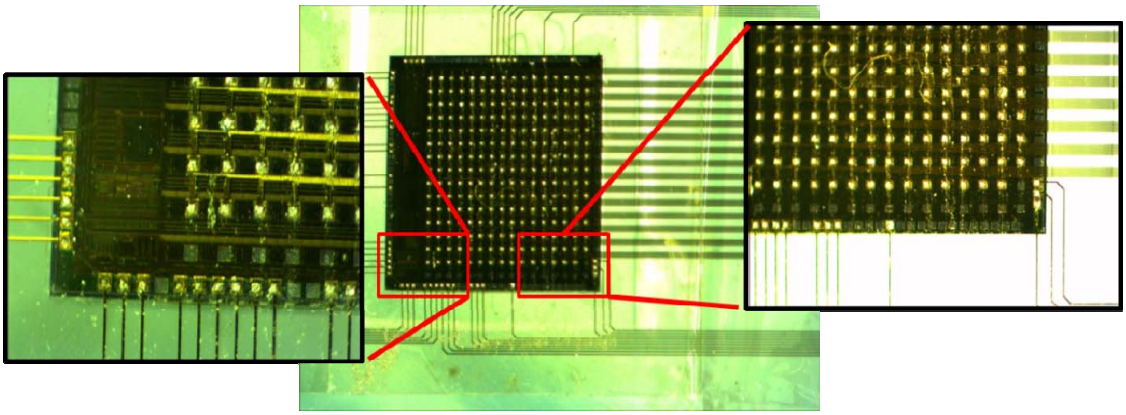


Figure 5.38. 256-channel integration with high density squeegee bonding technique

Finally, the actual 256-channel chip is integrated with the parylene integration platform and tested by University of California, Santa Cruz (shown in figure 5.38). Basic chip functionality is successfully tested and a plan to integrate the entire system for implantation and to develop a 1,024-channel stimulation chip is underway.

5.5 Conclusion

This chapter presents two designs of the parylene integration platform for high density stimulation channel for retinal prosthesis. Much effort has been put in to optimizing the fabrication and integration process for constructing an ideal and functional pocket to accommodate a custom chip that is designed for this purpose. The issues and challenges including parylene cracking, metal line lift-off, and thick photoresist etching that one might encounter while building both parylene pocket on silicon substrate and parylene substrate are discussed and investigated. This chapter also presents several techniques to either solve or alleviate some of these fabrication and integration challenges. The techniques include a high density squeegee metal pad bonding, screen printing, short circuit and open circuit repair technique that utilizes laser technology, a highly efficient RIE etching technique, optimization of lift-off photoresist to facilitate metal line definition, and a PDMS molding technique to protect the IC chip that is to be inserted into the pocket.

In the end, a conduction dummy chip has been fabricated to test the functionality of the platform and the efficiency of the bonding process. A printed circuit board has also been designed and built to integrate the entire system together for system testing. Future work is underway to integrate data and power coils on this platform to simulate a total system that will eventually be implanted *in vivo*. The multilayer technology presented in chapter 2 also allows the wiring to be done on more than one layer of parylene, to enable the integration of a chip with even higher pad density. It is believed that this new technique can be further scaled to achieve 10,000 connections in an area of 1 cm^2.

Although a comprehensive system testing is still under progress, positive initial result from these basic functional tests, along with a promising prototype and a plan to implant a complete system *in vivo* in the near future, has proven this technology to be an extremely useful and efficient method in advancing the research and development process for a complete, working retinal prosthetic system that will enable a blind patient to be able to see again.

6 CONCLUSION

We have successfully utilized MEMS micromachining and parylene technology to make flexible parylene platforms that can be monolithically fabricated with other MEMS devices and can house commercially available IC chips and discrete components. This technology and its various forms were discussed in chapter 2. Two complete integration processes with two different circuits were demonstrated in chapter 3. Their respective functionality have been successfully shown and verified, which further validated the efficacy of this technology. In chapter 4, the mechanical, water diffusion, and long-term survival properties of the packaging were discussed in length by *in vivo* studies and accelerated testing. Finally, a high-density bonding paradigm was introduced to solve the interconnection problem that has not been addressed completely by the state-of-the-art technologies.

The three major technologies being developed to build a complete implantable system include electrode technology, wireless technology and interface technology. Continuous improvements and progress of each sector are being made every day to achieve the subsystem integration and miniaturization by various different research efforts. *In vivo* testing of fully functional models are also possible as a result of the conglomeration of work done by these technologies thrusts. With this goal in mind, the integration of the high density chip that is presented in this dissertation only served as a precursor for what is to come in the future.

On the other hand, it should be noted that the use of this technology is not only limited to retinal or brain prosthetic applications/interfaces. Because of the extremely high throughput and precision of this technology, it can be easily adapted by the integrated circuit fabrication industry to enable higher density applications. When the combination of the epoxy and the aspect ratio of the photoresist well that retains it have been optimized, one single device with 1,000 or more connections can be connected in the matter of seconds with close to 100% yield.

It can thus be concluded from this evidence that the parylene pocket technology with the squeegee bonding method not only has the potential to impact the IC packaging industry, but more importantly, it can lead to new generations of implantable bioelectronic devices that could potentially restore the quality of life of patients who suffers from various degenerative diseases.

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